PCI Express 3.0 PHY Electrical and CEM Update

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Agenda

- PCI Express® (PCIe®) 3.0 Electrical Requirements
- PCIe 3.0 Data Rate
- PCIe 3.0 Electrical Optimizations
- PCIe 3.0 Architecture Overview
  - ✓ Transmitter
  - ✓ Receiver
  - ✓ Reference Clock
  - ✓ Channel
- PCIe 3.0 CEM Requirements and Analysis
- Summary and Conclusions

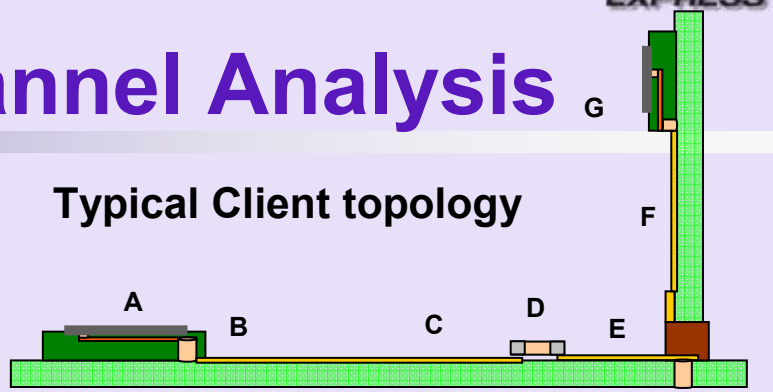
PCI Express 3.0 Electrical Requirements

- 2x the data payload BW of PCIe 2.0
- Full backwards interoperability with PCIe 1.x, PCIe 2.0
- Same cost structure for high volume platforms
- Continue to support common clock and data clock architectures
- Same or better mW/GB/s power budget as PCIe 2.0
- Same channel reach as for PCIe 2.0
  - ✓ Client: 14 inch, one connector
  - ✓ Mobile: 8 inch, one connector
  - ✓ Server: 20 inch, two connectors
- Re-use of Refclk components
  - ✓ Jitter performance need not be improved

PCI Express 3.0 Channel Analysis

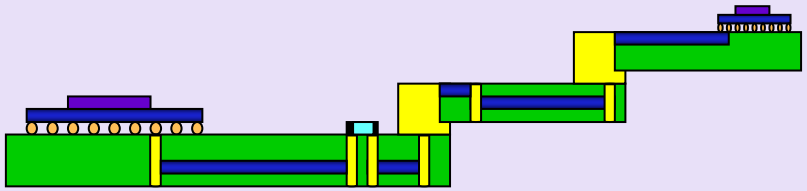
- Client
  - ✓ Motherboard and adapter
  - ✓ 1 PCIe connector
  - ✓ No vias other than connector
  - ✓ Routed as mstrip
  - ✓ Channel length: ~14”
- Server
  - ✓ Motherboard, riser card, and adapter
  - ✓ 2 PCIe connectors
  - ✓ Several vias on motherboard
  - ✓ Routed primarily as stripline
  - ✓ Channel length: ~20”
- Channel analysis includes corner cases

Typical Client topology



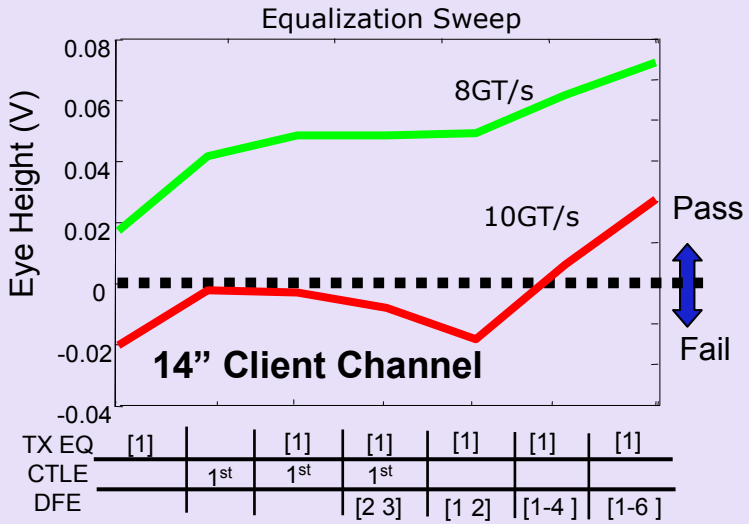
Seg	Description
A	MCH PKG (transmitter)
B	Break Out
C	MB Main 7”
D	MB post cap
E	Add in card main 3”
F	Add in card PKG Break out
G	Add in card PKG (receiver)

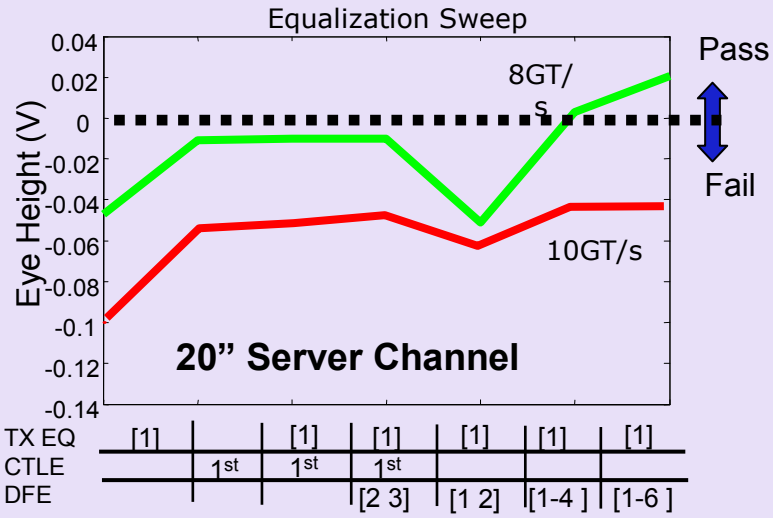
2 Connector Server topology



PCIe 3.0 targets support for the same channels and lengths as PCIe 2.0

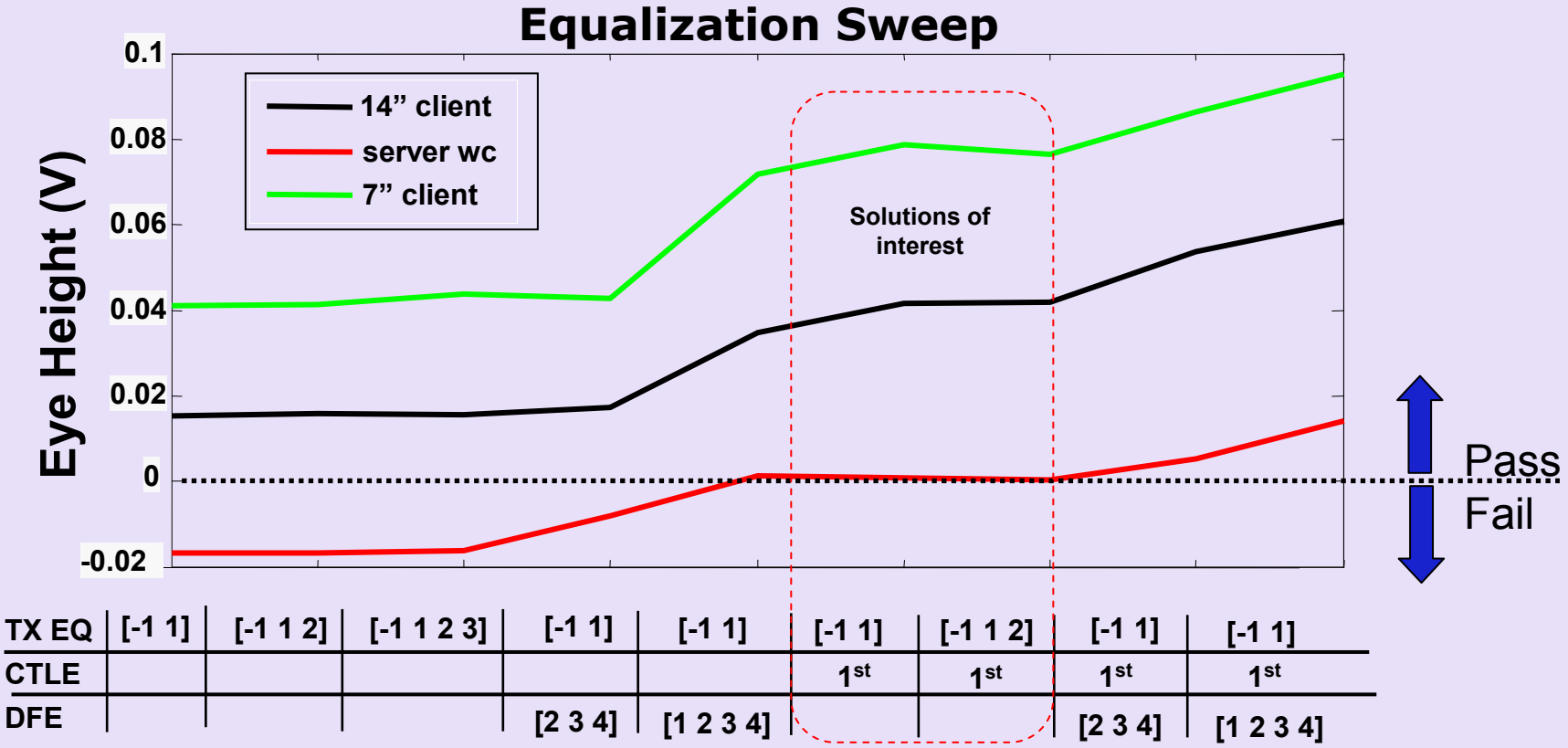
8GT/s Solution Space





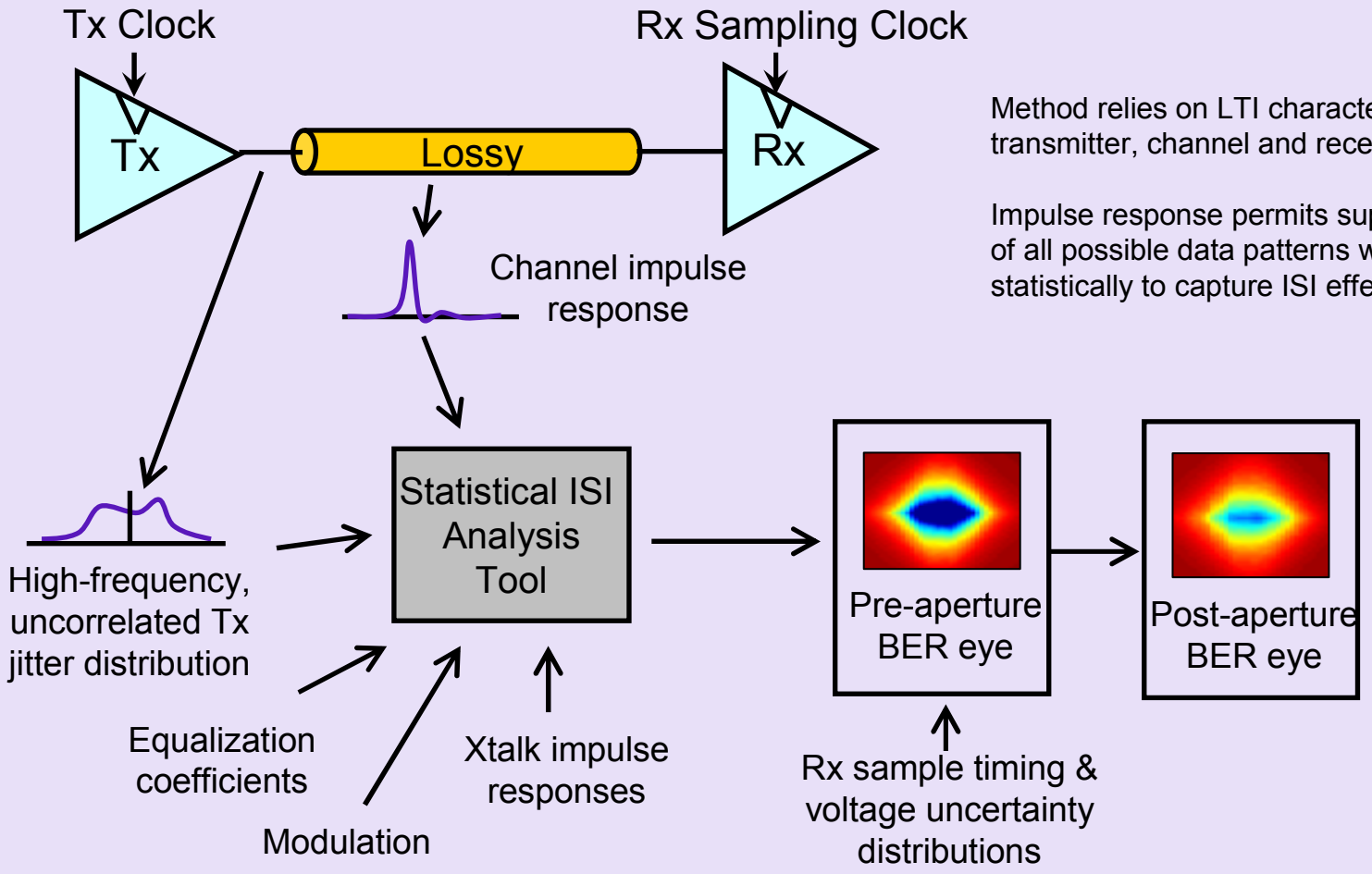
- Solution space exists to satisfy 8GT/s client and server channels requirements
  - ✓ Power, channel loss and distortion much worse at 10GT/s
- PCI-SIG® voted to adopt 8GT/s in Q2'07

Margins vs. Equalization Type



With the exception of a few w/c max length server channels, a combination of Tx de-emphasis and Rx LE yields positive margins. Voltage/jitter margins may be increased by use of more complex Rx equalization techniques.

Statistical Analysis Methodology



Method relies on LTI characteristics of transmitter, channel and receiver

Impulse response permits superposition of all possible data patterns weighted statistically to capture ISI effects

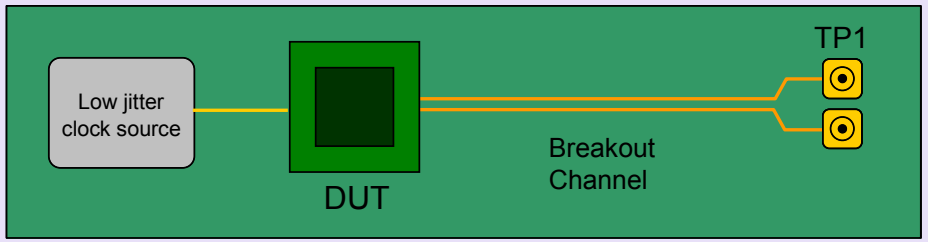
Source: Intel Corporation

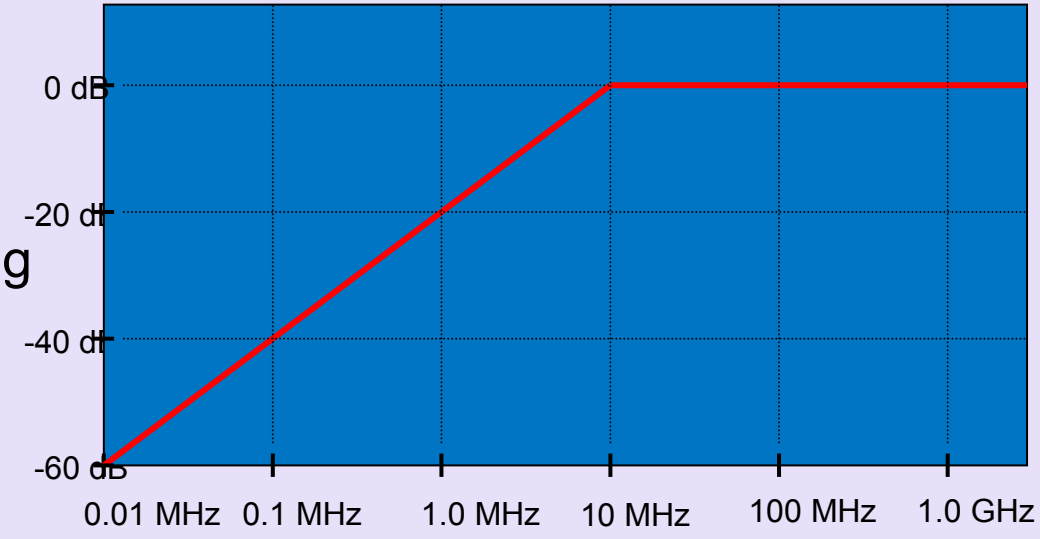
PCIe 3.0 Electrical Optimizations

- Tx de-emphasis
  - ✓ Several presets to accommodate different classes of channels
  - ✓ One post cursor tap and (possibly) one pre cursor tap
- Receiver equalization
  - ✓ 1st order LE is assumed as minimum Rx equalization
  - ✓ Spec does not stipulate what type of Rx eq. may be implemented
- Optimizations for Tx, Rx PLLs and CDR
  - ✓ PLL BW reduced, CDR jitter tracking increased
- Employ statistical methods in identifying solution space
  - ✓ Properly account for all Tx, Rx jitter components
  - ✓ Model interaction between scrambled data and channel

Transmitter

- Measurements at the end of breakout channel(s)
  - ✓ May need a long and short channel.
- TX Jitter parameters
  - ✓ Tj > 10 Mhz
  - ✓ Djdd > 10 Mhz
  - ✓ DCD (Duty cycle distortion)
- TX Voltage parameters
  - ✓ V swing for full and half swing
  - ✓ De-emphasis
    - – Dynamic Range
    - – Resolution
- TX Return Loss





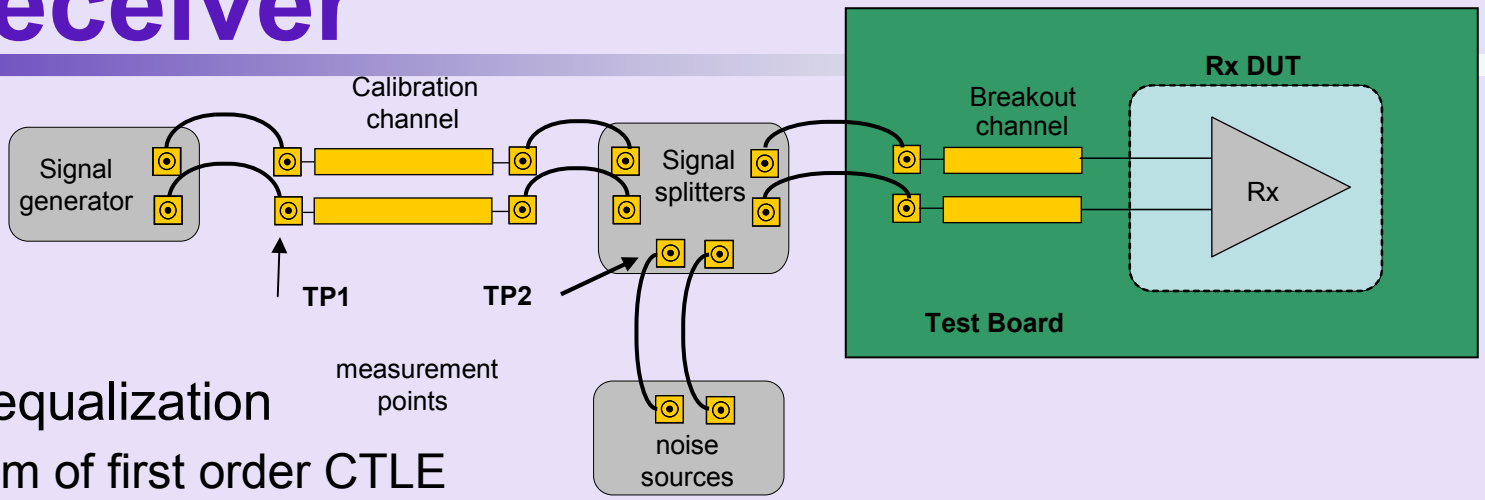
Tx De-Emphasis

- Investigating Tx and Rx equalization requirements for given topologies
- 1 pre-cursor and 1 post-cursor
- Open question on whether TX de-emphasis needs to adjust based on receiver feedback
- Tolerance of Tx de-emphasis settings used for channel validation must be consistent with w/c

Tx and Rx Multiplying PLL

- 5GT/s allows a minimum Tx PLL bandwidth of 5MHz with 1dB jitter peaking
- Investigating using a 5MHz to 10MHz PLL bandwidth with 1dB peaking and 10MHz CDR (0.3 draft has 2MHz to 4MHz)
  - ✓ Provides overlap with 5GT/s requirements
  - ✓ Increased bandwidth relaxes phase noise requirements on PLL VCO
  - ✓ Receiver tolerance testing ensures CDR will reject low frequency phase noise
- High bandwidth CDR makes up for reduced attenuation of LF jitter from higher PLL bandwidths
- Allows backward compatibility with 2.5GT/s and 5GT/s
  - ✓ Common PLL architecture can be used for 2.5GT/s – 8GT/s
  - ✓ Multiple PLLs only needed for devices that support splitting links

Receiver

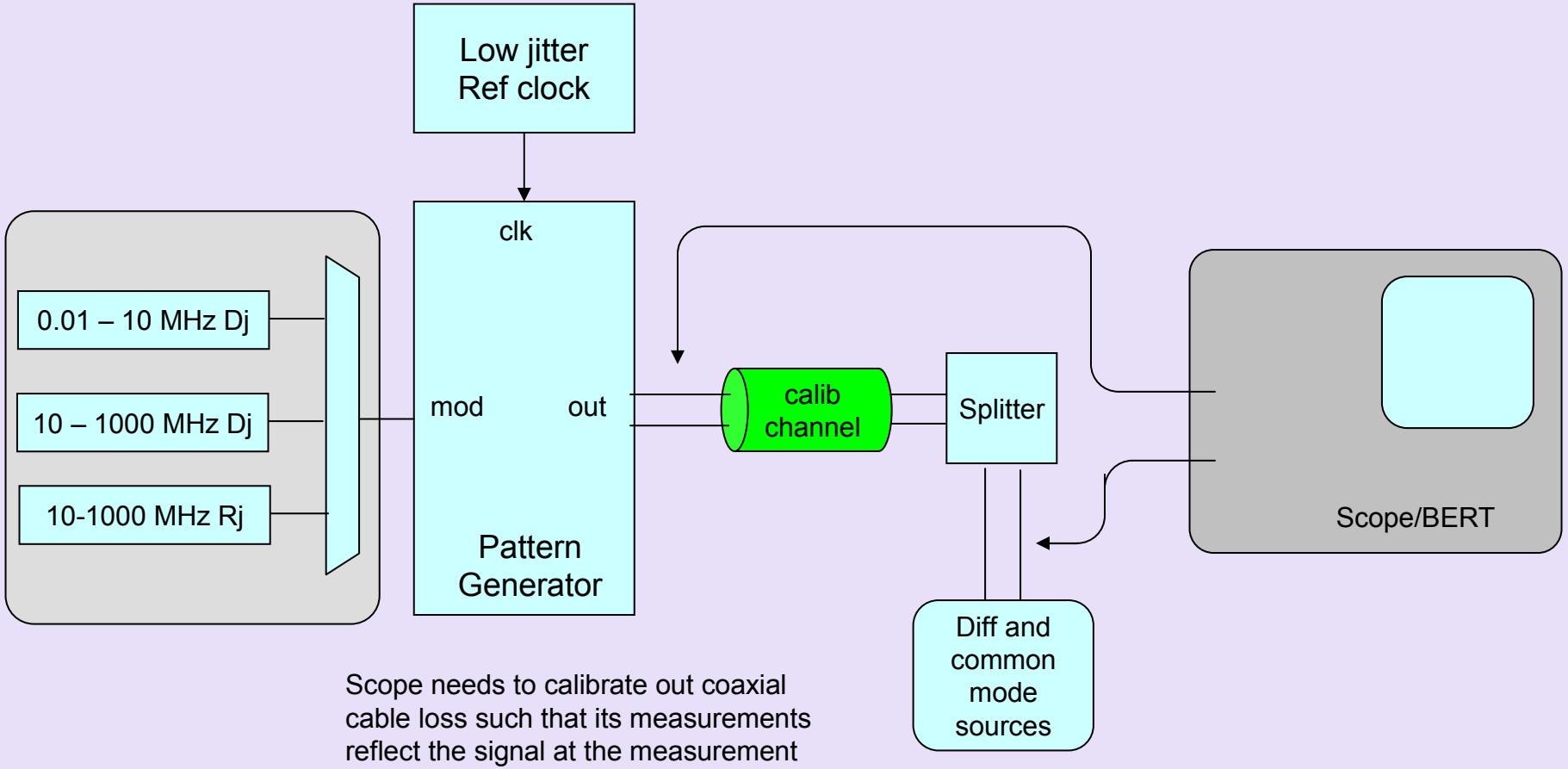


- Receiver equalization
  - ✓ Minimum of first order CTLE
- Tolerancing approach similar to PCI Express (PCIe) 2.0
  - ✓ Pass/fail requirement in term of BER with worst case input signal
  - ✓ Precisely defined compliance channel(s) to inject ISI
  - ✓ Calibration done at output of signal generator (add setup picture)
- Jitter Injection
  - ✓ Low frequency (10 khz – 1 Mhz)
  - ✓ Mid frequency (1 – 10 Mhz)
  - ✓ High frequency (10 Mhz – 1 Ghz)
- Voltage Injection
  - ✓ Common mode (Power supply noise)
  - ✓ Differential mode (crosstalk)

CDR Bandwidth

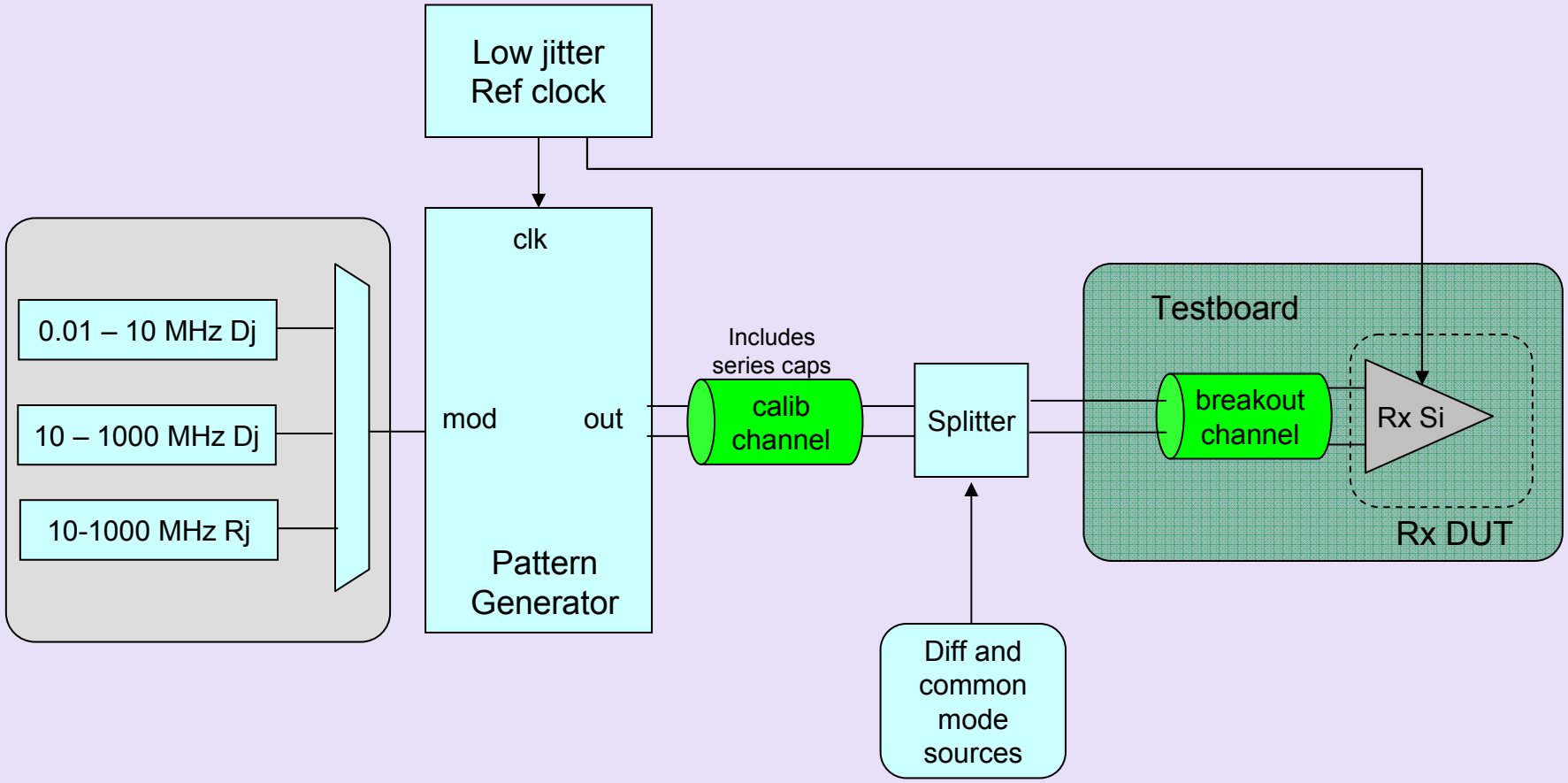
- Key to solving these problems is to place burden on the Rx CDR
  - ✓ 2.5GT/s and 5GT/s have no specific CDR phase tracking requirements
  - ✓ 8GT/s higher data rate allows CDR bandwidth to be increased
- 8GT/s Rx tolerance testing validates CDR tracking performance
  - ✓ Rx must tolerate 0.35UI of additional sinusoidal eye closure at 1MHz compared to minimum eye opening
- Studies of typical bang-bang digital CDR implementations indicate they can be designed to meet this requirement
  - ✓ Expectation is that existing Rx CDR's can be modified to meet these requirements for 8GT/s
- Conservative model of 1st order high pass filter accurately bounds CDR behavior.
  - ✓ Minimum bandwidth target is 10 Mhz for PCIe 3.0

Calibrating into scope
(Common Refclk arch)



Scope needs to calibrate out coaxial cable loss such that its measurements reflect the signal at the measurement reference plane

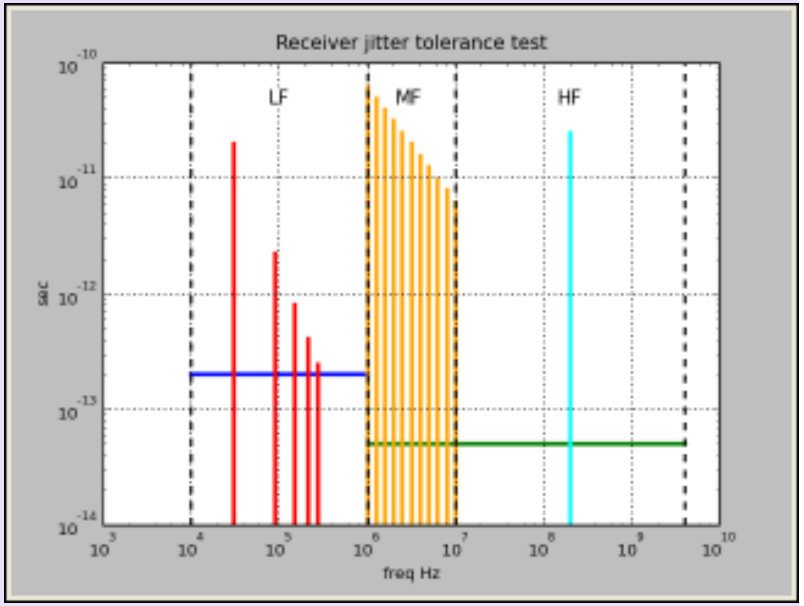
Tolerancing Rx under test
(Common Refclk arch)



Receiver tolerance testing

- To be able to rely on the receiver to follow a first order high pass we need to test its response
- We can add a jitter tolerance test that phase modulates the data source and sweeps the frequency
  - ✓ Voltage waveform generated like PCIe 2.0 with a calibration channel to generate ISI
- At high frequency (>10MHz) two sinusoids are calibrated to create a limit stressed eye as in PCIe 2.0
  - ✓ Use a variable and fixed frequency
  - ✓ 10MHz ~0.04UI pk-pk (5ps) + 200MHz ~0.2UI
- Variable frequency sinusoid is then swept to a lower frequency increasing its amplitude from 10MHz to 1MHz at 20dB per decade
  - ✓ 1MHz ~0.4UI pk-pk (50ps) + 200MHz ~0.2UI

Approx scale for illustration

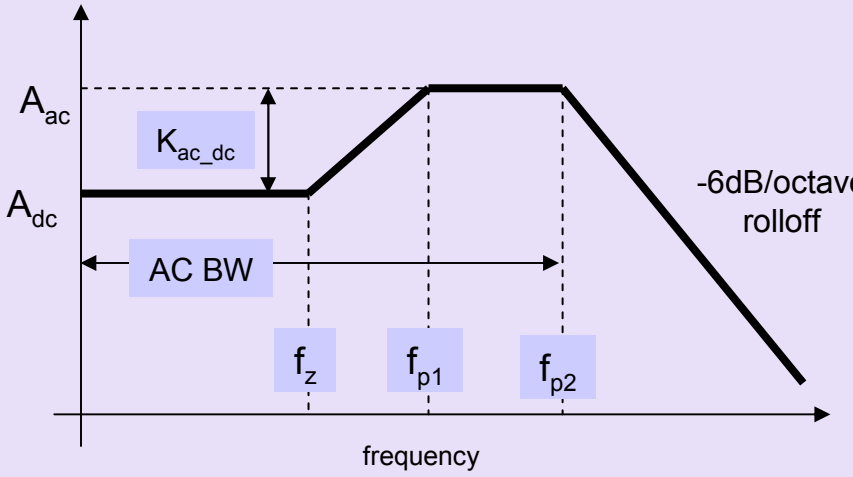


Key:
RED: residual SSC
BLUE: LF RMS
GREEN: HF RMS
ORANGE: MF sinusoidal
CYAN: HF DJ

N.B. Only one MF spur applied at a time

Rx Reference Equalizer

- Reference equalizer represents minimum Rx requirements to guarantee interoperability
  - ✓ Defined by a simple transfer function
  - ✓ Actual Rx equalizer must be as good or better
- Rx: Rx equalizer is defined by several parameters
  - ✓ AC vs. DC gain, Zero frequency, AC BW, Gain BW
- Goal is to minimize number of parameters that need to be adjusted
  - ✓ AC vs. DC gain from K_{AC-DC} = 1 to 4 in 16 steps



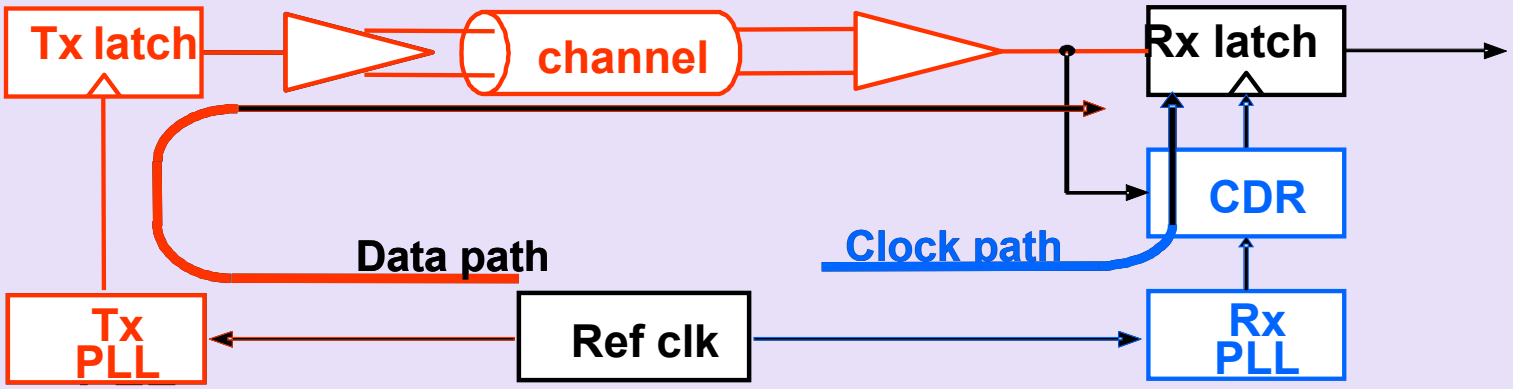
$A_{ac} = (GBW / f_{p2})$

$A_{dc} = A_{ac} / K_{ac\_dc}$

$f_{p1} = f_z * K_{ac\_dc}$

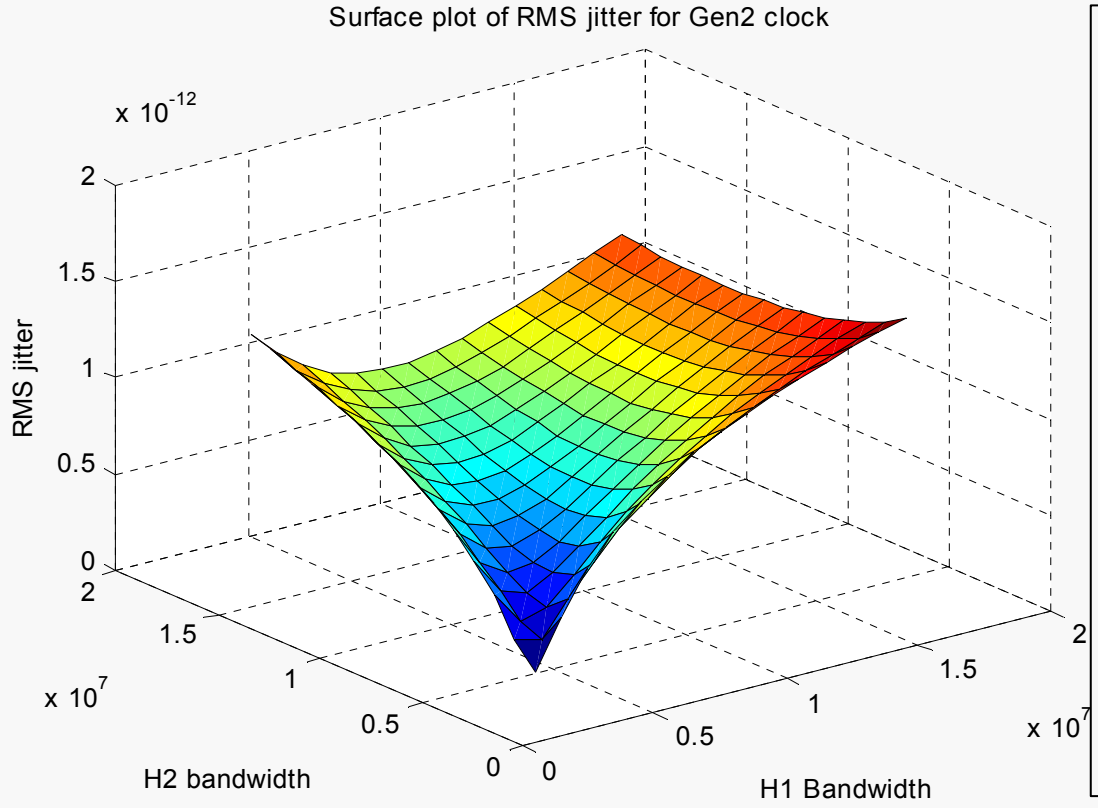
Reference clock

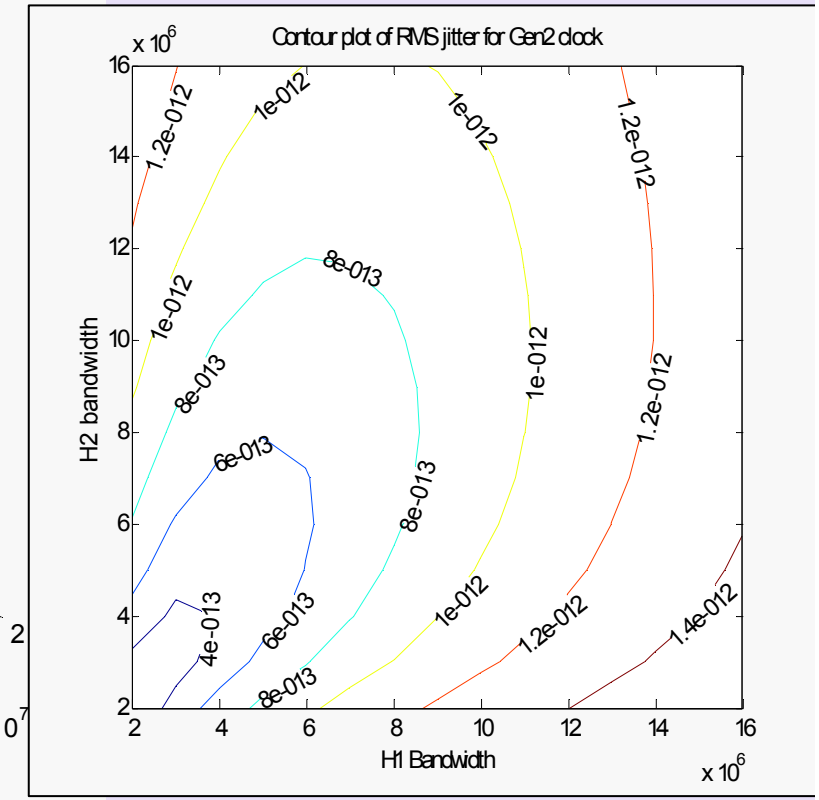
- Same usage model as PCI Express (PCIe) 2.0
  - ✓ Common clock jitter defined by transfer function HT=(H1-H2*delay)*H3
- Challenging area
  - ✓ At 5.0 GT/s Reference clock consumes significant portion of timing budget. (3.1 ps RMS)
- Goal is to use the same reference clock components
- Goal for 1 ps RMS effective jitter after CDR bandwidth and PLL bandwidth optimizations



Reference Clock Jitter For Marginal 2.0 Component

- Filter characteristics
  - ✓ 10 MHz H3 (3.0 target)
  - ✓ Sweep PLL bandwidths 2-16 Mhz. 1.5 dB Peaking
    - 12ns of delay lumped onto H2 transfer function

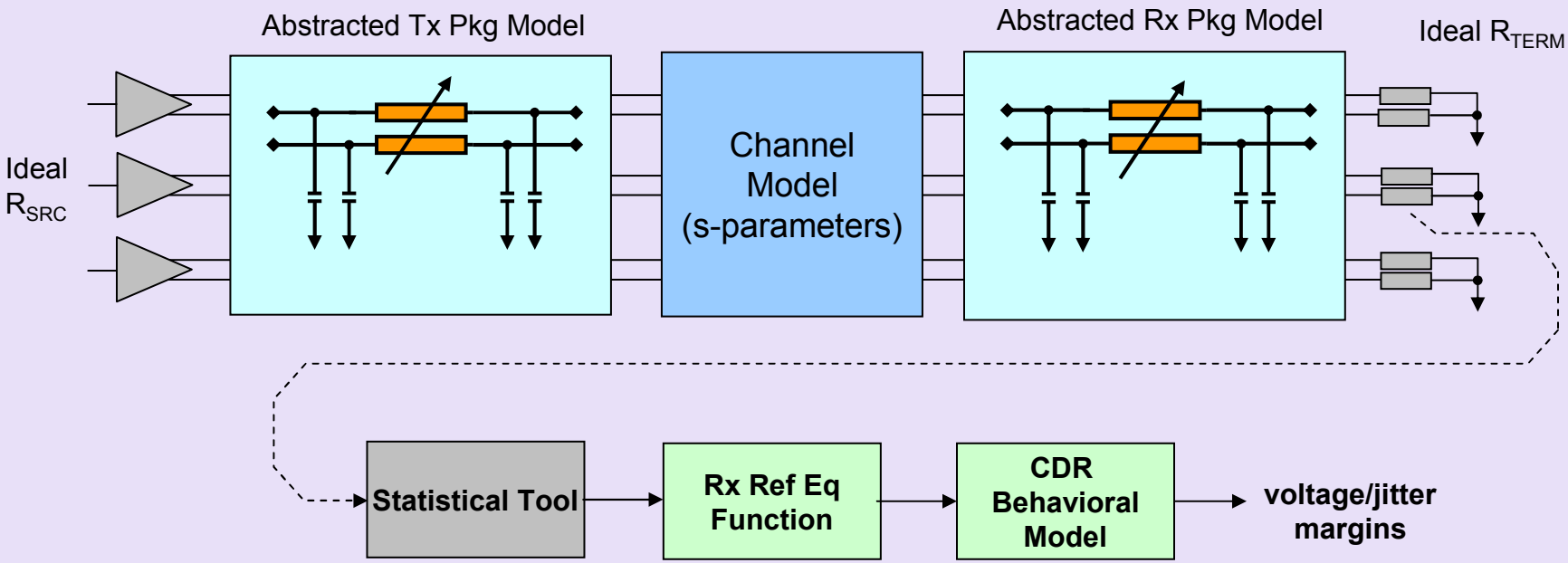




Channel Validation

- Investigating channel pass/fail using Tx/Rx parameters
  - ✓ A channel meets requirements if, when driven by W/C Tx into W/C Rx, the eye at Rx die pad meets Rx spec (after applying Rx equalizer and CDR behavioral models)
- Start with PCIe 2.0 approach
  - ✓ Capture channel as s-parameter or similar model
  - ✓ Define W/C Tx characteristics
  - ✓ Combine Tx and channel and observe results at far end of channel
- Investigating new ingredients
  - ✓ Tx and Rx parameters referenced to die pad, not the pin
  - ✓ Include abstracted Tx and Rx package models
  - ✓ Reference Rx equalization algorithm
  - ✓ Statistical tool captures data/channel/jitter interaction

Channel Validation Methodology

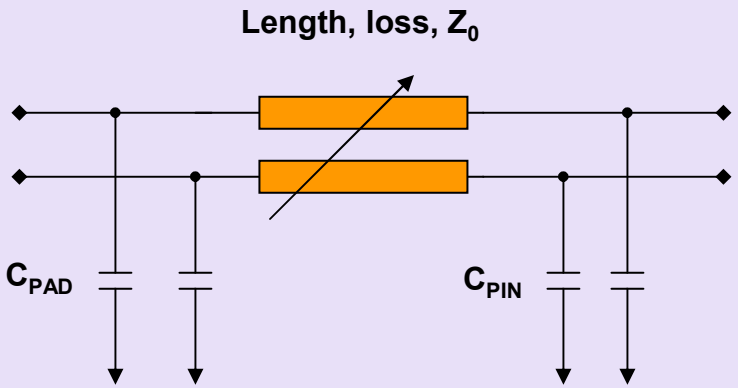


- Channel validation utilizes a combination of measured, fitted, and behavioral models
  - ✓Channel is measured and converted into s-parameters
  - ✓Tx, Rx package models are fitted
  - ✓Rx Ref equalizer and CDR are behavioral models

- Statistical tool convolves data pattern with pulse response of channel plus packages

Abstracted Tx Package Model

- Goal is to represent package in terms of a small number of parameters that can then be defined in the specification
- Example: Package is definable as a Pi model terms of C_{PIN}, C_{PAD}, and a lossy t-line with min/max swept length
  - ✓ Sweeping in necessary to excite potential pkg/channel resonances
- Methodology is based on assumption that discontinuities can be captured by C_{PAD} and C_{PIN}
- Show that abstracted pkg model's time domain behavior matches that of measured pkg model



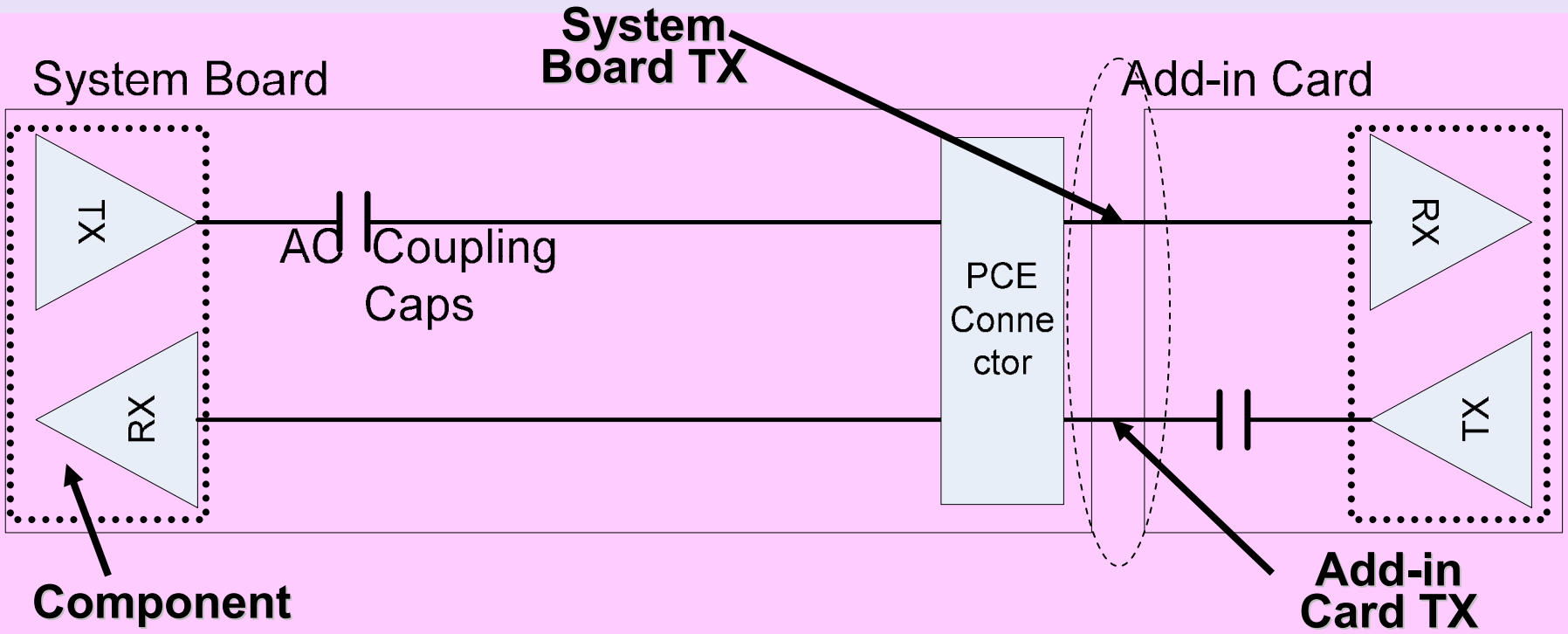
Package Parameters

$C_{PAD} \leq 1.5$ pf (max)
$C_{PIN} \leq 0.5$ pf (max)
50 mils ≤ Length ≤ 1500 mils
$80\Omega \leq Z_0 \leq 100\Omega$
loss/length 0.25 dB/GHz/Inch

PCI Express 3.0 CEM Goals

- Backwards compatibility
- No required changes to the connectors, card form factors, or material.
- Minimal or no changes to the measurement methodologies from those used in the PCIe 1.x/2.0 specifications.
  - ✓Use eye diagrams (jitter/voltage margin requirements). Minimize additional new requirements

CEM Spec – TX Path



CEM Spec Defines TX Requirements for Chip + Interconnect

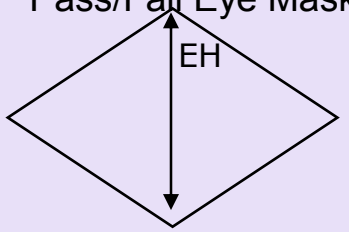
No Separate TX Chip Or Interconnect Only Requirements.

PCIe 3.0 CEM Simulation Method Under Investigation - Step 1: End to End (E2E) Simulations

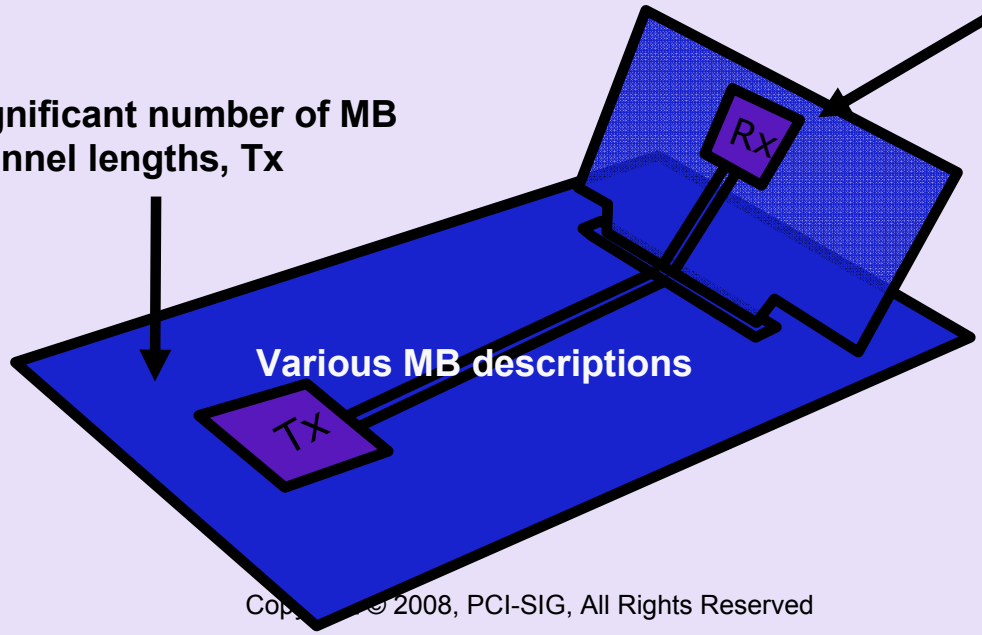
- Perform E2E simulations
  - ✓ Use target 1 connector and 2 connector solutions
  - ✓ Eye height (EH) and eye width (EW) examined after first order CTLE at die pad
  - ✓ Statistical tools used for all simulations
- Fix MB parameters and determine pass/fail conditions across expected add-in card solution space
- Repeat with many motherboard parameters

Sweep add-in card parameters over reasonable solution space

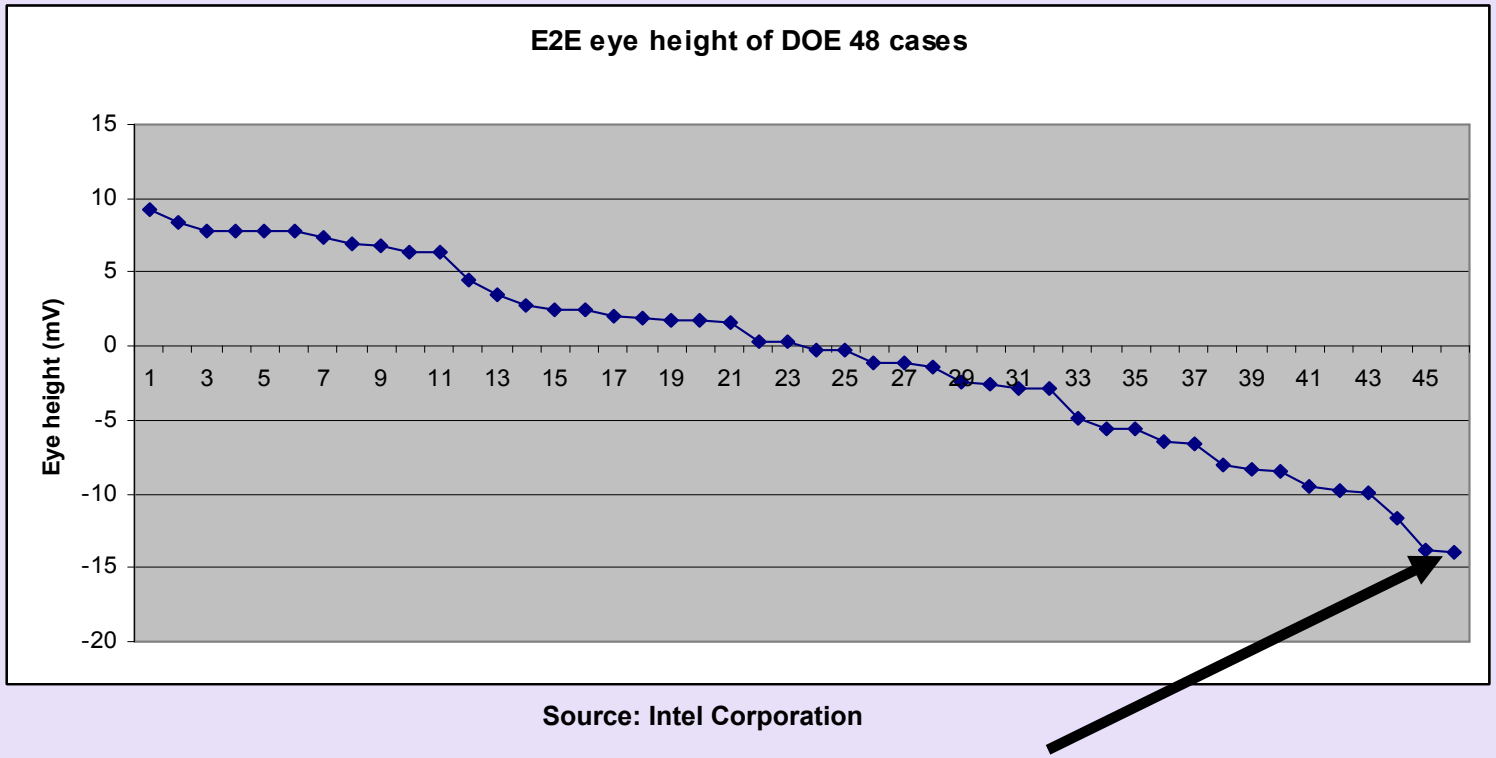
Pass/Fail Eye Mask



Create a statistically significant number of MB descriptions. (Vary channel lengths, Tx params, etc.)



CEM Simulations - Worst Case Eye Height



Source: Intel Corporation

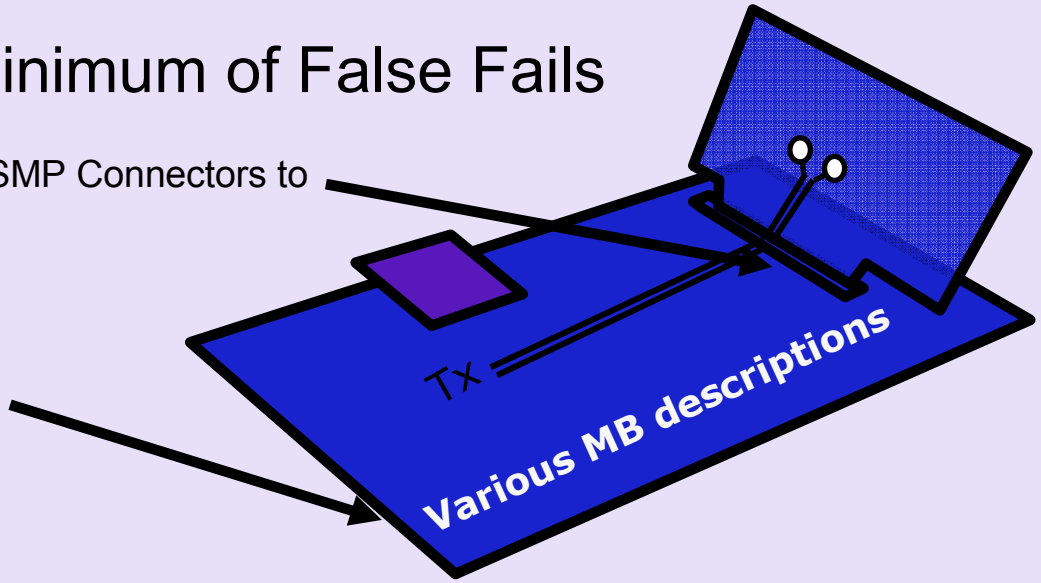
- Worst case Add-in card (AIC) parameters for given MB
- Repeat simulation with different MBs and find worst case for each
- THE ONLY POINT OF INTEREST FOR EACH SET OF MB PARAMETERS IS THE AIC PARAMETERS THAT GIVES WORST CASE

PCIe 3.0 Simulation Method Under Investigation - Step 2: Test Fixture Simulations

- Choose a test fixture
  - 2.0 CLB Test Fixture Used For Initial Investigation
  - No receiver equalization applied (eye is open)
- Repeat previous MB simulations with test fixture
  - Determine an eye mask at compliance Test Point
  - Find correlation between EH (and EW) at Test Point vs. end to end results
- No False Passes and a minimum of False Fails

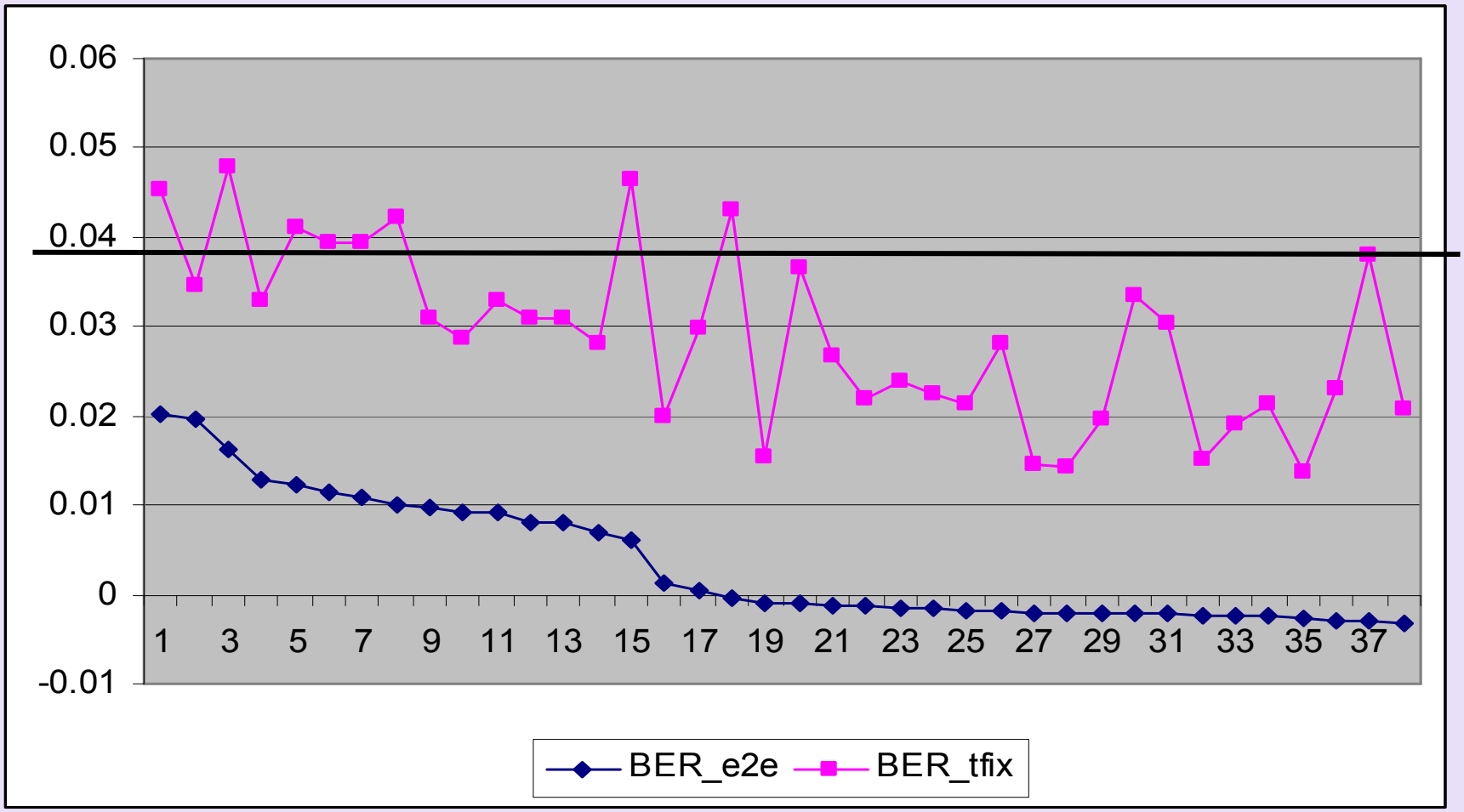
Text fixture with SMP Connectors to 'scope (CLB 3.0)

Statistically significant number of MB Descriptions (same as E2E simulations)



Preliminary Client Simulation Results

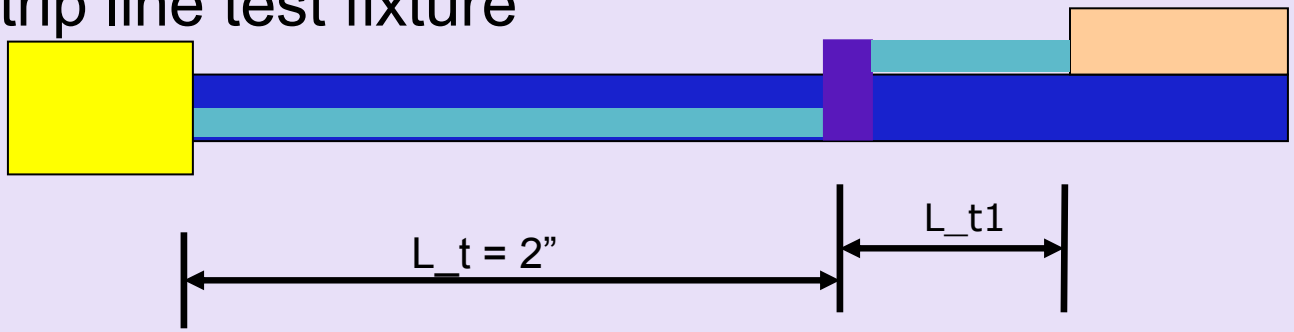
Simple Test Fixture (2” trace – 50 ohm terminations)

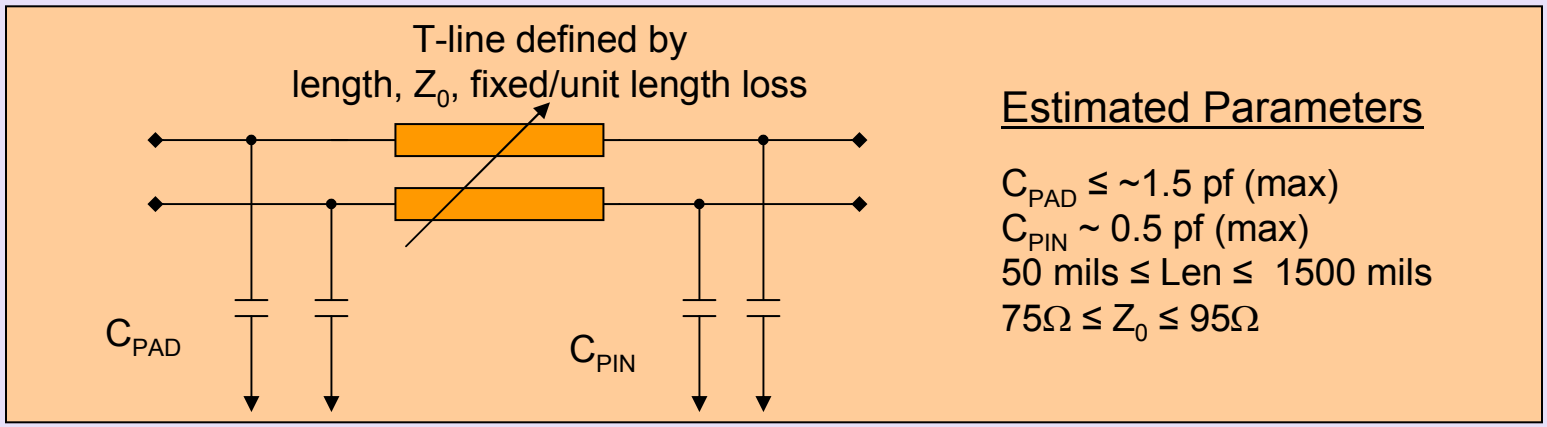


No False Failure Line

Package Test Fixture Topology

- 2” Strip line test fixture

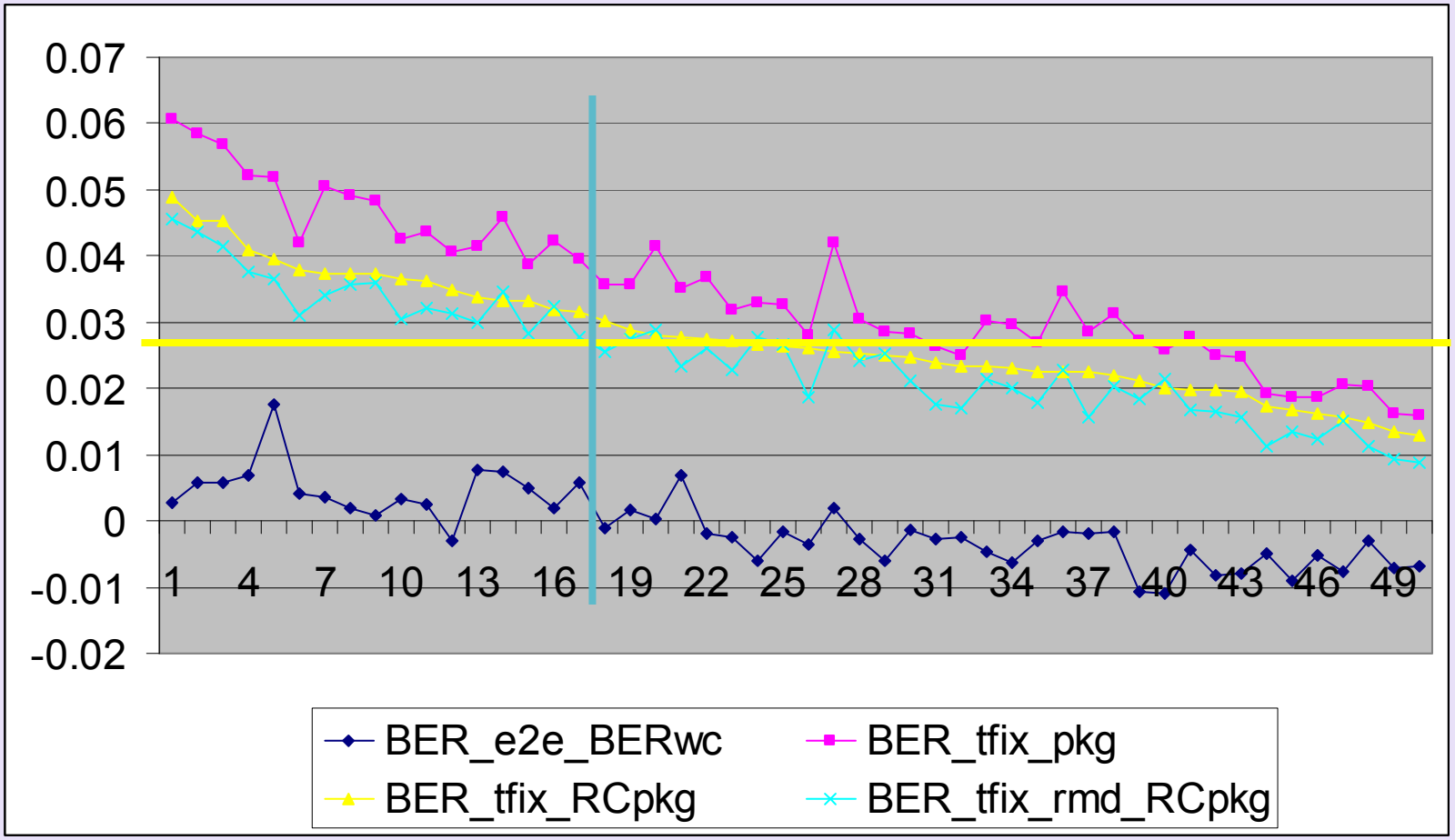




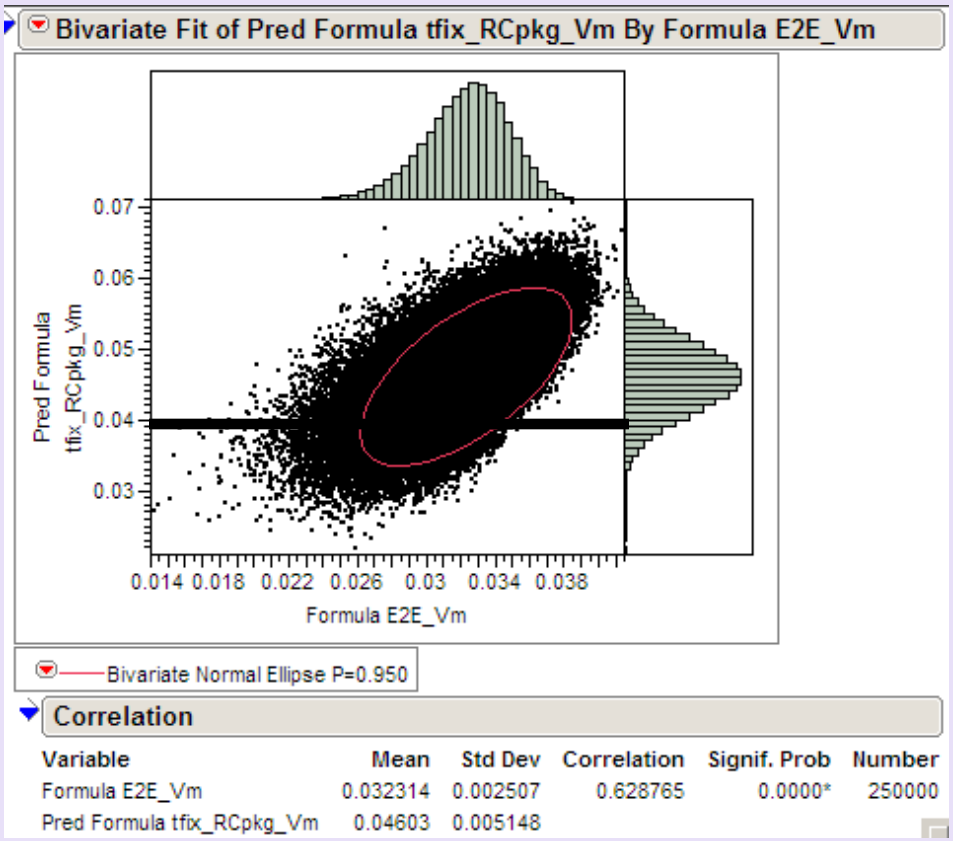
- Varying parameters {Cpad, Cpin, Z0} to mimic package behavior in e2e simulation
- WC AIC with the mother board combinations with Rx. to correlate test fixture
- Via on test fixture maybe used to mimic reflection from riser and AIC

Test Fixtures With RC Package Models

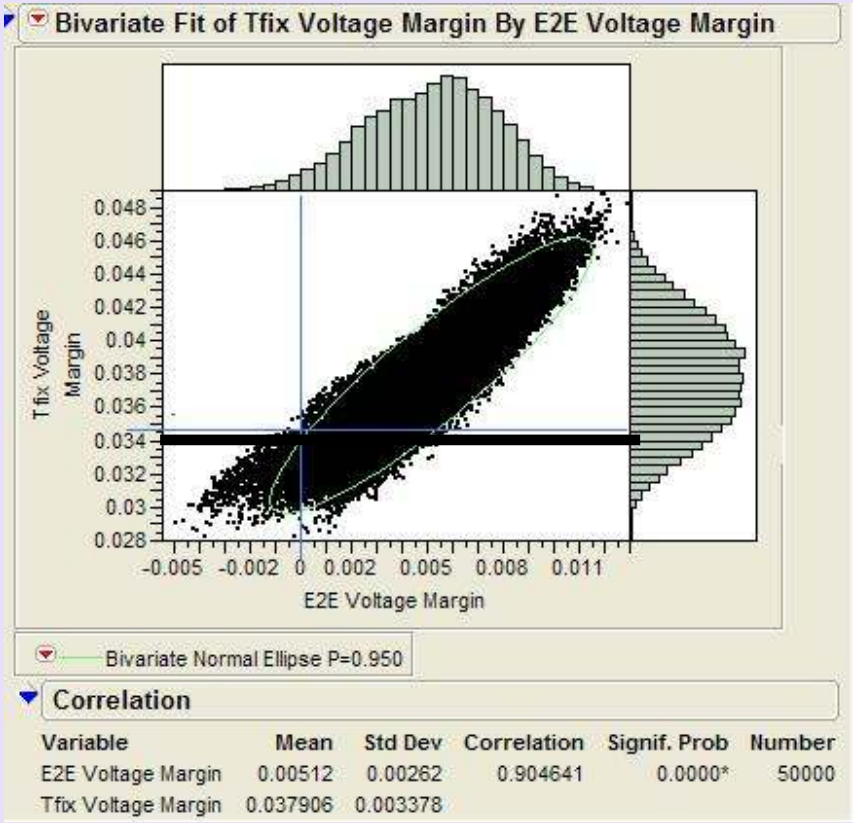
***Same methodology with 50 cases around pass/fail for 2 connector server also gives very close pass/fail numbers**



Package Model Test Fixture Performance With Product Design Targets



Client MB up to 11”



2 Connector Server up to 16”

Standard test fixture with eye specification can work for PCI Express* 3.0 form factors without eliminating target solution space

Summary/Conclusion

- 8GT/s with scrambling meets solution space for channels of interest
- 8.0 GT/s silicon design for same solution space as PCIe 3.0 is challenging but achievable with several optimizations
  - ✓ Higher CDR bandwidth (10 MHz target)
  - ✓ Optimized PLL bandwidth
  - ✓ Receiver equalization (first order CTLE or better)
  - ✓ Transmitter equalization
  - ✓ Statistical simulation tools
- PCIe 3.0 CEM electrical requirements can be specified as a simple eye diagram measured with a standard test fixture.
- For latest PCIe 3.0 specifications, visit www.pcisig.com
  - ✓ .5 PCIe 3.0 and .3 CEM specifications available for member review soon

Thank you for attending the PCIe Technology Seminar

For more information please go to www.pcisig.com