



**PCI**

**SIG<sup>®</sup>**

The logo features the text "PCI" in a bold, italicized, black sans-serif font. A stylized blue swoosh, resembling a ribbon or a wing, curves from the right side of "PCI" down and to the left, passing behind the word "SIG". The word "SIG" is also in a bold, italicized, black sans-serif font, followed by a registered trademark symbol (®). The entire logo is set against a dark blue background with a bright, glowing light source on the right, creating a lens flare effect.



# PCIe<sup>®</sup> 2.0 Cards and Slots

Yun Ling  
Intel Corporation



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# Agenda

- **Areas of Change From 1.1 CEM Specification**
- **Form Factor vs Base Specification**
- Deriving CEM Eye Diagrams From Base Spec
- Specific CEM Test Cases
  - ✓ Motherboard TX, Clock, RX
  - ✓ Add In Card TX, RX
- Card Interoperability and Misc Mechanical Changes
- 225/300 Watt High Power CEM Spec
- Summary

# PCIe<sup>®</sup> 1.x to PCIe 2.0 CEM Changes

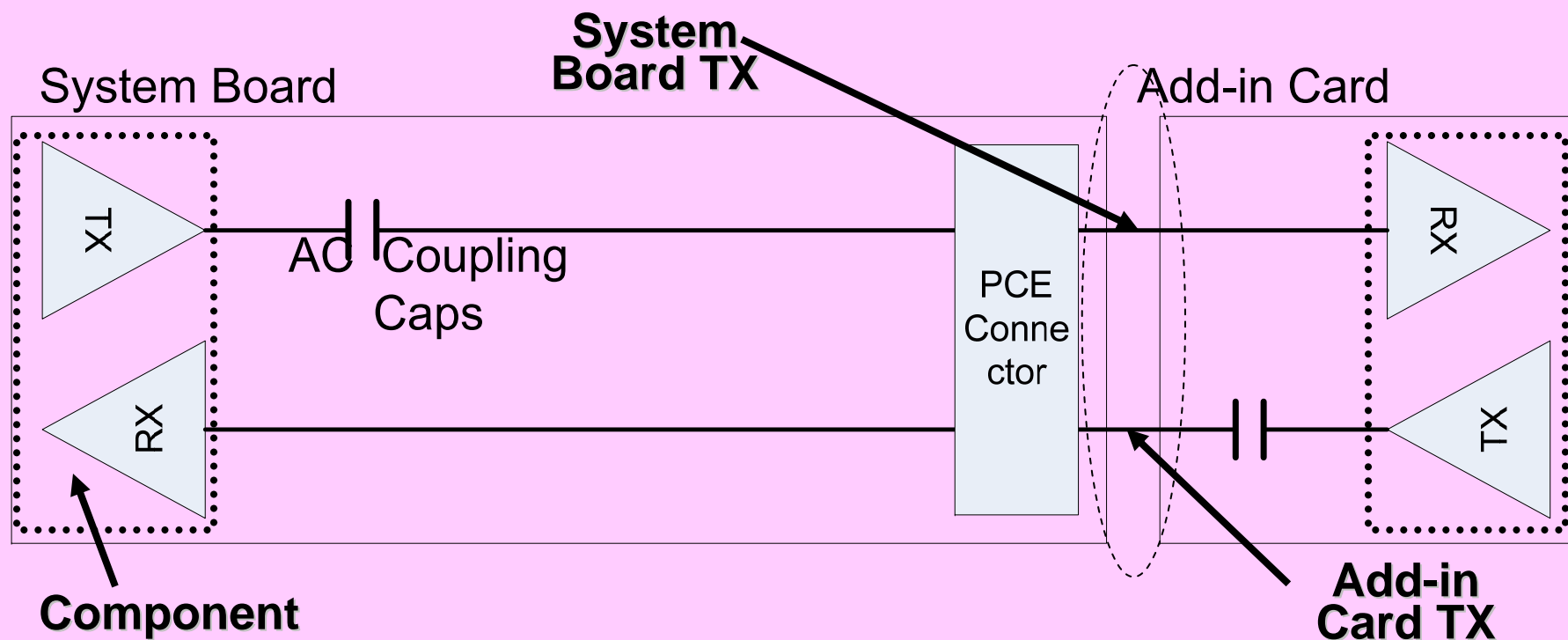
PCIe 1.1 CEM Spec Section	Areas Of Change
Auxiliary Signals	Reference Clock (Jitter)
Hot Insertion And Removal	None
Electrical Requirements	Electrical Budgets Eye Diagrams PCB Trace Impedance (85 Ohms)
Connector Specification	Signal Integrity Requirements and Test Procedures
Add-in Card Form Factors And Implementation	Card Interoperability

**No Required Mechanical Changes From 1.1 CEM Spec**

# PCI Express® 2.0 Base Spec

- Base spec attempts to guarantee interop for components
  - ✓ Transmitter, Receiver, Refclk, Channel
- All parameters referenced to pin location
  - ✓ Only location with guaranteed accessibility
- Each component is characterized in isolation
  - ✓ Tx: Test coupon with “Ideal” refclk
  - ✓ Rx: Calibration channel and pattern generator
  - ✓ Refclk: Test channel into capacitive load
  - ✓ Channel: s-parameter model convolved with W/C Tx behavioral model
- Methodology evolved to specify individual PCIe components without dependencies

# CEM Spec – TX Path



**CEM Spec Defines TX Requirements for Chip + Interconnect  
No Separate TX Chip Or Interconnect Only Requirements.**

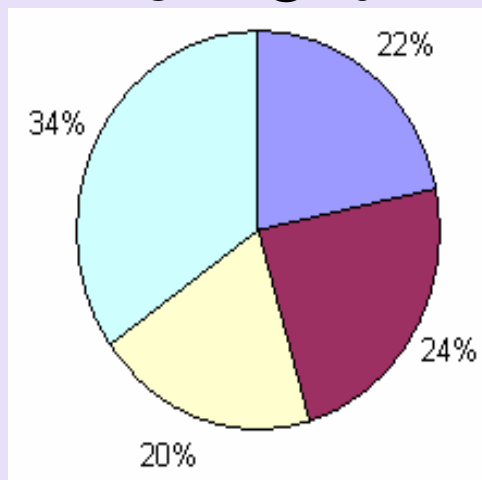


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# CEM Budgets and Topologies

1.1 CEM @ 10<sup>-12</sup>

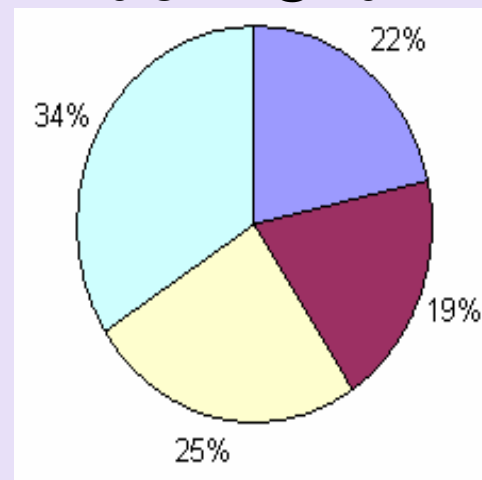


**Relative budget percentages unchanged between 2.5 and 5.0 GT/s. Overall budget half the size.**

■ TX  
■ Clock  
■ Channel  
■ RX

$$T_J = \sum D_J + \sqrt{\sum R_J^2} \leq 400 \text{ ps}$$

2.0 CEM @ 10<sup>-12</sup>



$$T_J = \sum D_J + \sqrt{\sum R_J^2} \leq 200 \text{ ps}$$

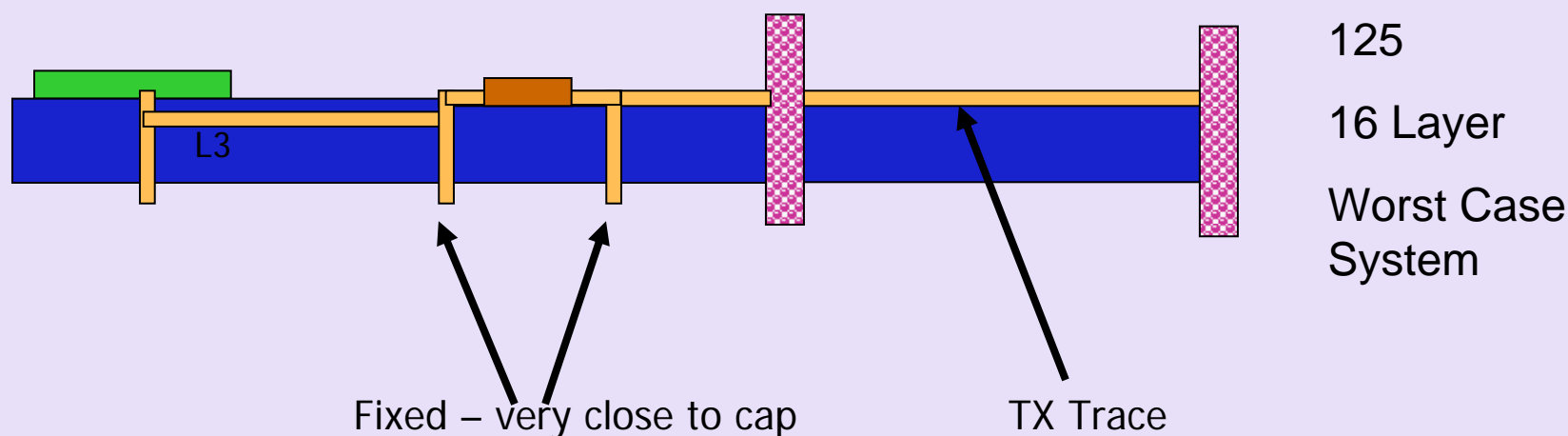
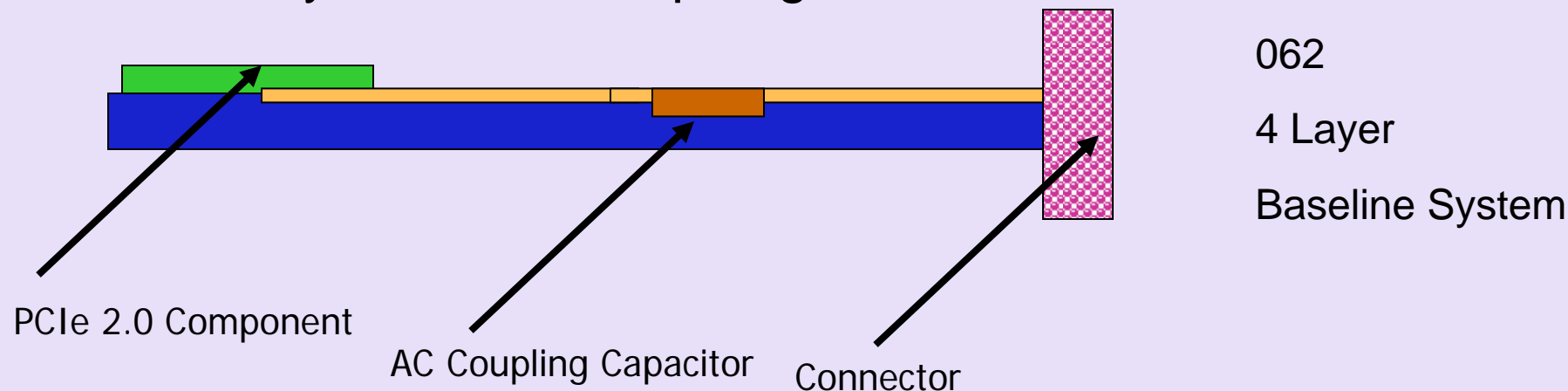
	2.5G – One Connector	2.5G – Two Connector	5G – One connector	5G – Two Connector
<b>Channel Impedance</b>	100Ω	100Ω	85Ω	85Ω
<b>Trace Type</b>	Microstrip	Microstrip	Microstrip	Stripline
<b>MB Length</b>	12"+	16"+	N/A – 100Ω 6-8" – 85Ω	N/A – 100Ω 16" – 85Ω

**CEM 2.0 Requires 85 ohm Nominal Differential Trace Impedance**



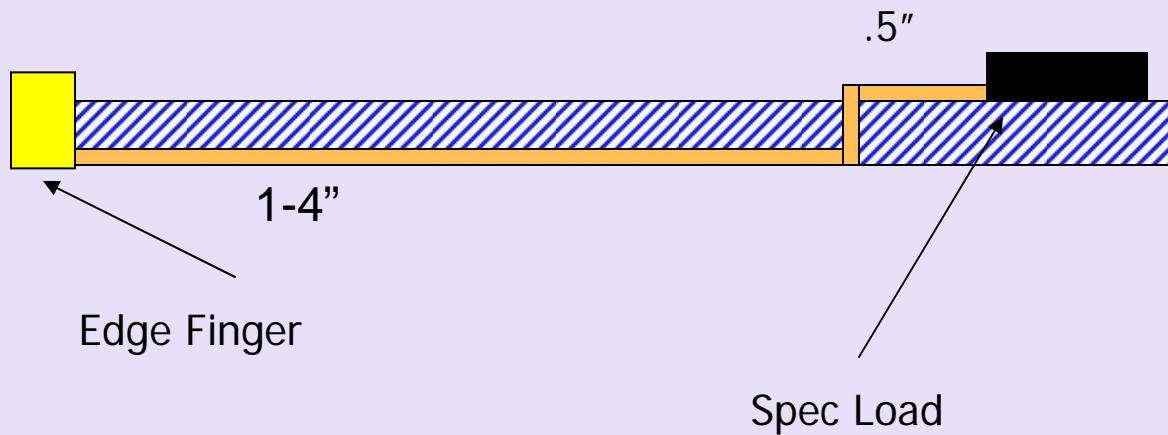
# Deriving CEM Eye Diagrams From Base Spec - System Board TX Eye Methodology

- Select system board topologies



# Deriving CEM Eye Diagrams From Base Spec - System Board TX Eye Methodology

- Select add-in card topologies



062

4 Layer

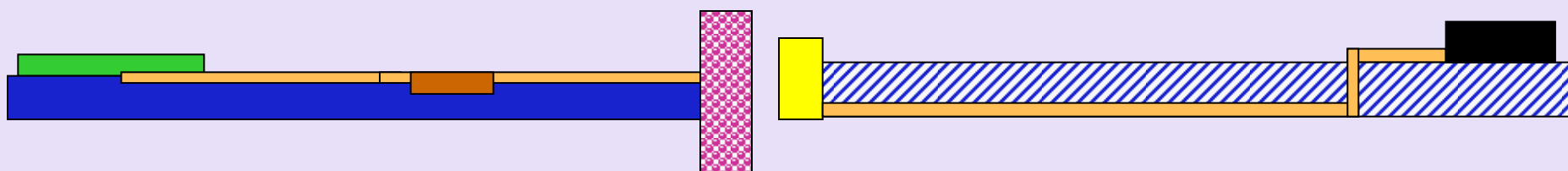
Worst Case AIC

# Simulation Parameters

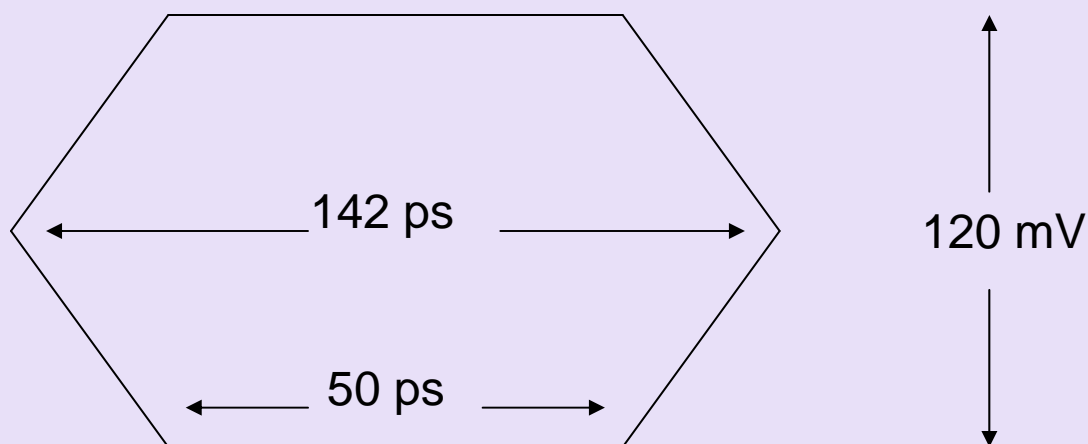
- Motherboard channel parameters and variations
  - 85 Ohm +/- 22% (Desktop)
  - Trace Length (Desktop)
    - 3-6", 6-10", ~.5" Breakout
  - Microstrip
    - 5-7-5-15 85 Ohms, 4-8-4-15 100 Ohms, 4-4-4-8 Breakout
  - Lab Measured Connector Model
- Vary Add-in Card parameters (Reasonable range)
  - 85 Ohm +/- 17.5%
  - Microstrip
    - 5-7-5-15 85 Ohms, 4-8-4-15 100 Ohms, 4-4-4-8 Breakout (~.5")
  - Spec Load (50 Ohm terminations).
- Behavioral Tx model parameters and variations (Per Base Specification)
  - 800 mV Min Swing into 50 Ohm terminations
  - Deemphasis 3 – 6.5 dB
    - No Jitter Derating
  - Spec Package Model
    - 1pf, 80-120 ohms

# System Board TX Eye Methodology

- Simulate end to end eye diagrams

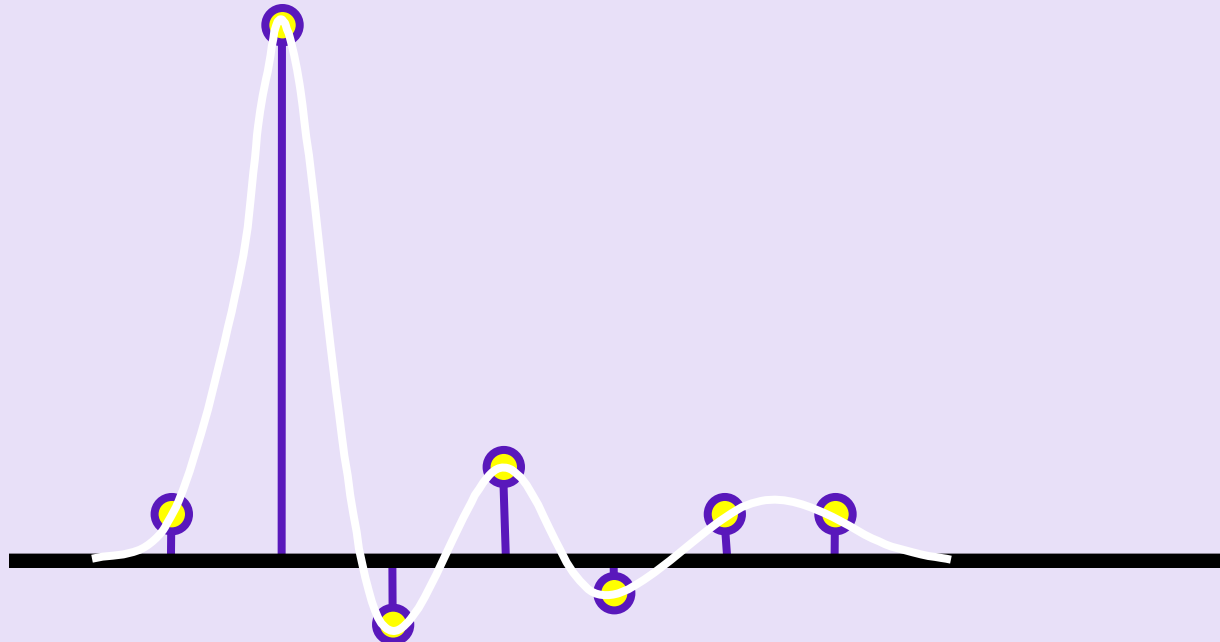


- Identify all end to end failures (worst case pattern)
  - 120 mVolt Eye Height (Base Spec Rx Pin Limit)
  - 142 ps Eye Width (Interconnect only) (Base Spec Channel Limit)



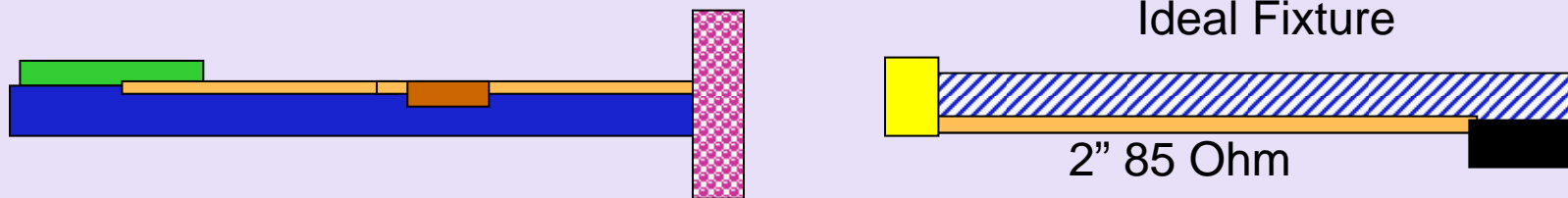
# Worst Case Patterns

- Peak Distortion Analysis
  - ✓ Deterministically Calculates Worst Case Patterns Given
    - Channel S Parameters
    - Pulse Response
  - ✓ Used For Simulation Data In This Presentation
- Differences From Pseudo Random or CMM Patterns Can Be Very Large (~ 30 ps eye width)



# System Board TX Eye Methodology

- Simulate end to connector eye diagrams

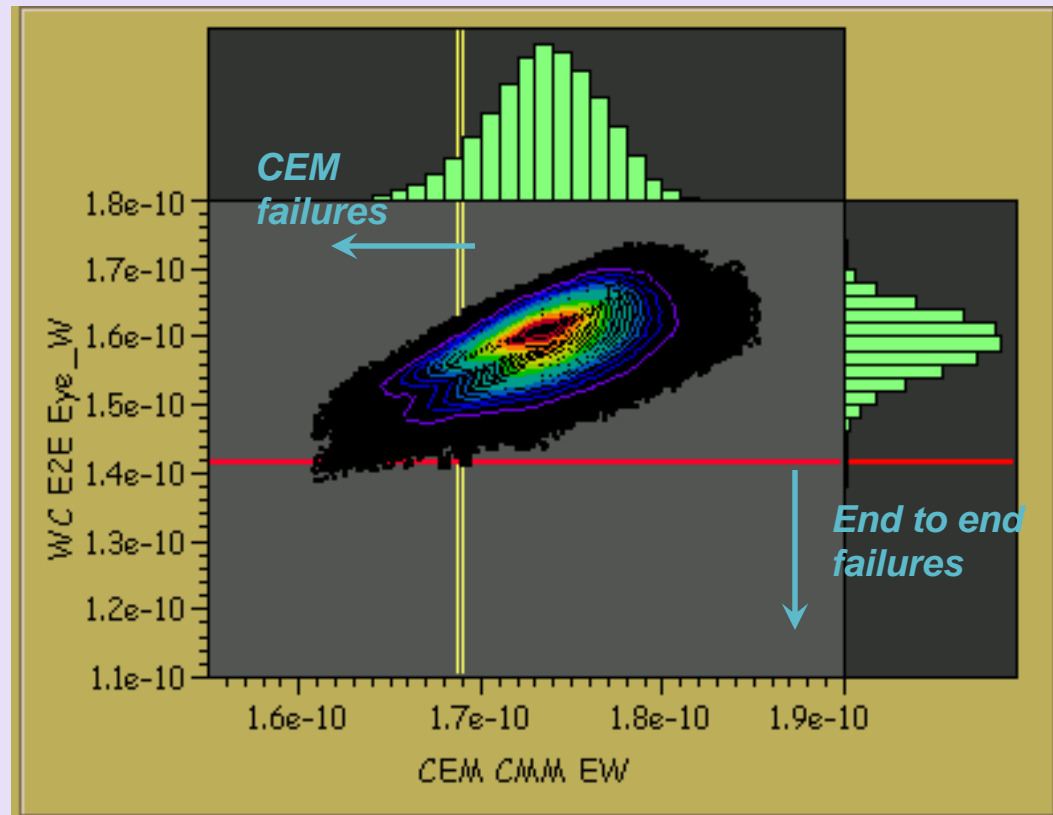


- Use CMM pattern as with real world test
- Correlate with end to end worst case pattern failures
- CEM eye specifications include ideal fixture
  - ✓ No need to de-embed if similar fixture used.



# Simulation Methodology

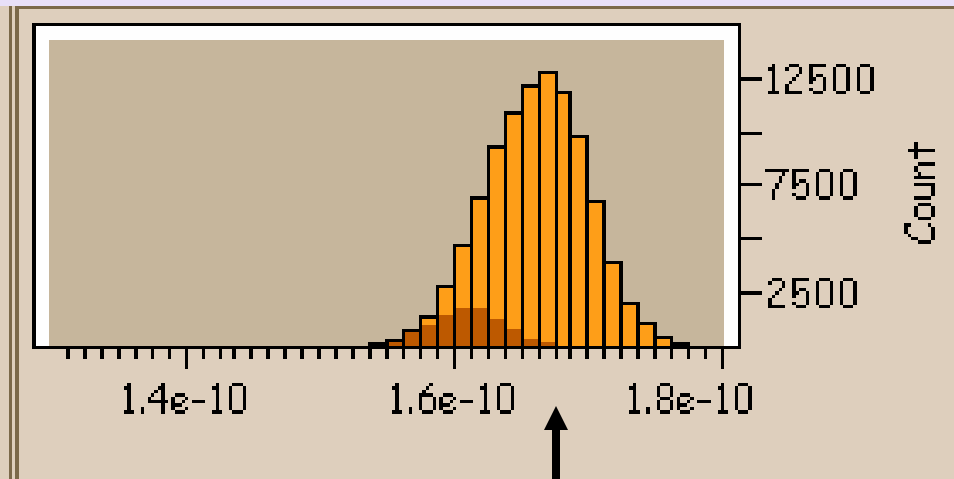
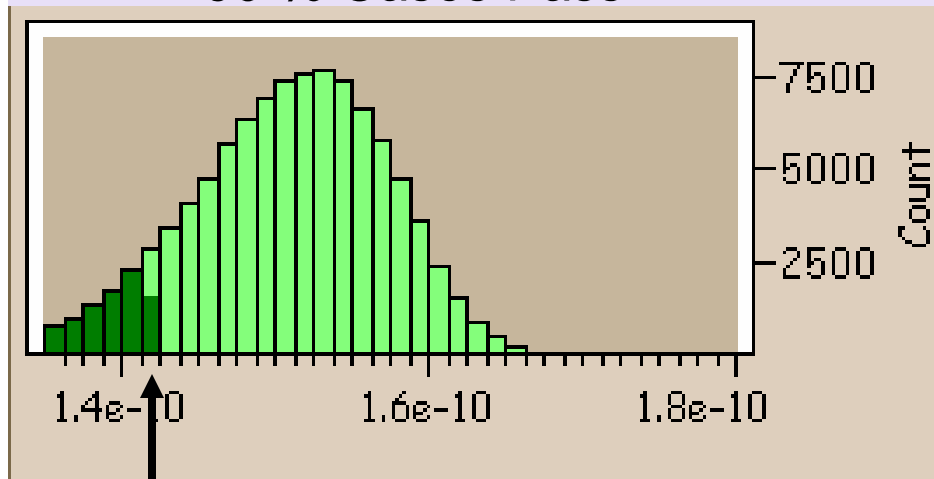
- The resultant eyes of the End to End and CEM simulations are plotted against each other for a large number of cases
- A Horizontal line is drawn with respect to the End to End eye to signify insufficient opening in the system
- A Vertical line is drawn such that no End to end failures are to the right
- Instances in the lower right quadrant would indicate End to End failures not screened out by CEM
- Instances in the upper left quadrant are cases which work End to End, but are screened out by the CEM\*



# Results – 3-6” 6 dB, 85 Ohms

End to End Eye Width  
90 % Cases Pass

Connector CMM Eye Width  
15% Cases Pass



Pass

142 ps

Fail

Fail

Pass

170 ps

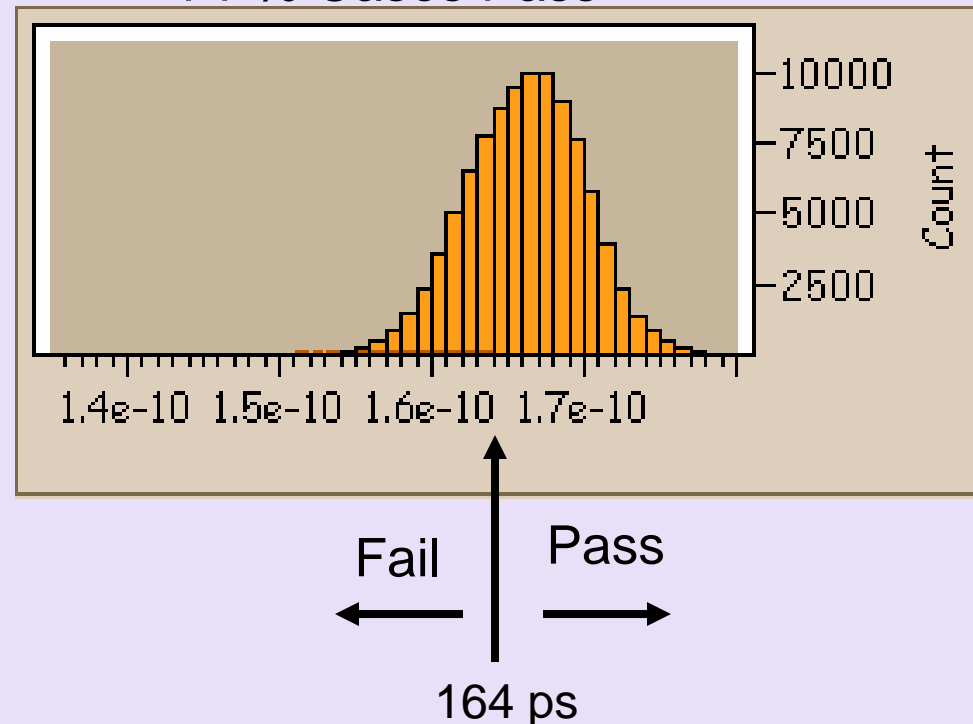
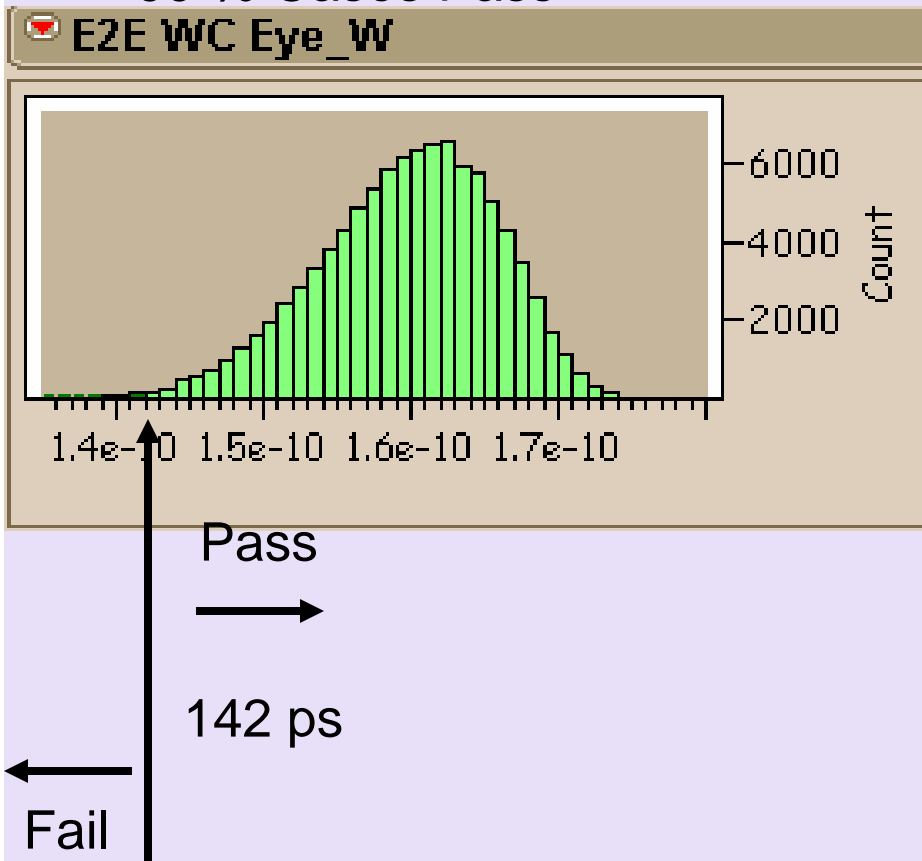
Identify eye diagram at the connector that catches all end to end failures.

6 dB CEM eye eliminates most solution space for client topology.

# Results – 3-6” 3.5 dB, 85 Ohms

End to End Eye Width  
99 % Cases Pass

Connector CMM Eye Width  
71 % Cases Pass



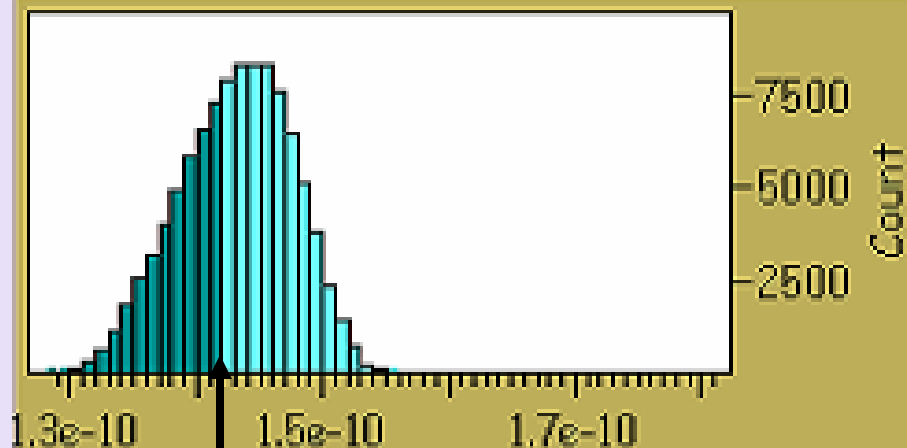
3.5 DB CEM eye catches all end to end failures and allows reasonable solution space for simple client motherboard topology.

## Results – 6-10” 6 dB 100 Ohm Impedance

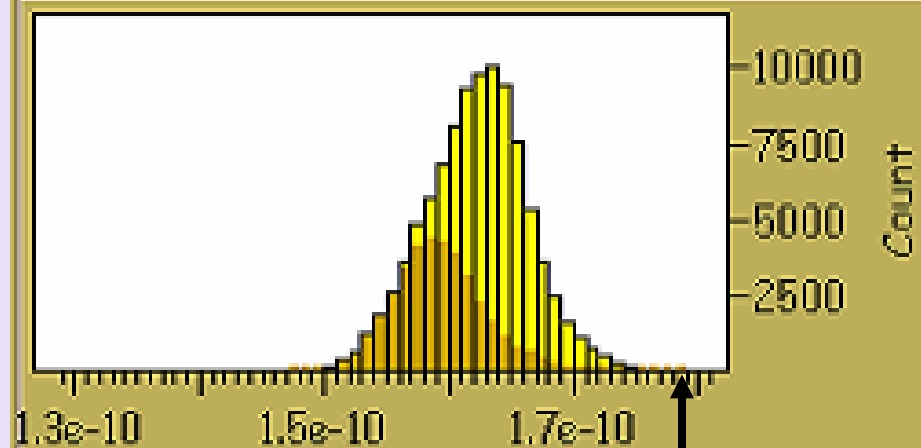
End to End Eye Width

Connector CMM Eye Width  
~ 0% Passing Cases

100 E2e WC Eye\_W



100 Midbus CMM EW

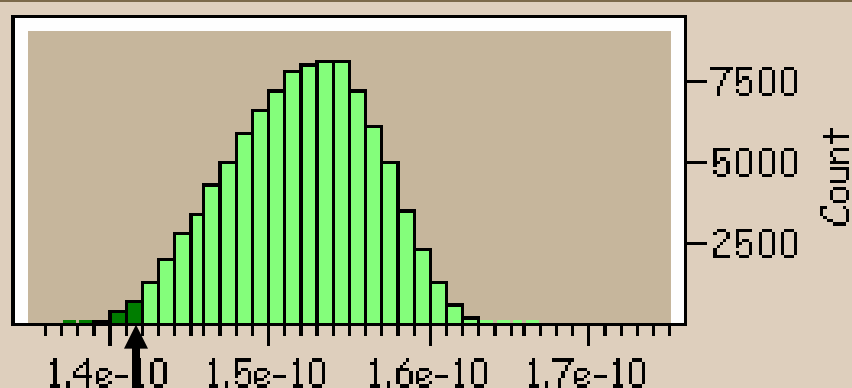


CEM Eye required to catch all end to end failures eliminates almost all solution space if nominal trace impedance is 100 Ohms

# Results – 6-10" 6 dB 85 Ohm Impedance

End to End Eye Width  
99 % Cases Pass

❑ E2E WC Eye\_W



Pass

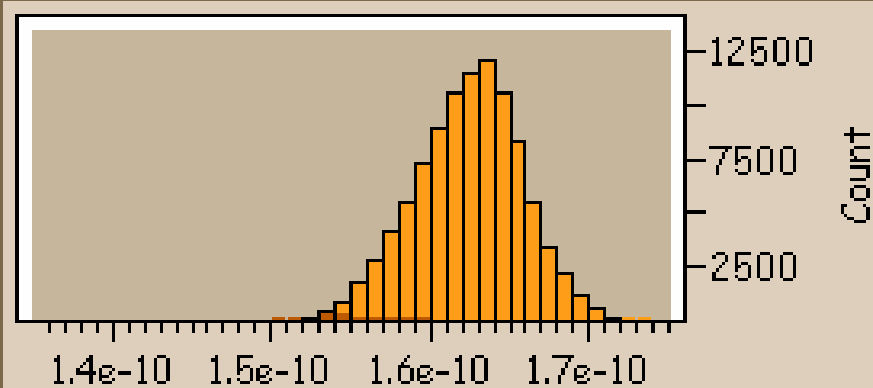


142 ps

Fail

Connector CMM Eye Width  
83% Cases Pass

❑ Midbus CMM EW



Fail



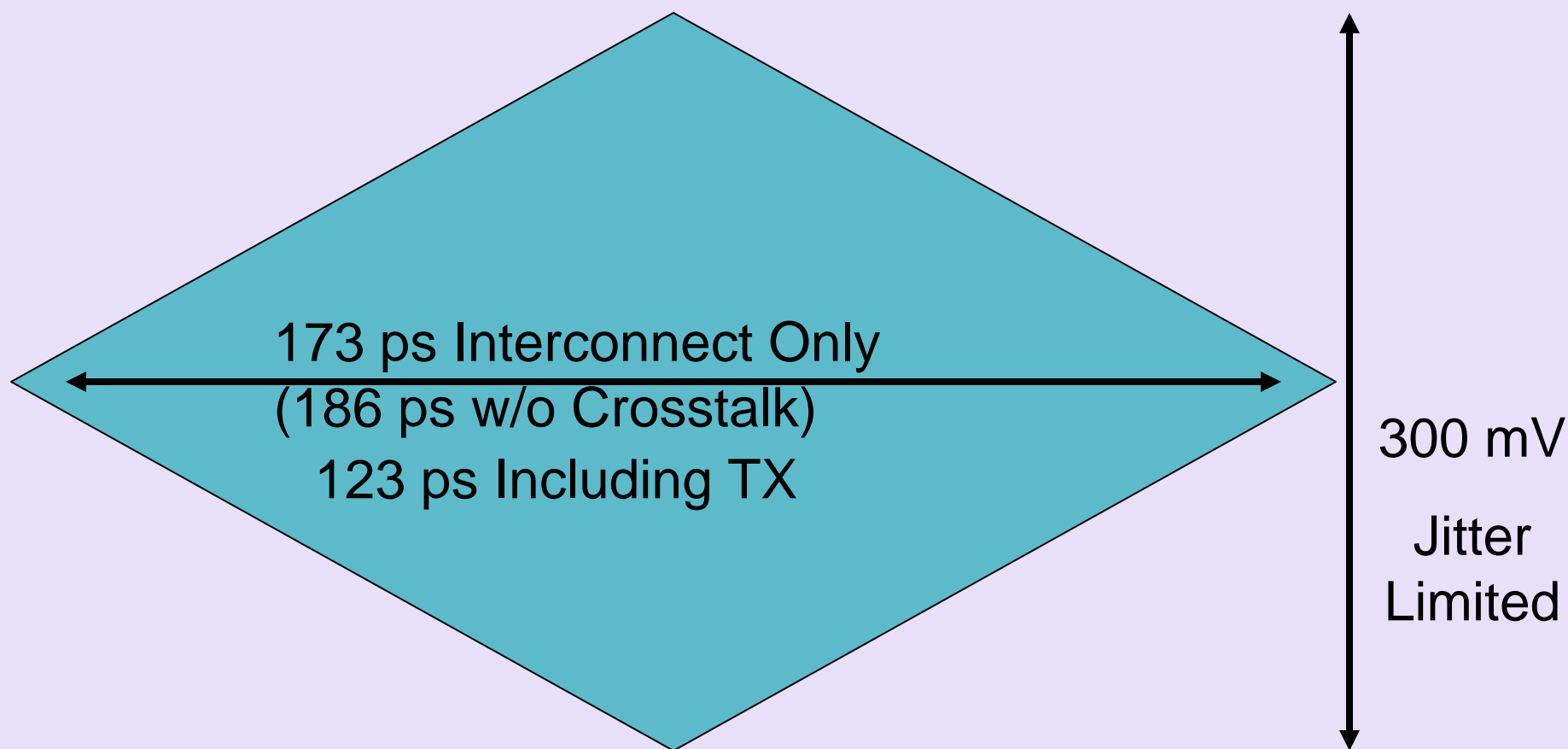
Pass



159 ps

CEM eye catches all failures and still allows reasonable solution space.

# MB TX Eye Tx + Interconnect (FYI Only)



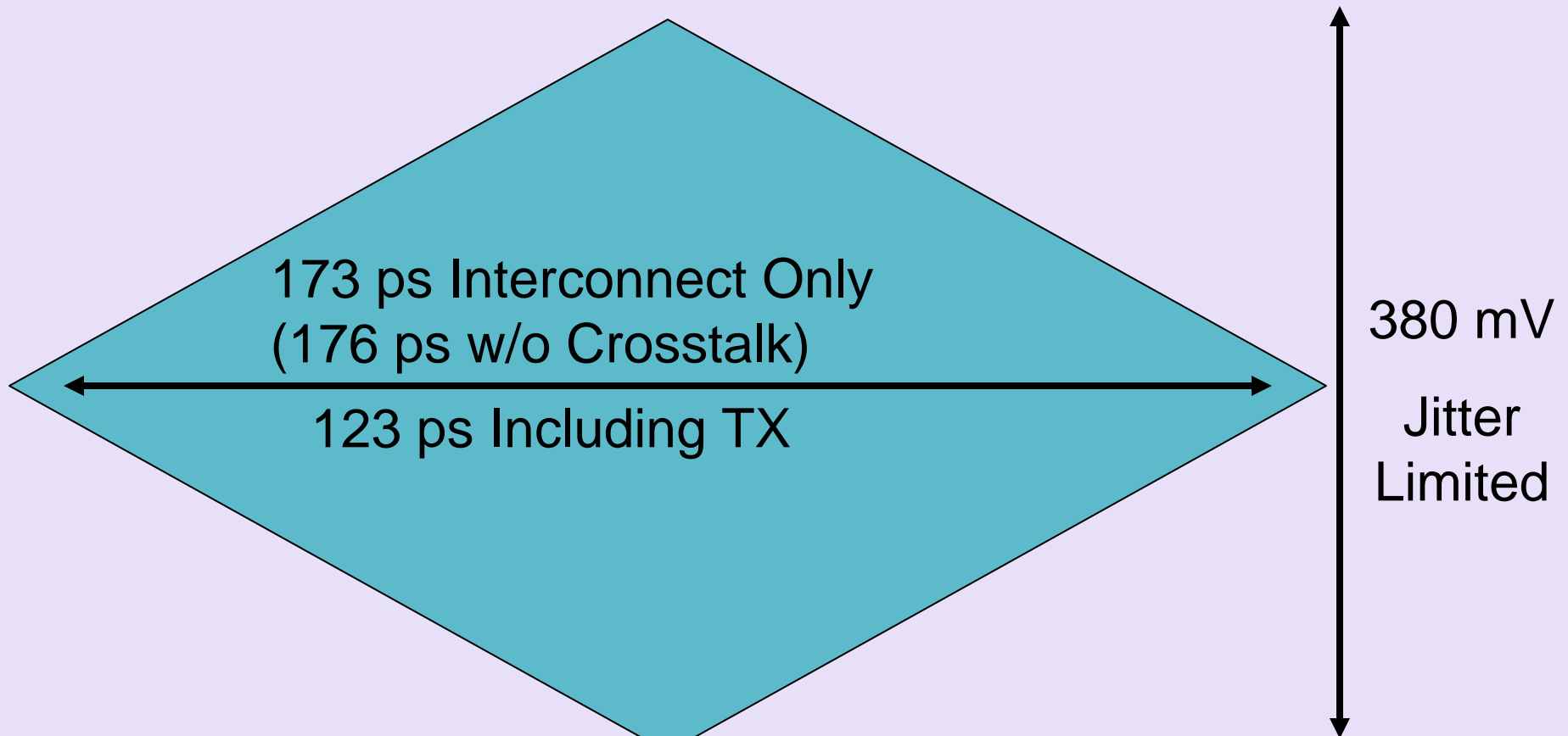
Eye methodology works and allows 6-10" motherboard high volume solution space with 85 ohm impedance target.



# CEM Add-in Card TX Eye Methodology

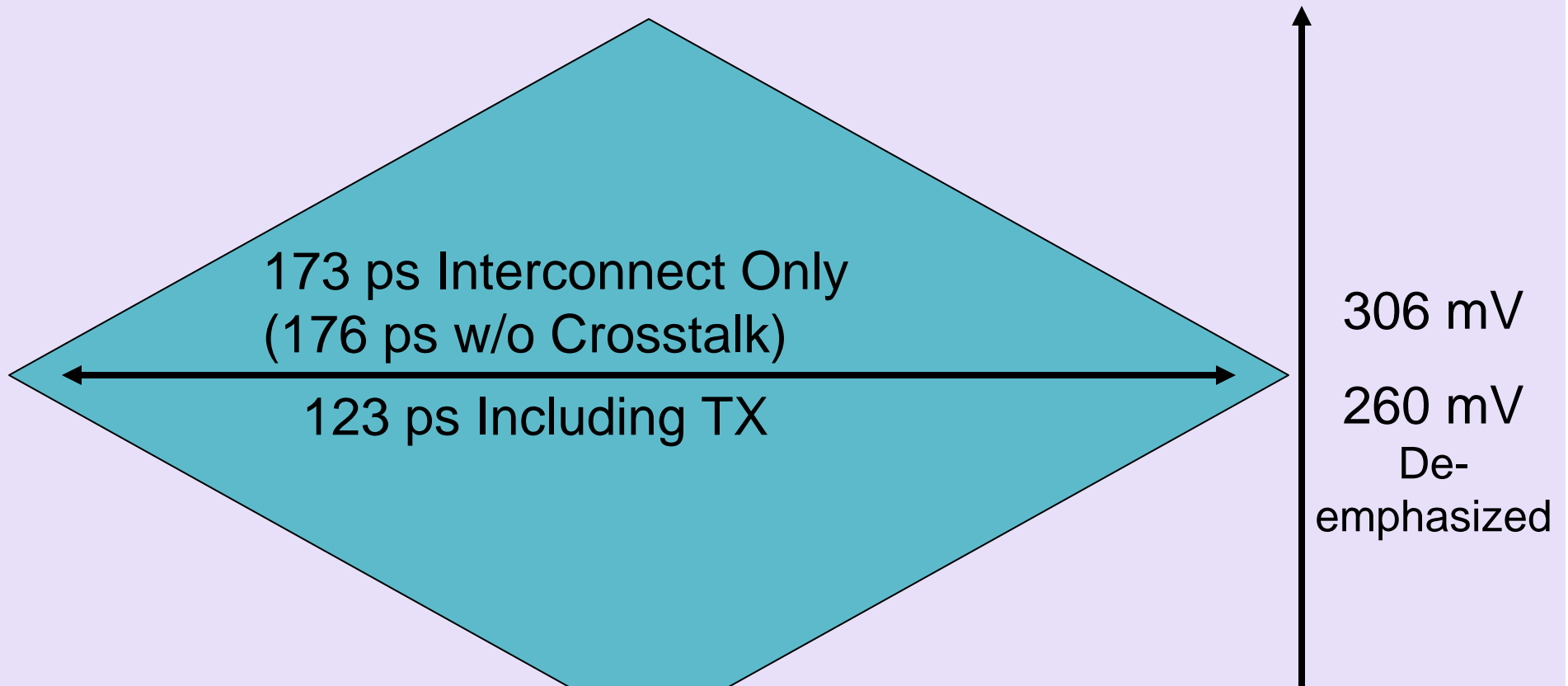
- Select Add-in card topologies
  - ✓ Vary parameters slightly outside of reasonable ranges
- Select system board topologies
  - ✓ Vary parameters only through reasonable ranges
- Simulate end to end worst case eye diagrams  
Simulate end to edge finger worst case eye diagrams
- Identify all end to end failures
- Identify eye diagram at edge finger that fails all cases that fail end to end

# AIC TX Eye – 3.5 dB



Eye methodology works and allows ~4" add-in card high volume solution space with 85 ohm impedance target.

# AIC TX Eye – 6.0 dB

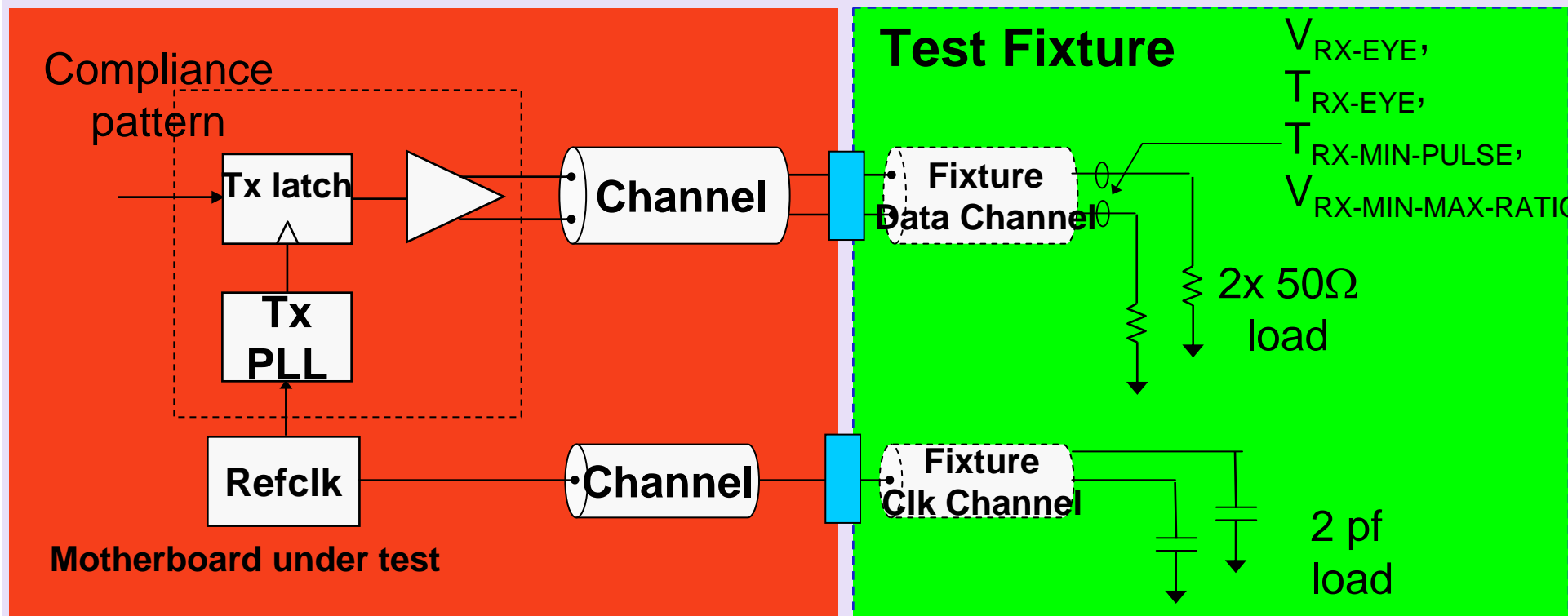


Add-in Card Eye Diagrams include fixture  
Standard connector with 3" 85 ohm traces

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# Testing Transmitter on Motherboard



- Data and Refclk Output Tested At Connector
- Refclk margins same as those defined in base spec
- How do you test transmitter jitter on a motherboard with a real clock?
  - ✓ Ref clock jitter appears on transmitter up to transmitter PLL bandwidth

# Dual-Port Approach

- Sample TX and Clock Simultaneously at MB Connector
- Low Pass Filter Clock with PLL Limits
  - ✓ 5 MHz 1 dB Peaking
  - ✓ 8 MHz 3 dB Peaking
  - ✓ 16 MHz 3 dB Peaking
- Add Transport Delay. Max ~ 3ns for Add-in Card.
- Use Filtered Clock To Calculate TX Jitter With Each Filtered Clock Record
- Apply 1.5 MHz High Pass Step Function
- Select Largest TX+Interconnect+Clock Jitter Val

Real System PLL Factored Into Measurement  
Real System Delay Factored Into Measurement  
Random Jitter From RefClk and TX RSS Together

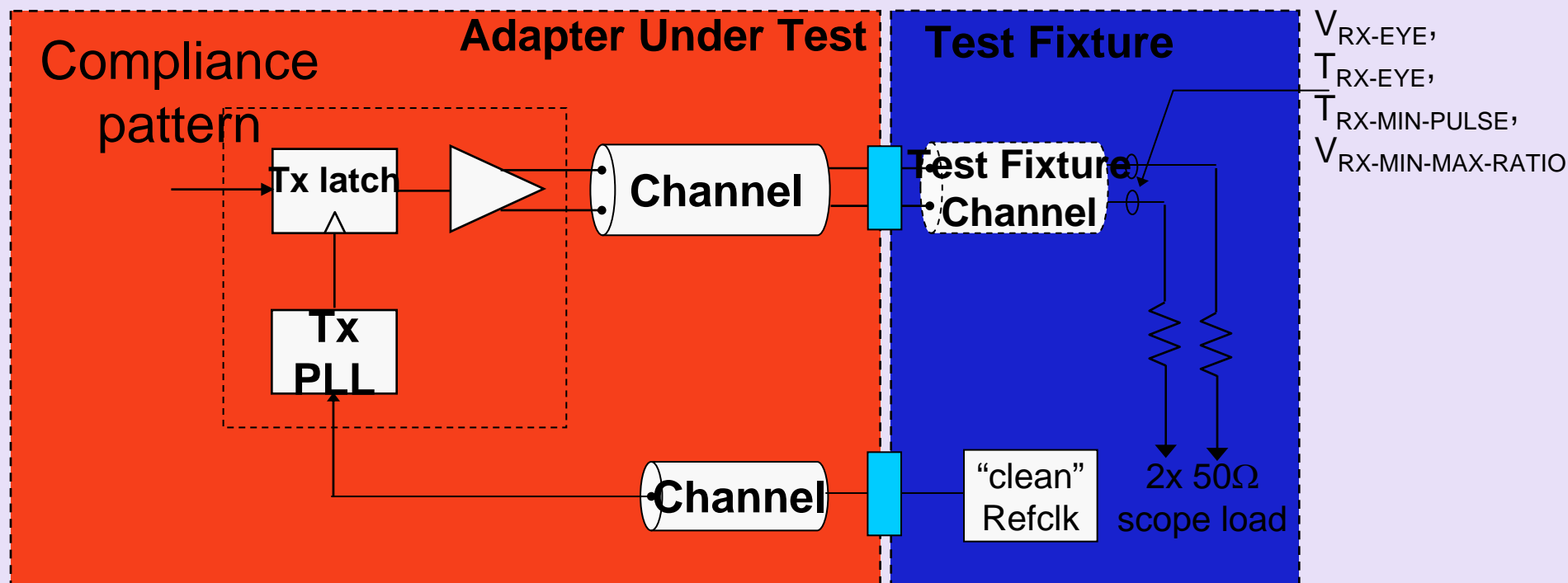


# Jitter Limits w/ Dual-Port Method

	Max Dj (ps)	Max TJ @ E-12 BER (ps)
With Crosstalk	57	105
W/O Crosstalk	44	92

- TX and Clock Limits
  - ✓ TX      30 ps Dj      50 ps TJ @ E-12
  - ✓ Clock    43.6 ps TJ @ E-12. Dj Limit is 0
- TX + Clock Limit (worst case)
  - ✓ = 30 ps Dj + 20 ps Rj + 43.6 ps Rj
  - ✓ = 30 ps Dj +  $\sqrt{20^2 + 43.6^2}$  = 78 ps Tj @ E-12 BER
- Interconnect Limit
  - ✓ 27 ps Dj with Crosstalk, 14 ps Dj without Crosstalk

# Testing Transmitter on an Adapter



- Test topology similar to that defined in base spec
- Test adapter furnishes a "clean" Refclk
  - Same post processing as used for base spec

# Receiver Test Eye Diagrams

- Receiver test eye diagrams defined using ideal Add-in card (Compliance Base Board) and System board (Compliance Load Board) test fixtures.
- Test Add-in Card
  - ✓ Connect both test fixtures.
  - ✓ Inject signal into RX lanes of compliance base board
  - ✓ Measure signal at RX output of compliance load board.
  - ✓ Calibrate eye to match system board TX limits.
  - ✓ Remove compliance load board and insert Add-in card under test.
- Test Motherboard
  - ✓ Connect both test fixtures
  - ✓ Inject signal into RX lanes of compliance load board.
  - ✓ Measure signal at TX output of compliance base board.
  - ✓ Calibrate eye to match AIC TX limits for de-emphasis level used by system board link under test.
  - ✓ Remove compliance base board and insert CLB to motherboard slot to test

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# Card/Slot Interop - New Interoperability Requirements

Connector Card	x1	X4	X8	x16
x1	Required	Required	Required	Required
x4	No	Required	Required	Required
x8	No	No	Required	Required
x16	No	No	No	Required

Table 6-2: Card Interoperability

All PCI Express Add-in Cards must be able to negotiate and operate in all smaller link widths from the full link width down to x1. **x2 and x12 link widths are optional.**

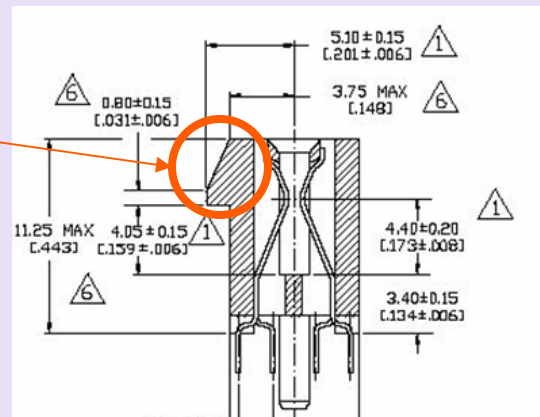
The upstream PCI Express components on a system board must be able to negotiate and operate in all smaller link widths from the full link width down to x1. **x2 and x12 link widths are optional.**

**New For CEM 2.0**

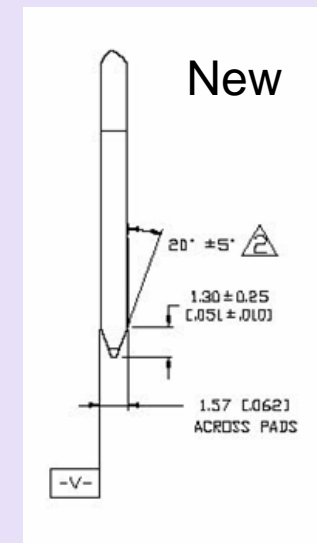
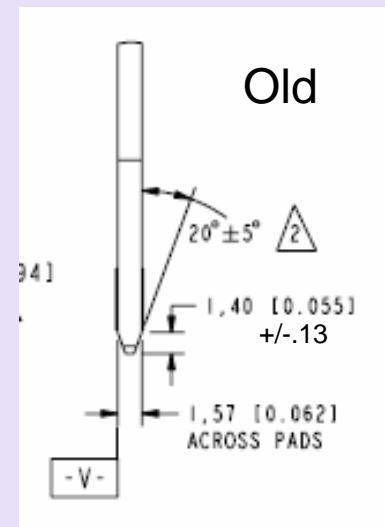
# Misc Mechanical Changes

- Add-in card retention ridge on connector is now optional
  - ✓ Improve connectors yields. Asymmetry made manufacturing more difficult.

Optional



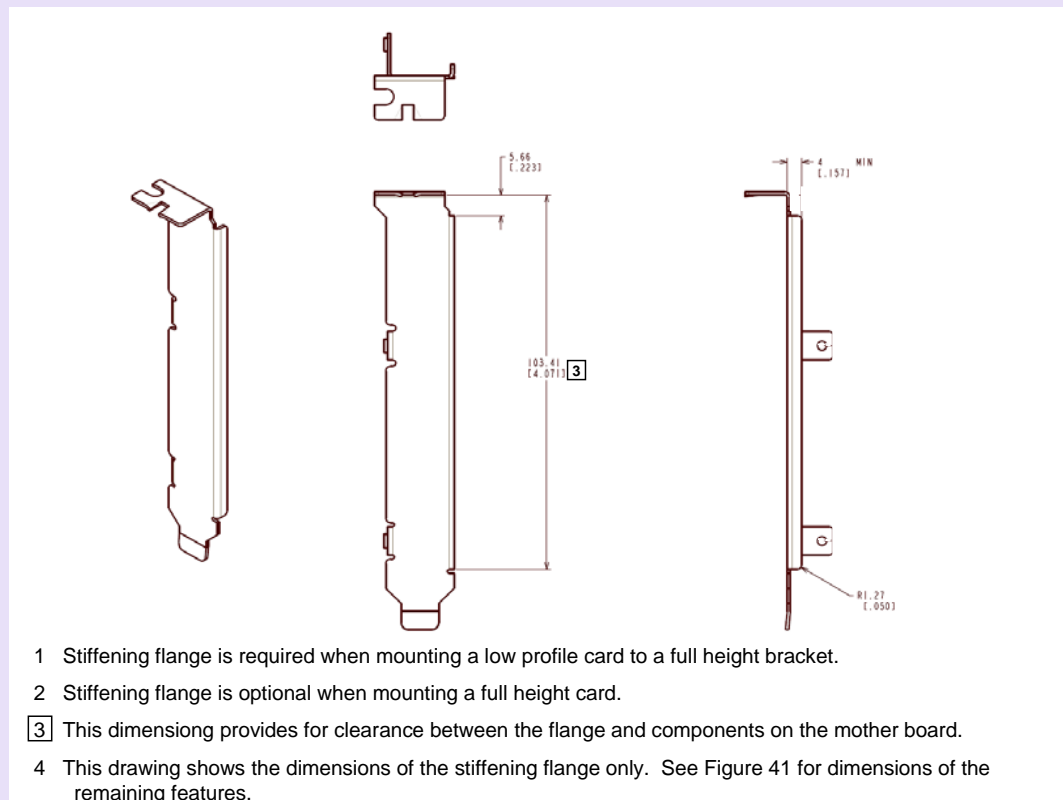
- Add-in card bevel height
  - ✓ Old - .055 +/- 5 mil
  - ✓ New - .051 +/- 10 mil
  - ✓ Improve manufacturing yields.
  - ✓ Old tolerance requirement difficult to meet.





# Full-Height I/O Bracket for Low Profile Card

- Added a stiffener flange requirement for the full-height I/O bracket used with low profile cards



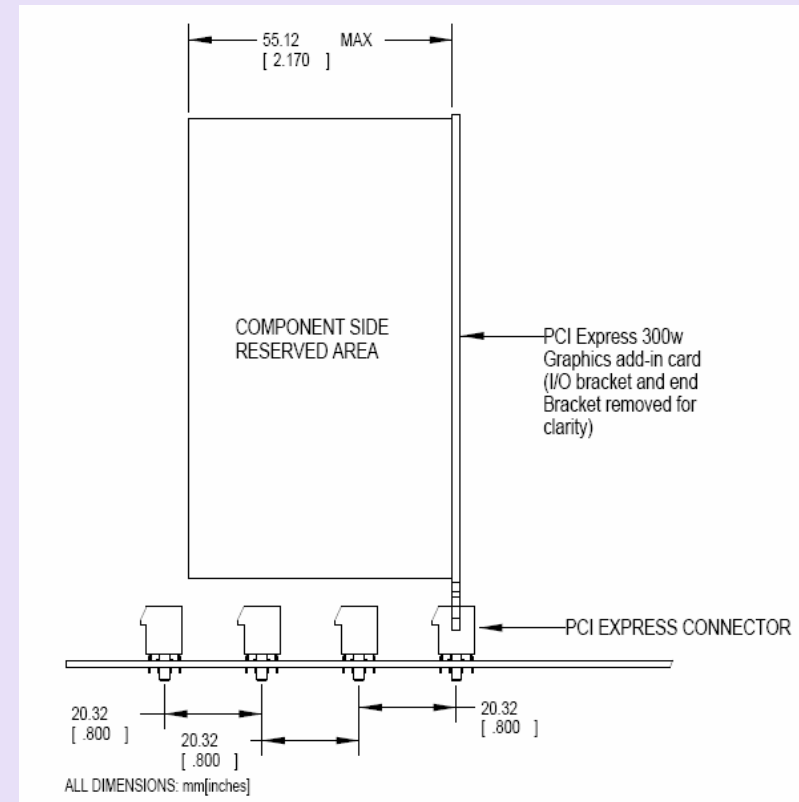
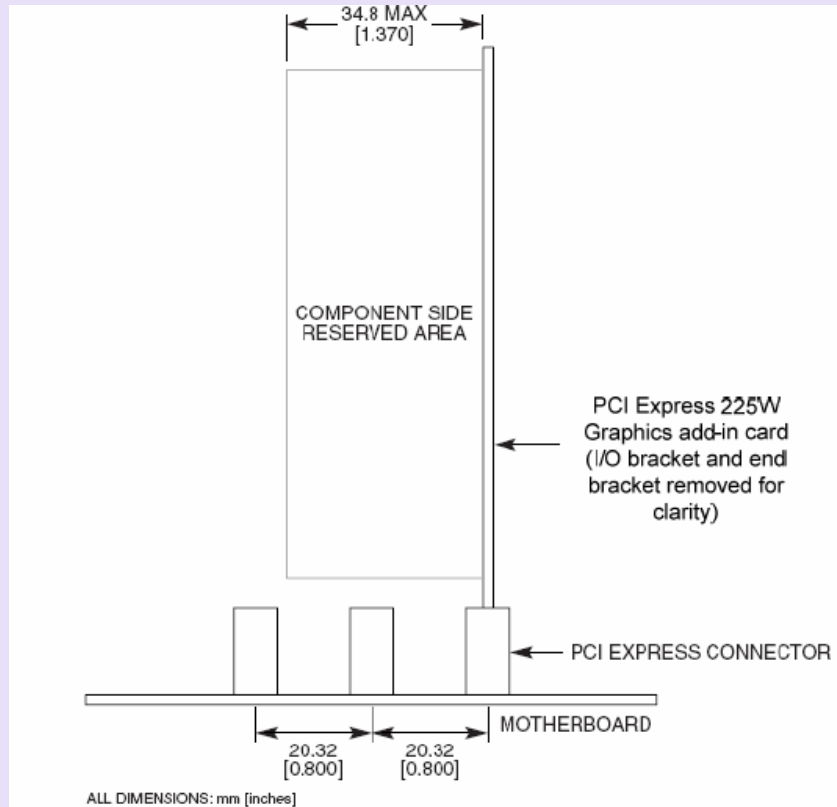
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# 225/300W High Power CEM Spec

- 0.7 spec completed by the CEM Workgroup in July'07
- 0.9 spec will be done in a couple of weeks
- 1.0 spec release targeted for end of 2007
- Spec scope
  - ✓ Support 225 W and 300 W high power requirements for add-in cards and systems
  - ✓ Standardize new power delivery connector and new power-up sequencing scheme
  - ✓ Define interoperability between 225W/300W high power card components [225W and 300W cards have new system boundary conditions that may require improvement to existing chassis form factor and power delivery systems.]
    - PCI-SIG® investigating ATX form factor
    - No intention to preclude BTX form factor

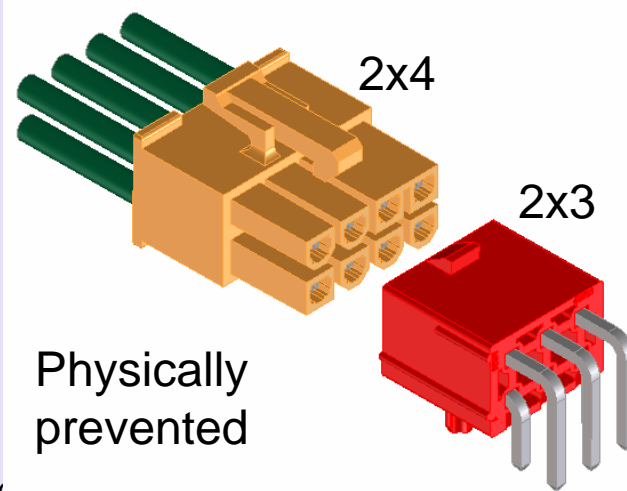
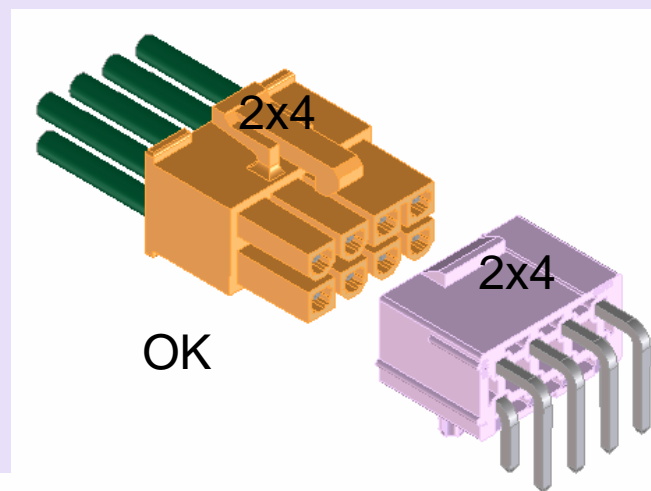
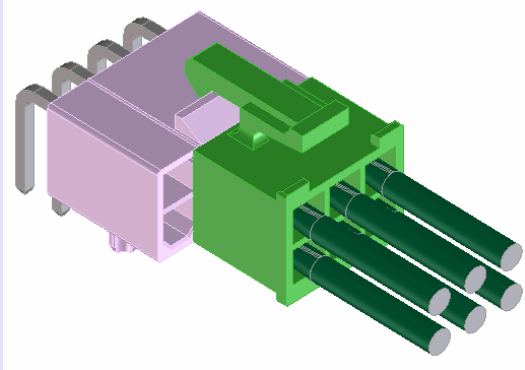
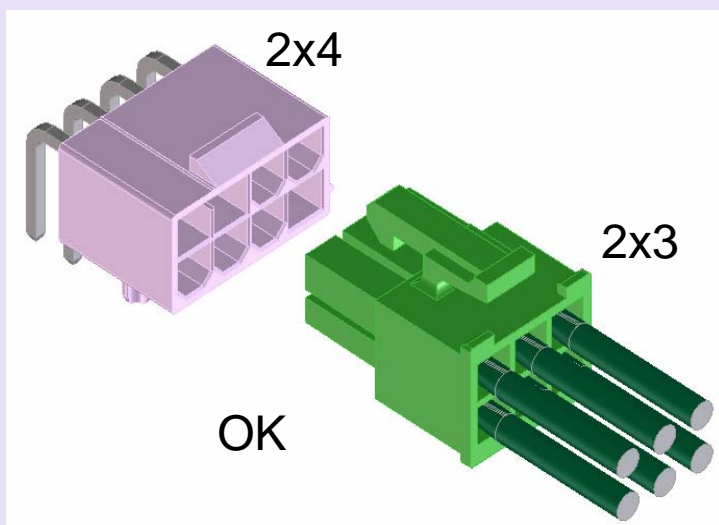
# System Volumetric



(150W-225W] cards can occupy two slots    (225W-300W] cards may occupy three slots

# Auxiliary 2x4 Connector

- Besides the 2x3 connector defined in the 150W Graphics Spec 1.0, a new 2x4 connector is defined for delivering power to the 225/300W cards



# Delivering Power to Cards

- A 300W add-in card can receive power by the following methods:
  - ✓ 75W from x16 PCIe connector plus 150W from a 2x4 connector plus 75W from a 2x3 connector.
  - ✓ 75W from x16 PCIe connector plus 75W from a first 2x3 connector, plus 75W from a second 2x3 connector, plus 75W from a third 2x3 connector. Note that this is not the preferred approach.
- A 225W add-in card can receive power by one of the following methods:
  - ✓ 75W from x16 PCIe connector plus 150W from a 2x4 connector.
  - ✓ 75W from x16 PCIe connector plus 75W from a 2x4 connector plus 75W from a 2x3 connector.
  - ✓ 75W from x16 connector plus 75W from a first 2x3 connector plus 75W from a second 2x3 connector.



# Additional Power Delivery Requirements



- The +12V delivered from the standard x16 edge connector and the additional +12V(s) delivered via the dedicated 2x3 and/or 2x4 auxiliary power connector(s) must be treated as coming from independent separate system power supply rails.
- The different +12V input potentials from different connectors must not be electrically shorted at any point on a PCI Express 225W/300W add-in card.
- The power pins of a single 2x3 or 2x4 auxiliary power connector can be shorted together.
- No specific power sequencing between the slot, 2x3 and 2x4 connector power can be assumed. A PCI Express 225W/300W add-in card must handle all possible combinations.

# Power-up Sequencing

Table 3-1 PCI Express 300W Graphics (with one 2x4 + one 2x3 connectors) permitted initial power draw

2x4 Sense0 Detected?	2x4 Sense1 Detected?	2x3 Sense Detected?	Power draw permitted at system power up
N	N	N	25W available from PCI Express edge connector
N	N	Y	Total of 75W is available: 25W available from PCI Express edge connector 50W available from 2x3 connector
Y	N	N	Total of 75W is available: 25W available from PCI Express edge connector 50W available from 2x4 connector
Y	N	Y	Total of 125W is available: 25W available from PCI Express edge connector 50W available from 2x3 connector 50W available from 2x4 connector
Y	Y	N	Total of 125W is available: 25W available from PCI Express edge connector 100W available from 2x4 connector
Y	Y	Y	Total of 175W is available: 25W available from PCI Express edge connector 100W available from 2x4 connector 50W available from 2x3 connector

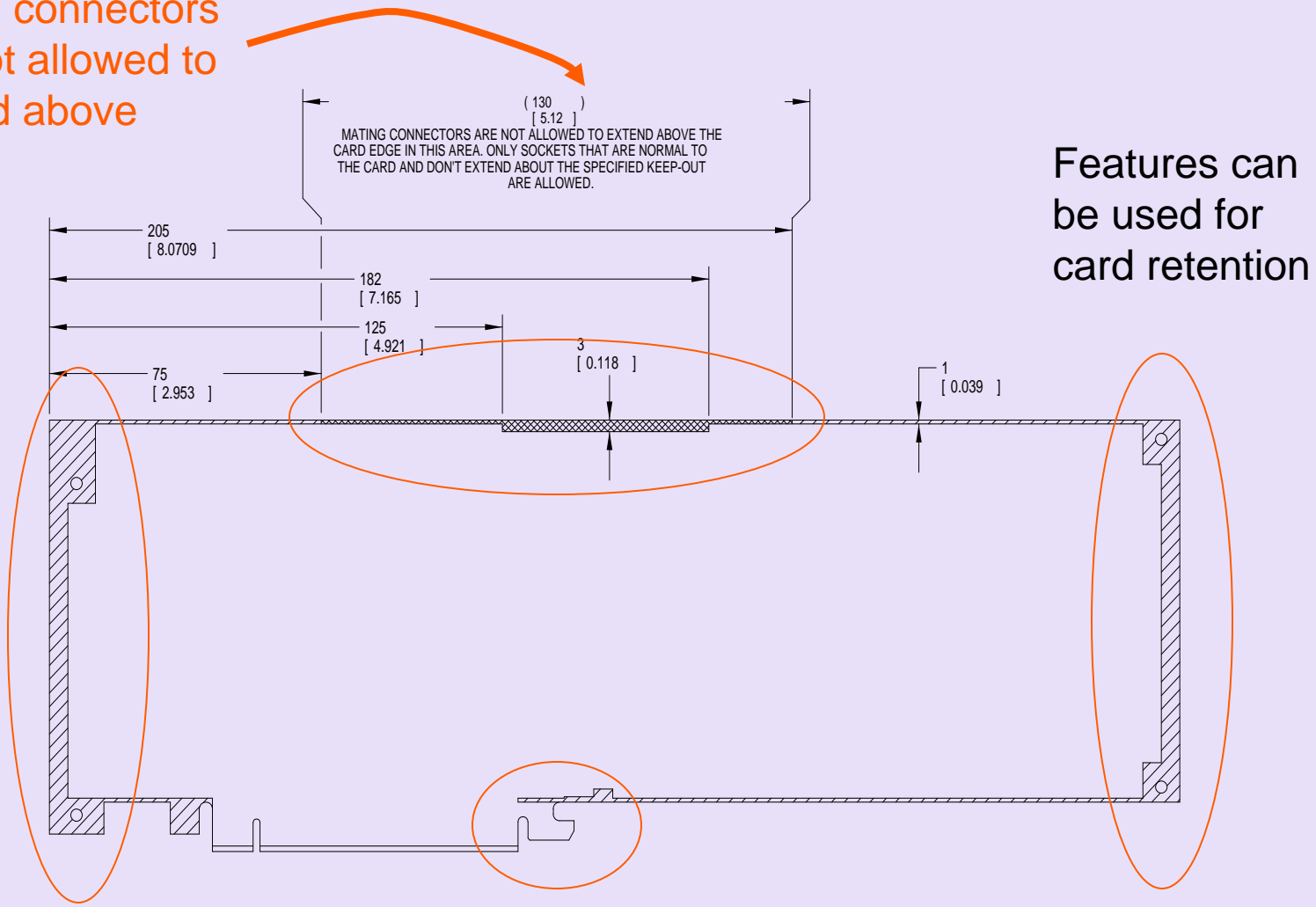
If the Slot\_Power\_Limit is bigger than or equal to the permitted initial power draw, the card can then draw power up to the Slot\_Power\_Limit in any order from the PCI Express edge connector, the 2x3 connector (if exists) and the 2x4 connector (if exists), subject to and limited to the individual power ratings of the respective connectors.

If the Slot\_Power\_Limit is smaller than the permitted initial power draw, the card can ignore the Slot\_Power\_Limit message and continue draw the same amount of power as permitted at system power up time.



# Card Keepout

Mated connectors  
are not allowed to  
extend above



# Other Mechanical Requirements

- Card total mass:  $\leq 1.5$  Kg
- All cards, including partial-length cards, shall be enabled for a full-length add-in card retainer as shown in CEM 2.0 Figure 6-6
- All cards, including partial-length cards, shall have means of being stiffened along their entire length from the rear bracket to the front card retainer

# Thermal and Acoustic

- Card inlet temperature:
  - ✓ Currently 50°C for (150W- 225W] cards and 45°C for (225W- 300W] cards
    - Detailed analysis still in process
  - ✓ Detail measurement methodology are still being discussed in the CEM workgroup
- System integrators would like to have some way to manage the heat dumped to the system, but how to do it is still TBD
- Acoustic discussion will serve as guidelines only

# Summary

- Method for deriving CEM Eye Diagrams from Base Spec demonstrated
- Eye diagram methodology demonstrated to be effective and robust
- High volume solution space challenging at 5.0 GT/s
  - ✓ 85 Nominal Channel Impedance Provides Reasonable Solution Space
- Measurement techniques for characterizing motherboard and adapter Tx and Rx defined
- Key contents of the 225/300W high power CEM spec discussed
- Stay tuned for further specification updates from PCI-SIG ([www.pcisig.com](http://www.pcisig.com))
  - ✓ Revision 0.9 of 225/300W high power CEM specification will be available for member review very soon

Thank you for attending the  
PCI-SIG Developers Conference Asia-  
Pacific 2007.

For more information please go to  
[www.pcisig.com](http://www.pcisig.com)



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