5 GT/s and 8 GT/s PCIe® Compared

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Introduction

- As the next generation of PCI Express® is defined, the information throughput will double and yet the symbol rate will only move from 5 GT/s to 8 GT/s. There are some significant changes and challenges:
  - ✓ While 5 GT/s communications used 8b/10b encoding to limit the longest occurrences of consecutive 1's and 0's, 8 GT/s will use scrambling. This has system budget and signal integrity impact on both transmitter and receivers.
  - ✓ Baseline wander due to the long runs of consecutive 1's and 0's will impact the available eye height.
  - ✓ AC coupling capacitors of 220 nF will be required in order to reduce the baseline wander
  - ✓ The combination of higher data rate and channel length up to 20" combine to cause Inter Symbol Interference (ISI), in addition to jitter from reference clocks and transmitters. These will limit the eye opening width available.

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Content

- Similarities for 5 GT/s (Giga Transfers/second) & 8 GT/s
  - ✓ System communicating over same 20” channel
- Differences between 5 GT/s and 8 GT/s
  - ✓ Double data throughput rate
  - ✓ 8b/10b encoding versus PRBS23 scrambling
  - ✓ Base line wander
- Transmitter
  - ✓ Phase Locked Loop (PLL) bandwidth
  - ✓ Pre-emphasis 2 taps at 5 GT/s versus 3 taps at 8 GT/s
    - – Pre-, main and post cursor
- Receiver Tolerance
  - ✓ Clock Data Recovery (CDR) bandwidth
  - ✓ Equalization

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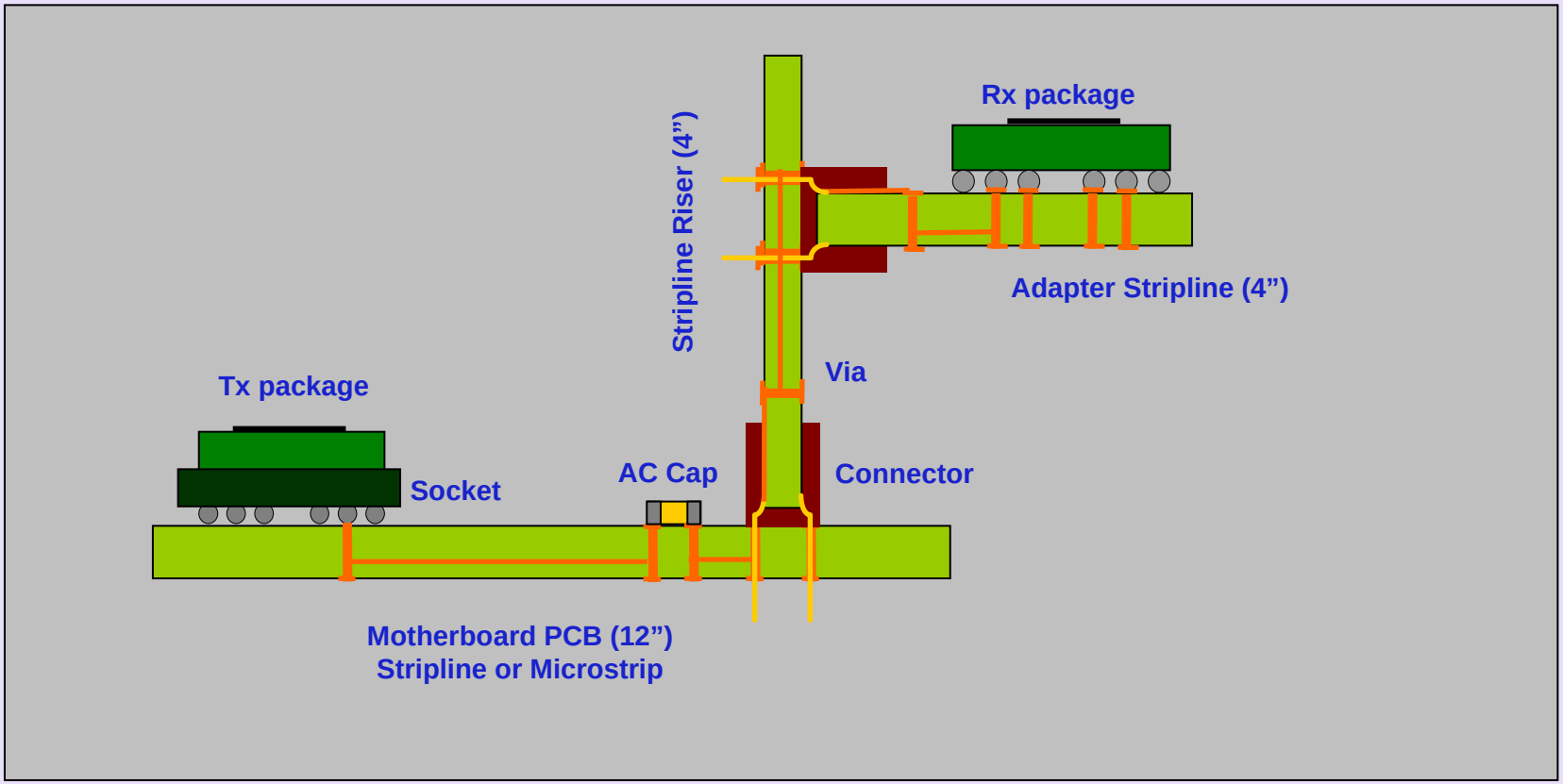
Interconnect Model

Model represents typical 1U or 2U server consisting of motherboard, riser, and adapter



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8 bits to 10 bits Encoding

Ensures that the longest length of identical transmitted logic levels is 5 consecutive bits

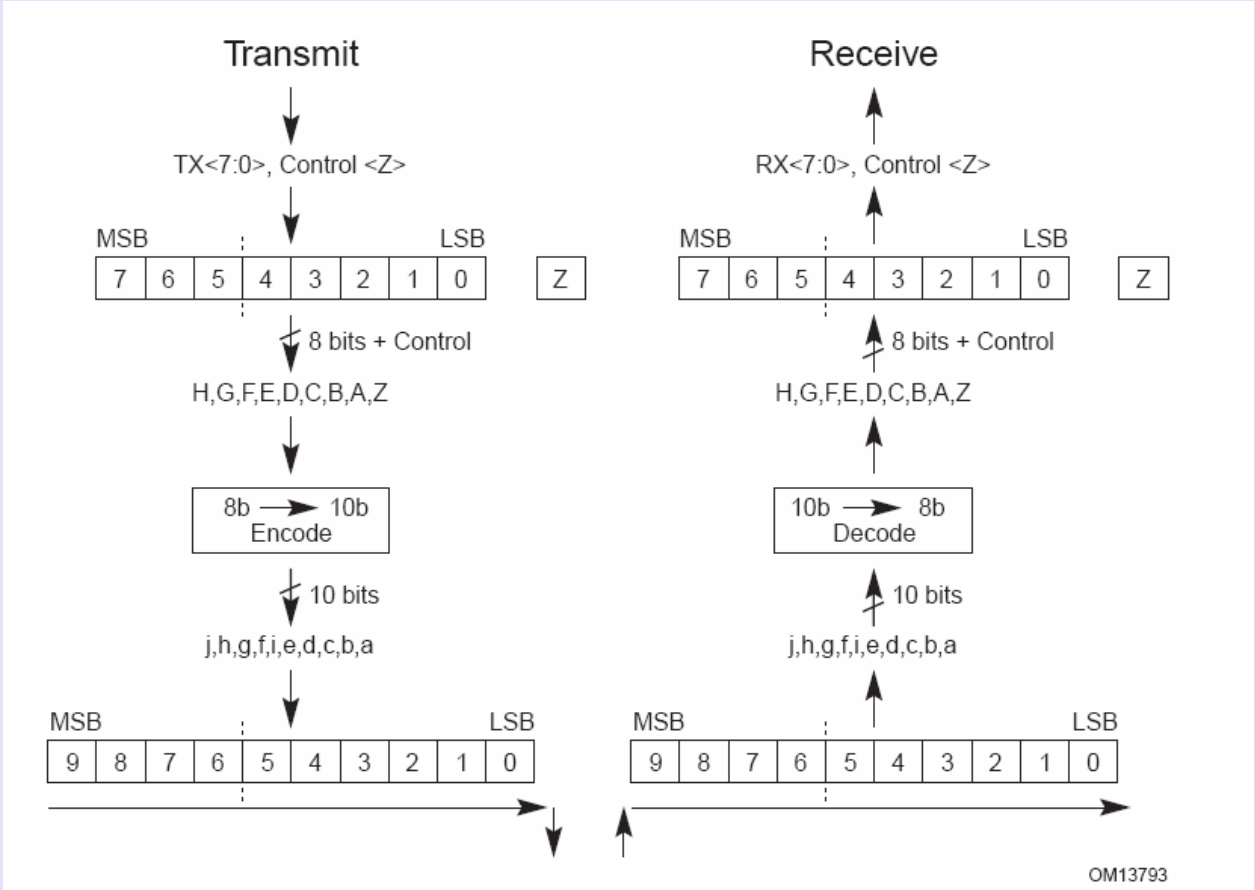

Figure 4-2: Character to Symbol Mapping

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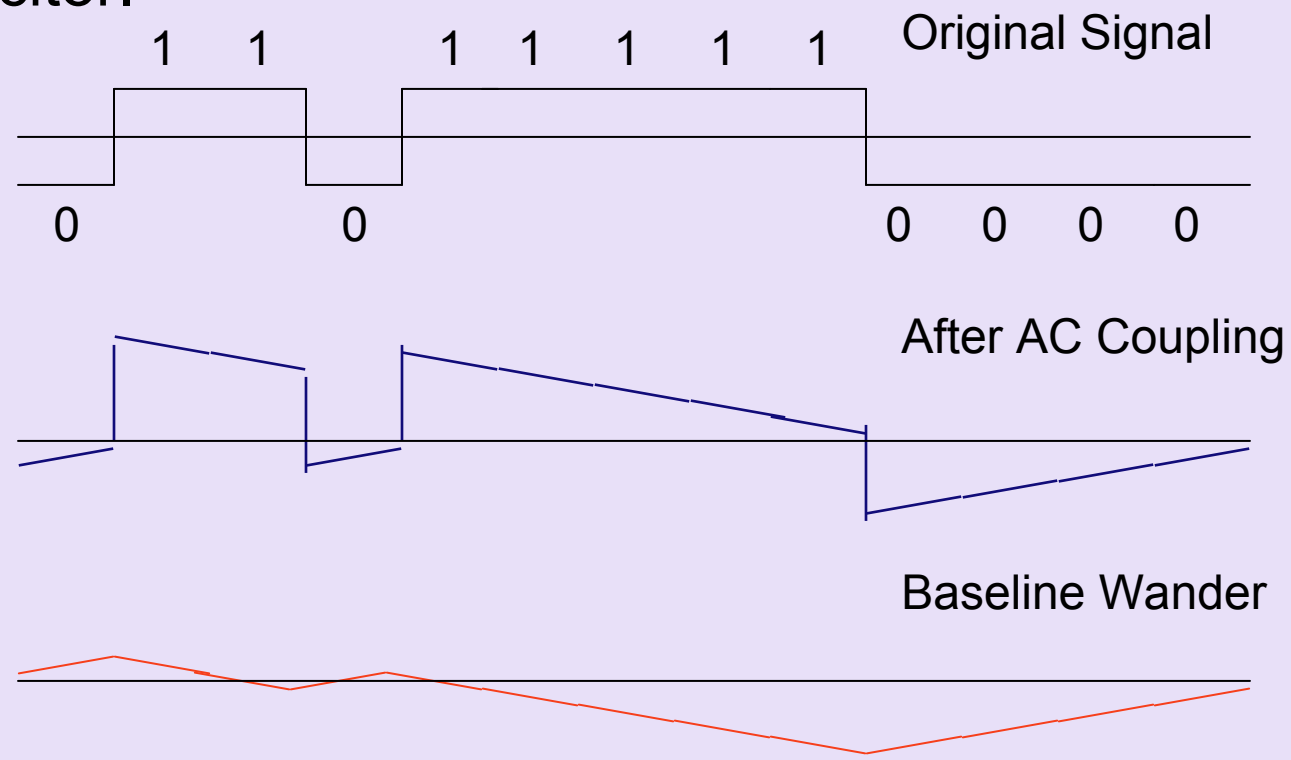
Baseline Wander

Long length of consecutive 1's or 0's create baseline wander due to the high pass filter effect of the AC coupling capacitor.



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Scrambling

- Missing the disparity control which provided a balanced number of 1's and 0's at 5 GT/s.
- 128/130 encoding inserts 01 or 10 symbols.
- However no upper bound on longest length of consecutive identical transmitted data levels.
- Theoretically the data could be "un-doing" the scrambling sequence.
  - ✓ The likely hood of this worst case is however small and diminishing as the length of the scrambling sequence increases.
  - ✓ X^23+X^21+X^18+X^15+X^7+X^2 Scrambling polynomial is longer than 8 Mbits.

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AC coupling Capacitors

- Even with the seed for PRBS to selected to minimize baseline wander:
  - ✓ Baseline wander is simulated to be < +/-2.3 mV.
  - ✓ The group which I work with will be conducting real measurements of the baseline wander using averaged waveforms of PRBS23 and worst case patterns.
- It is still important to increase the AC coupling capacitors to 220 nF nominal value:
  - ✓ Baseline wander more than doubles to +/-5.4 mV in simulations if AC coupling capacitor is 75 nF.

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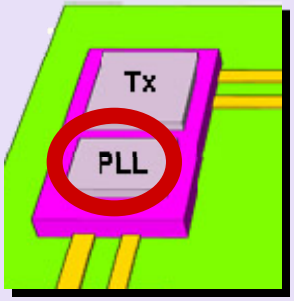
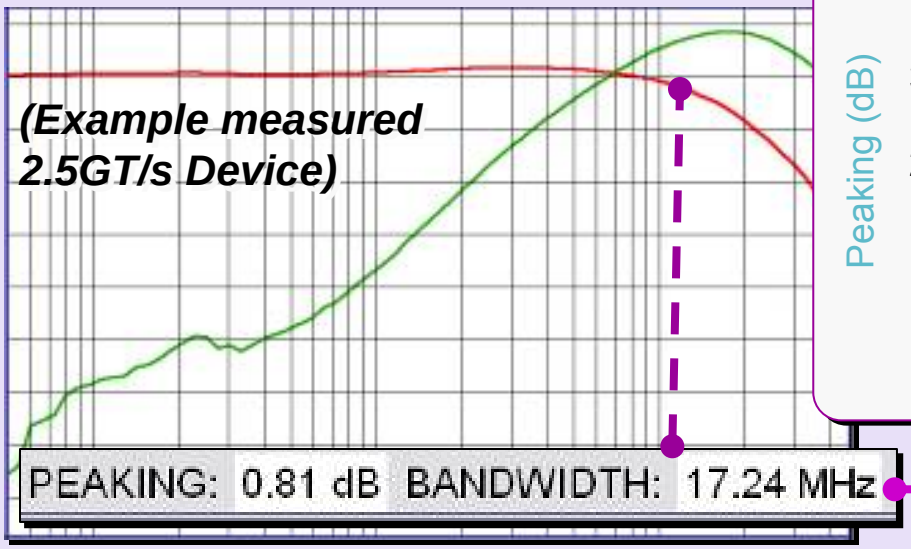
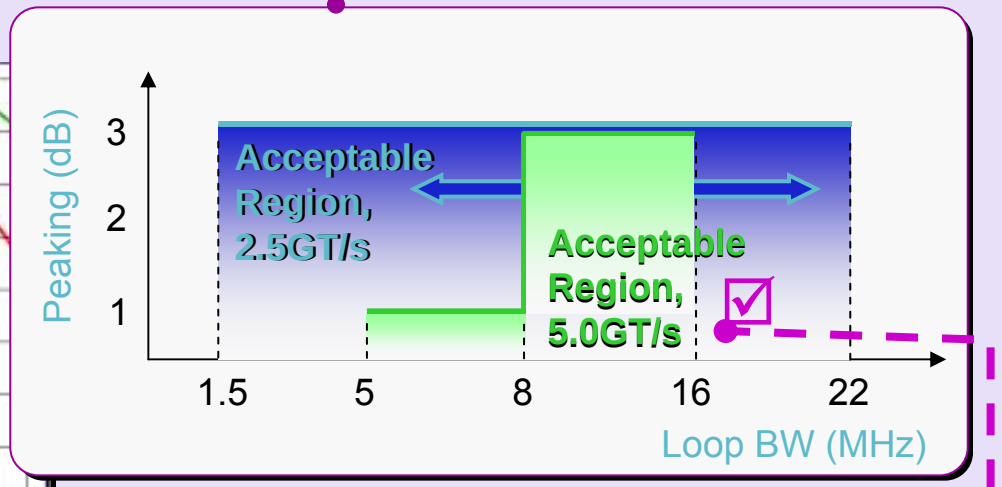
PLL Loop Bandwidth

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units
BW_{TX-PLL}	Maximum Tx PLL bandwidth	22 (max)	16 (max)	MHz
$BW_{TX-PLL-LO-3DB}$	Minimum Tx PLL BW for 3 dB peaking	1.5 (min)	8 (min)	MHz
$BW_{TX-PLL-LO-1DB}$	Minimum Tx PLL BW for 1 dB peaking	Not specified	5 (min)	MHz

From Table 4-9, 2.0 Base Spec







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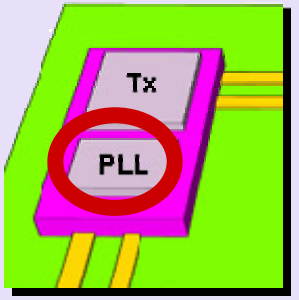
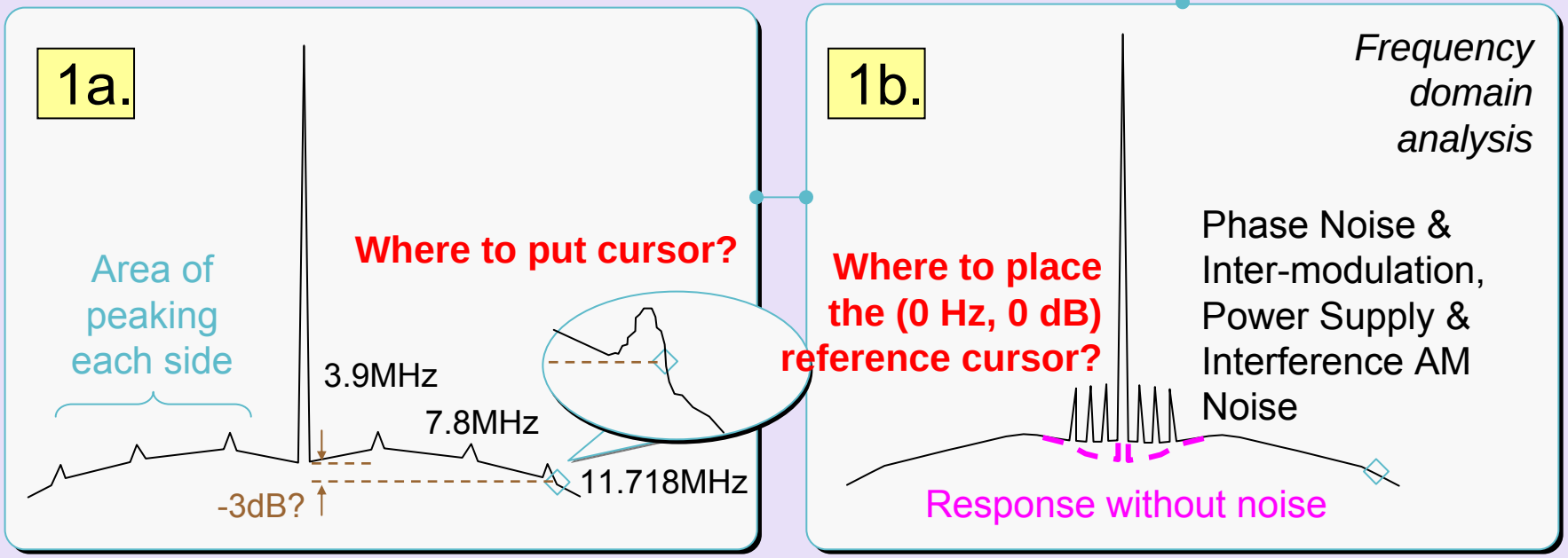
Possible Measurement Methods

- Currently two methods for characterizing PLL response:
  - ✓ Spectrum Analyzer — Reference issues
  - ✓ Clock PLL Analyzer — Follows data edge for Better Accuracy & Repeatability





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Assumptions/Enablers

- Statistical jitter analysis
  - ✓ More closely approximates reality
  - ✓ Doing without leaves too much margin on the table
- Optimized reference clock and CDR bandwidths
  - ✓ Permits use of existing reference clock infrastructure

	PCIe 2.0	PCIe 3.0***
Min CDR BW	1.5 MHz	10 MHz
PLL BW	5-16 MHz	2-4 MHz

- Trainable equalization to mitigate channel effects
  - ✓ Rx equalization: multi-tap linear or DFE?*** (study in progress)
  - ✓ Tx equalization: multi-tap linear*** (study in progress)

*** Currently in discussion; not the final spec

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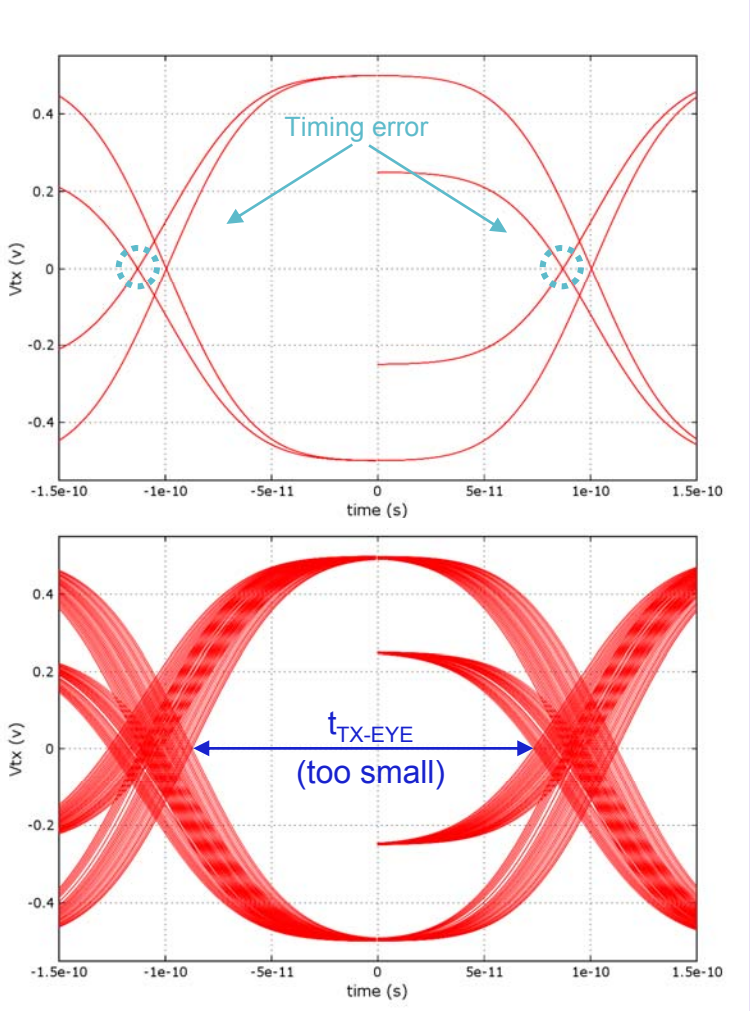
Jitter from de-emphasis

- Jitter due to de-emphasis is actually desirable and the transmitter should not be punished for this.
  - ✓ Channel effectively removes the de-emphasis jitter
  - ✓ Tx approximates the inverse of the HF loss of the channel
- De-emphasis causes a timing error in cumulative eye measurement
  - ✓ Closes the eye on right side
  - ✓ Overestimates eye opening on left side
  - ✓ up to17 ps error at 5 GT/s



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5.0 GT/s Rx Tolerancing Parameters (common clock architecture)

Parameter	Description	Min	Max	Units	Notes
UI	Unit Interval without including of SSC	200.06	199.94	ps	Over 10^6 UI
$T_{RX-HF-RMS}$	1.5 – 100 MHz RMS jitter		3.4	ps RMS	Spectrally flat
$T_{RX-HF-DJ-DD}$	Max Dj impinging on Rx under test		88	ps	2, 4
$T_{RX-SSC-RES}$	33 kHz Refclk residual	--	75	ps	
$T_{RX-LF-RMS}$	<1.5 MHz RMS jitter	--	4.2	ps RMS	Spectrally flat
$T_{RX-MIN-PULSE}$	Minimum single pulse applied at Rx	120		ps	2
$V_{RX-MIN-MAX-RATIO}$	Min/max pulse voltage ratio seen over an time interval of 2 UI.	--	5		2
V_{RX-EYE}	Receive eye voltage opening	120		mVPP diff	1, 3
$V_{RX-CM-CH-SRC}$	Common mode noise from Rx	--	300	mVPP	2

Notes:

1. Refer to Figure 4-41 for a description of how the Rx eye voltage is defined.
2. Accumulated over 10^6 UI.
3. Minimum eye is obtained by first injecting maximum Dj and then adjusting Rj until a minimum eye (defined by T_{RX-EYE}) is reached. Rj is filtered with a BPF having f_{C-LOW} and f_{C-HIGH} of 1.5 MHz and 100 MHz, respectively with step rolloff at 1.5 MHz and a 20 dB/decade rolloff on the high side. Minimum eye width is defined for a sample size equivalent to a BER of 10^{-12}.
4. Different combinations of $T_{RX-HF-DJ-DD}$ and $T_{RX-HF-RMS}$ are needed to measure T_{RX-TJ_CC} and $T_{RX-DJ-DD-CC}$.

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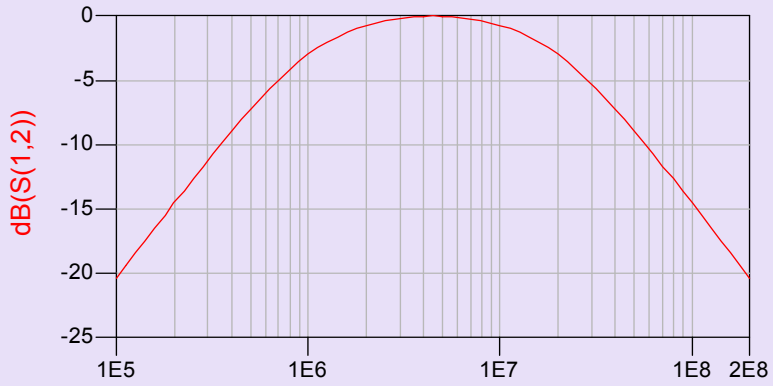
Band limited Random Jitter

- On one hand it is clear by specifying $f_{C\text{-}HIGH}$ = 100 MHz with a 20 db/decade roll off that the Rj level is required to be down by 3dB at 100 MHz.
- This is further substantiated by the definition of $f_{C\text{-}HIGH}$ in the original workgroup documents and version 0.4 of the base specification.



Filter function applied to white Rj corresponds to:
f_{C_LOW} = 1.0 MHz, f_{C_HIGH} = 20 MHz
Rolloff = 20 dB/decade

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Band limited Random Jitter

- On the other hand the note appears to require spectral flatness to 100MHz.
- The question is: “How flat”?

“Flatness” to 100 MHz	-3 dB Frequency
3 dB	100 MHz
2 dB	133 MHz
1 dB	200 MHz
0.5 dB	300 MHz
0.25 dB	420 MHz
0.1 dB	666 MHz

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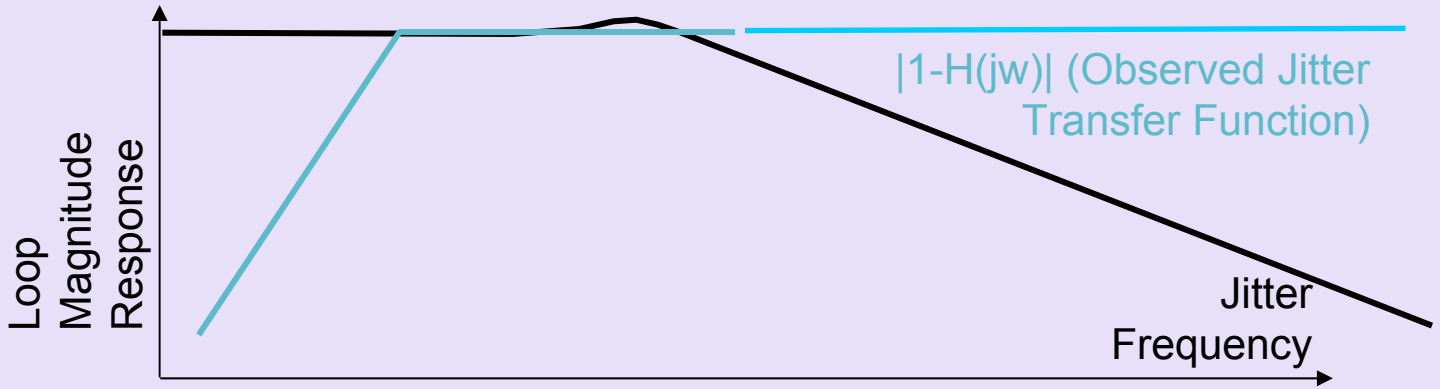
Band limited Random Jitter

- What would happen if one tested the same receiver with 100 MHz and 666 MHz 3 dB bandwidth Rj?
  - ✓ If the receiver CDR jitter transfer bandwidth is less than 1.5 MHz nothing would happen
  - ✓ If the CDR bandwidth was let's say 10 MHz then the receiver would see 91.4% of the Rj from the 100 MHz but as much as 98.7% from the 666 MHz source.



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Band limited Random Jitter

- The two requirements are inconsistent unless:
- HF Rj noise source that is spectrally flat from 1.5MHz to 100MHz before filtering.
- This spectrally flat noise source is then cascaded through two shaping filters:
  - ✓ 1. A high pass filter with a step roll off that is 3dB down at 1.5MHz.
  - ✓ 2. A low pass filter with a 20dB/decade roll off that is 3dB down at 100MHz.

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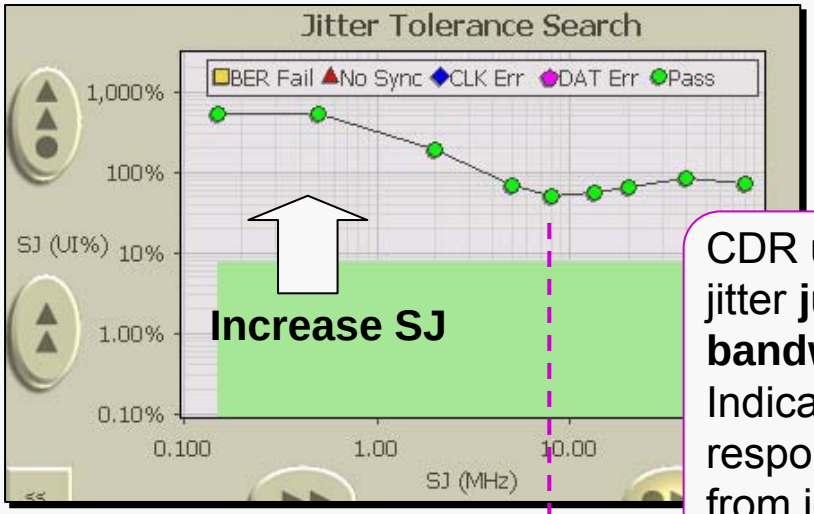
Going beyond $T_{RX-HF-DJ-DD}$

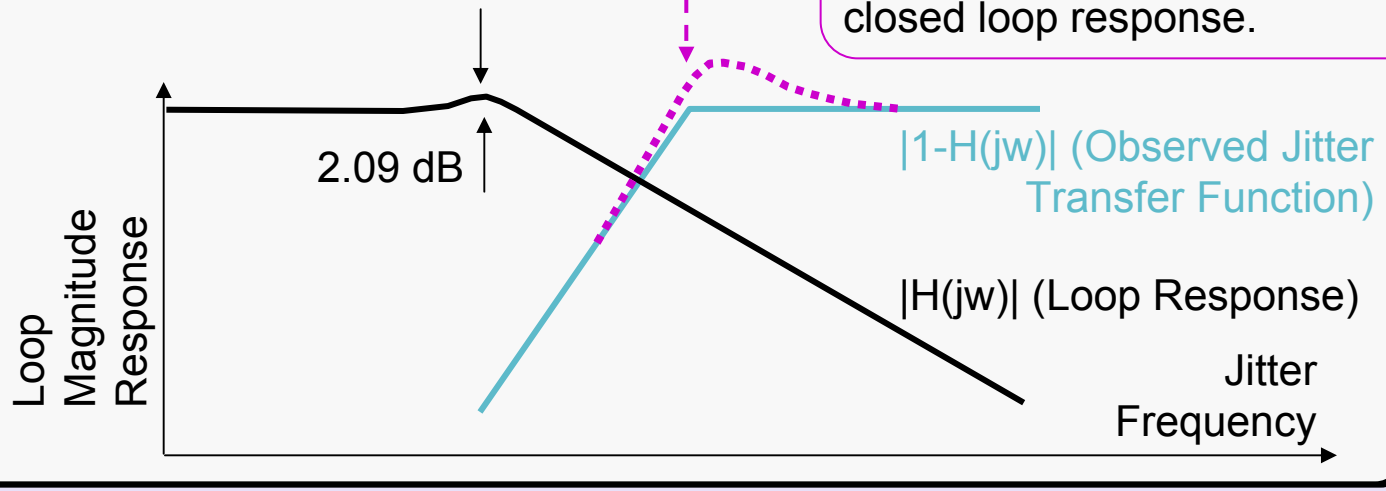
Search algorithms allow increasing of Sine jitter (Sj) until the failure point at each frequency is reached.



CDR usually **most sensitive** to jitter **just beyond** the **loop bandwidth.**
Indicates peaking in the inverse response, caused by deviation from ideal critical damping (2.09 dB peaking) and/or delay in the closed loop response.

CDR Response

(Jitter Transfer function directly visible in Rx testing)



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