Conventional PCI

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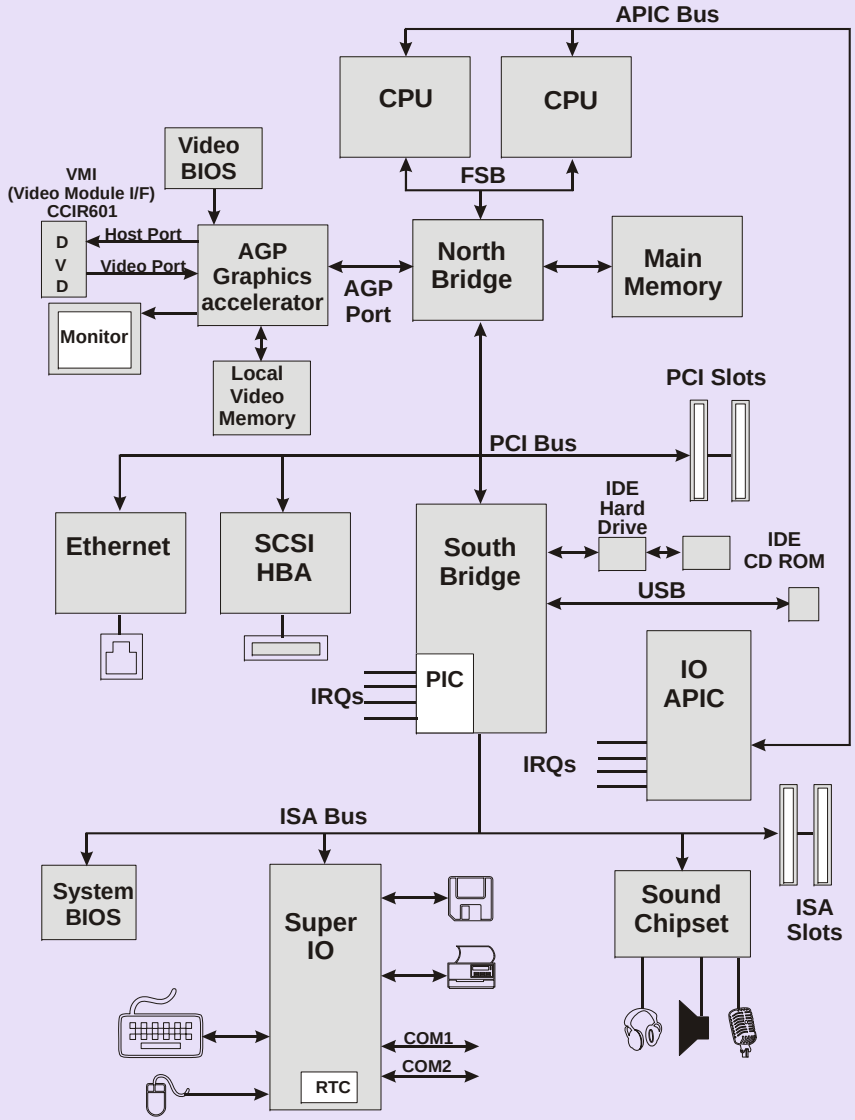
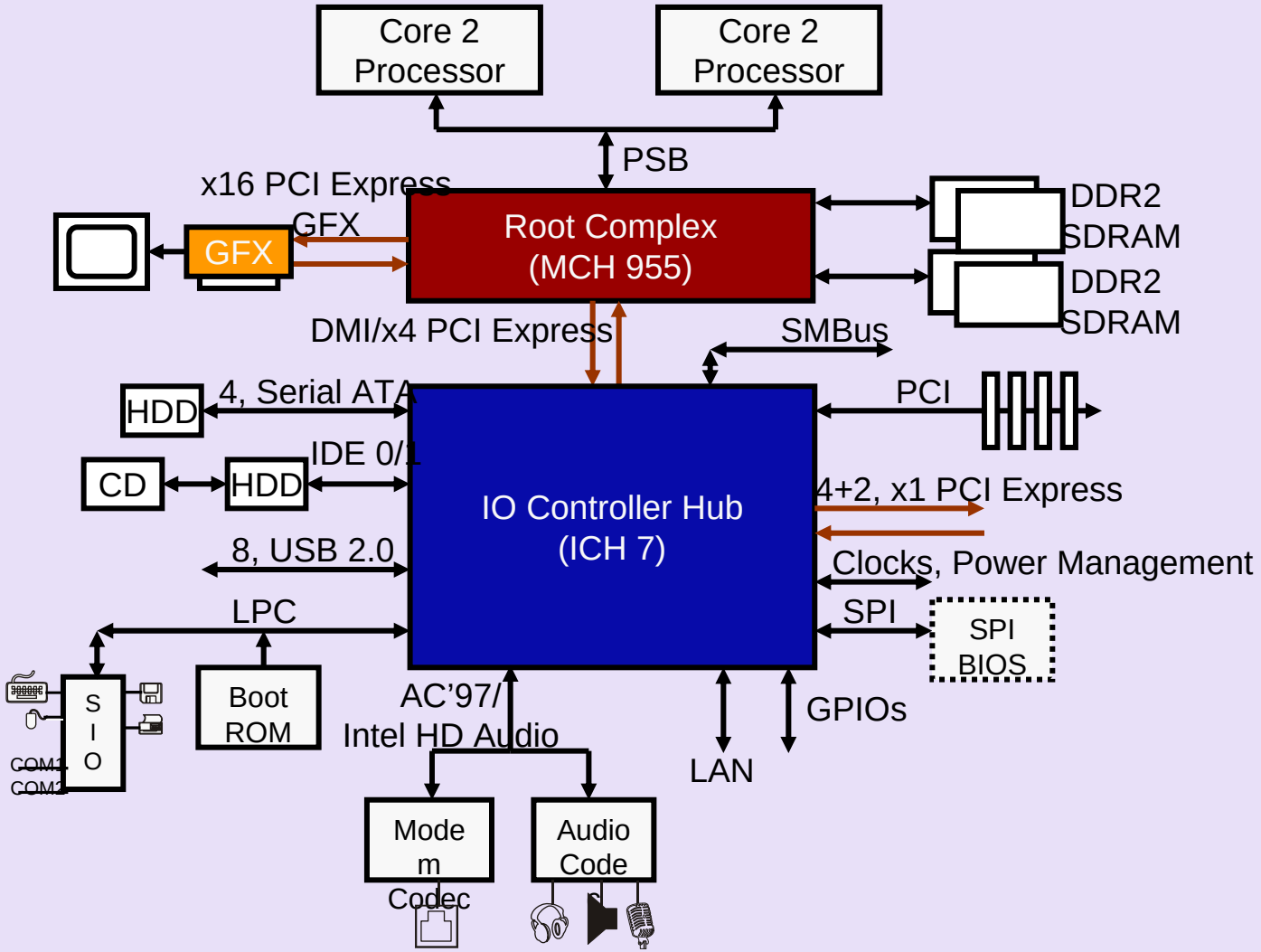
Agenda

- Big picture
- Features
- Transaction protocol
- Electrical signaling
- Arbitration
- Transaction types
- Configuration mechanism and space
- Interrupt handling

Example: Intel 440 Chipset Based PC System



Example: Intel 955 Chipset Based PC System



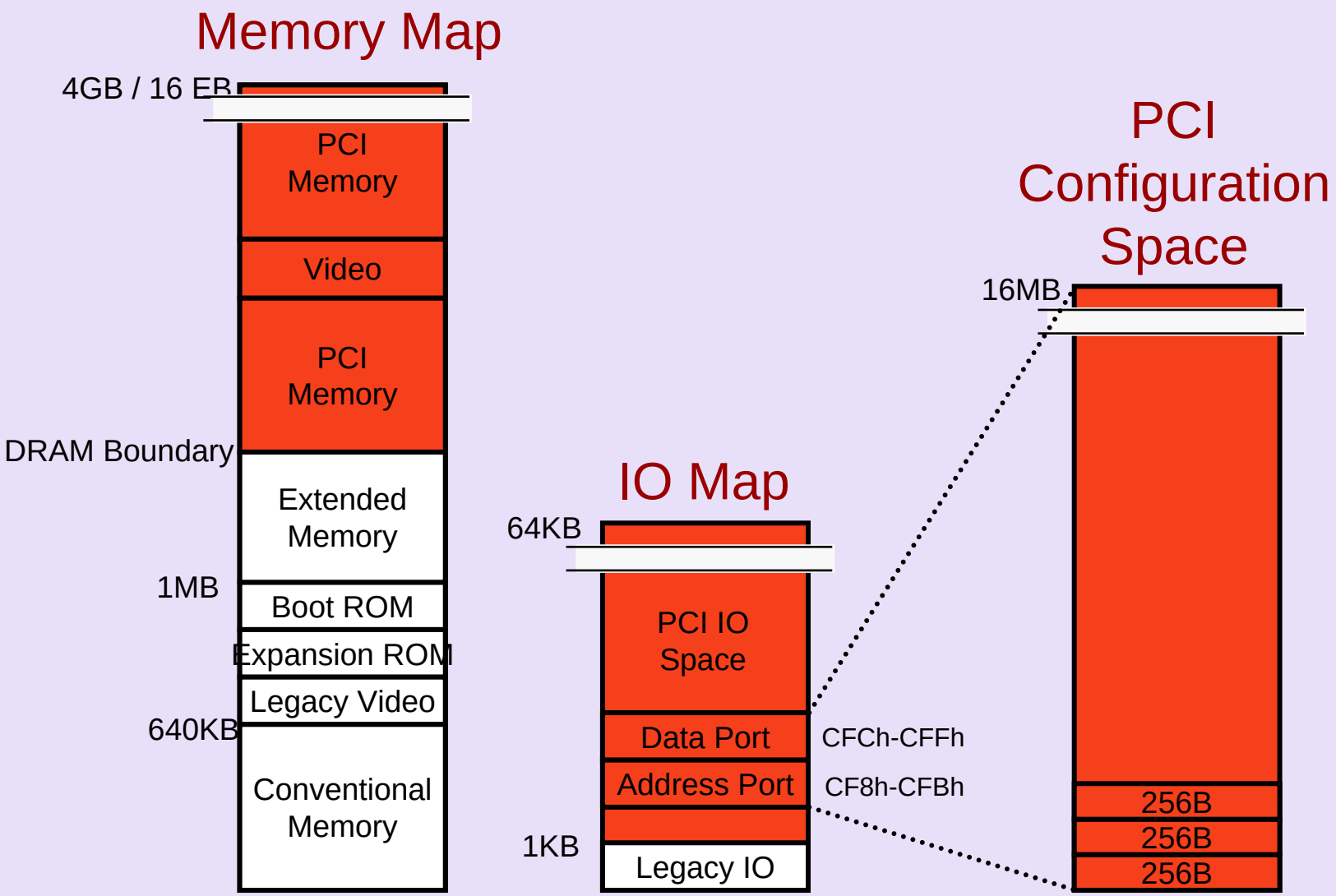
PCI Bus Features

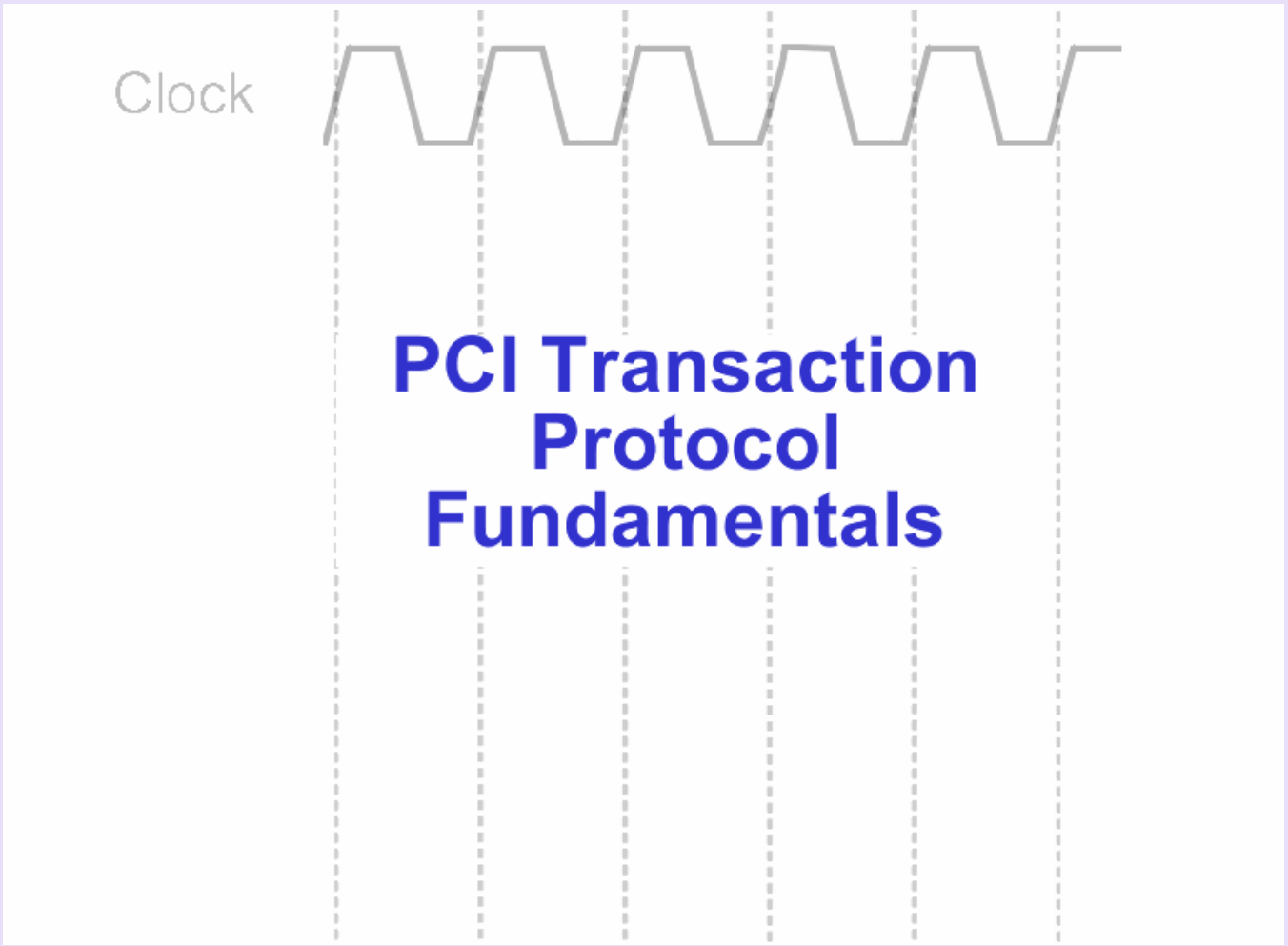
- Processor Independence
- Support for 256 functional devices per bus
- Support for up to 256 PCI buses
- Low power consumption
- Burst transactions supported
- 33MHz or 66MHz top frequencies
- 32- or 64-bit data bus width
- Access time as little as 2 clocks for writes, 3 clocks for reads

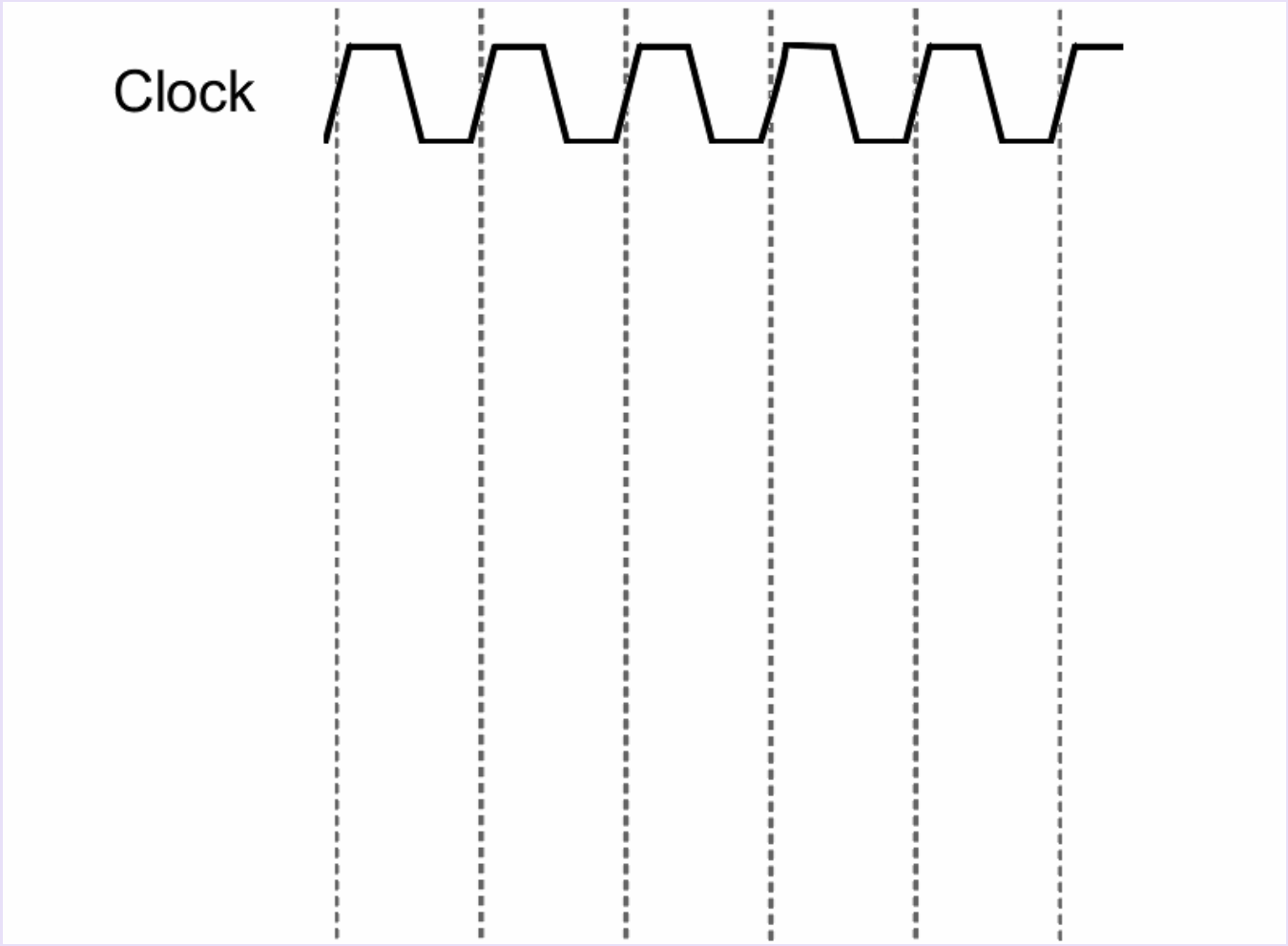
PCI Bus Features, continued

- Concurrent bus operation
- Bus master support
- Hidden bus arbitration
- Low pin count
- Transaction integrity checking
- Three address spaces:
  - ✓ Memory (4GB optionally 16EB),
  - ✓ I/O (64KB optionally 4GB), &
  - ✓ Configuration
- Auto configuration
- Software transparency
- Add-in cards with different dimensions

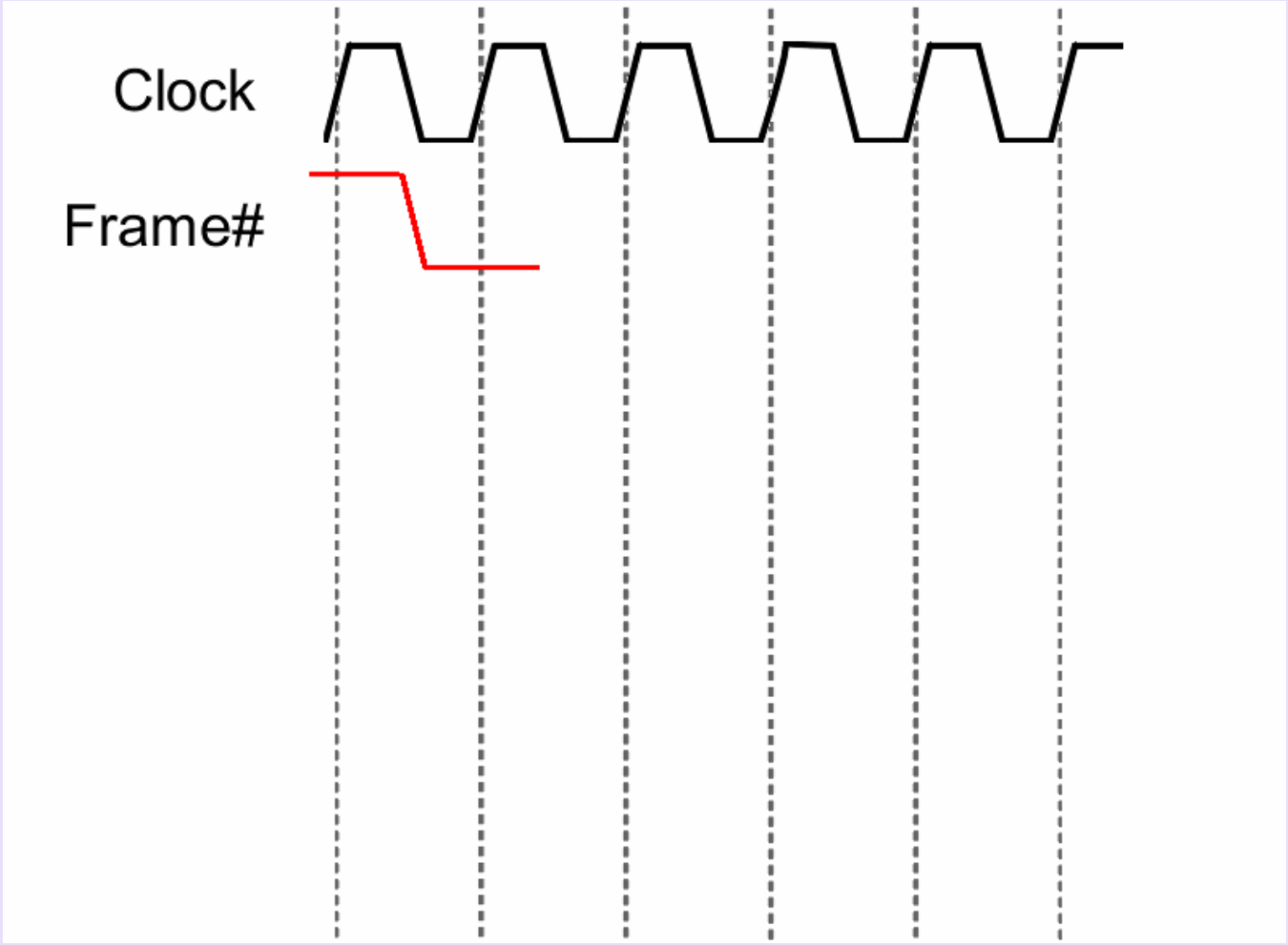
PC Address Space Mapping

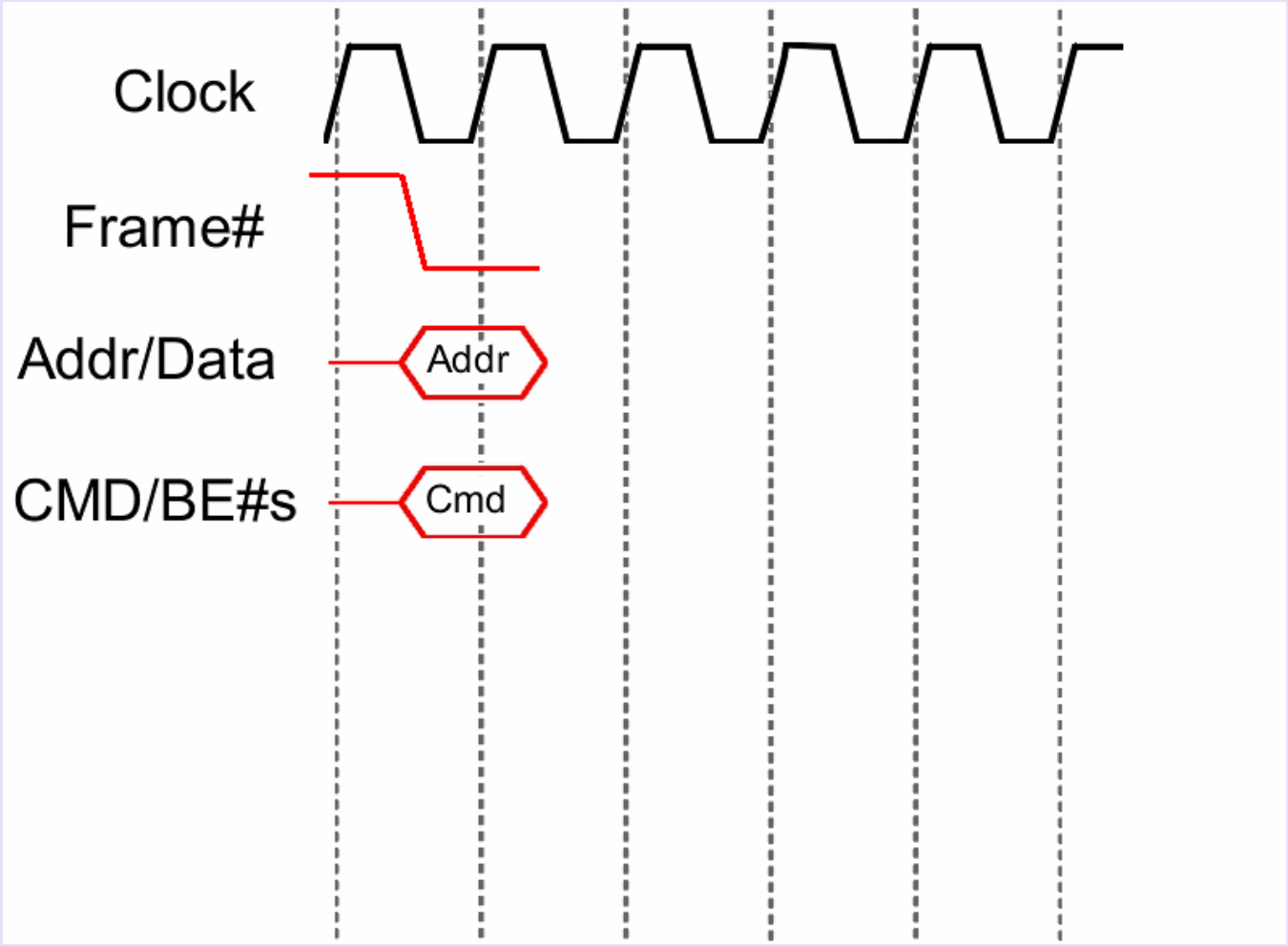


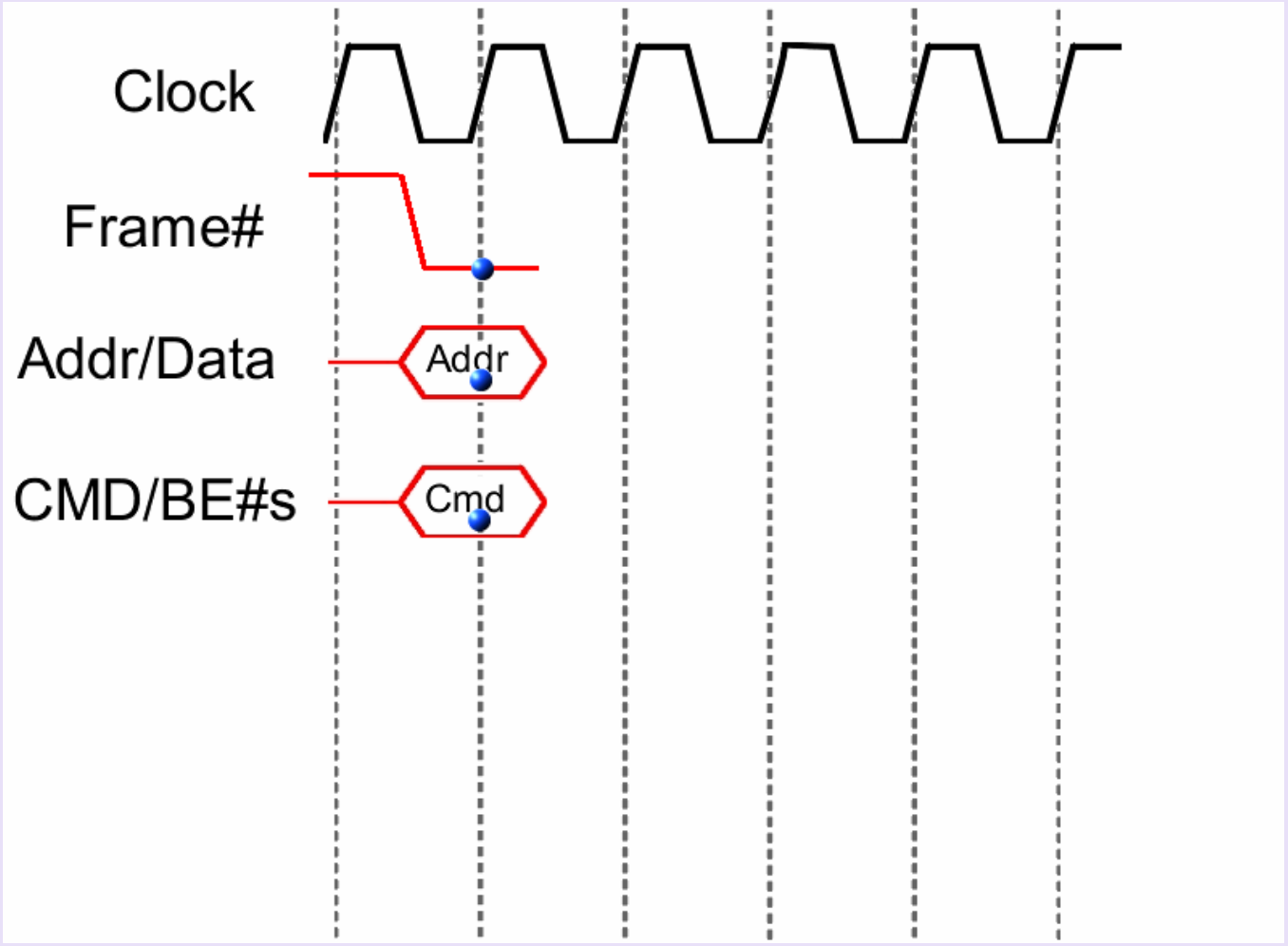


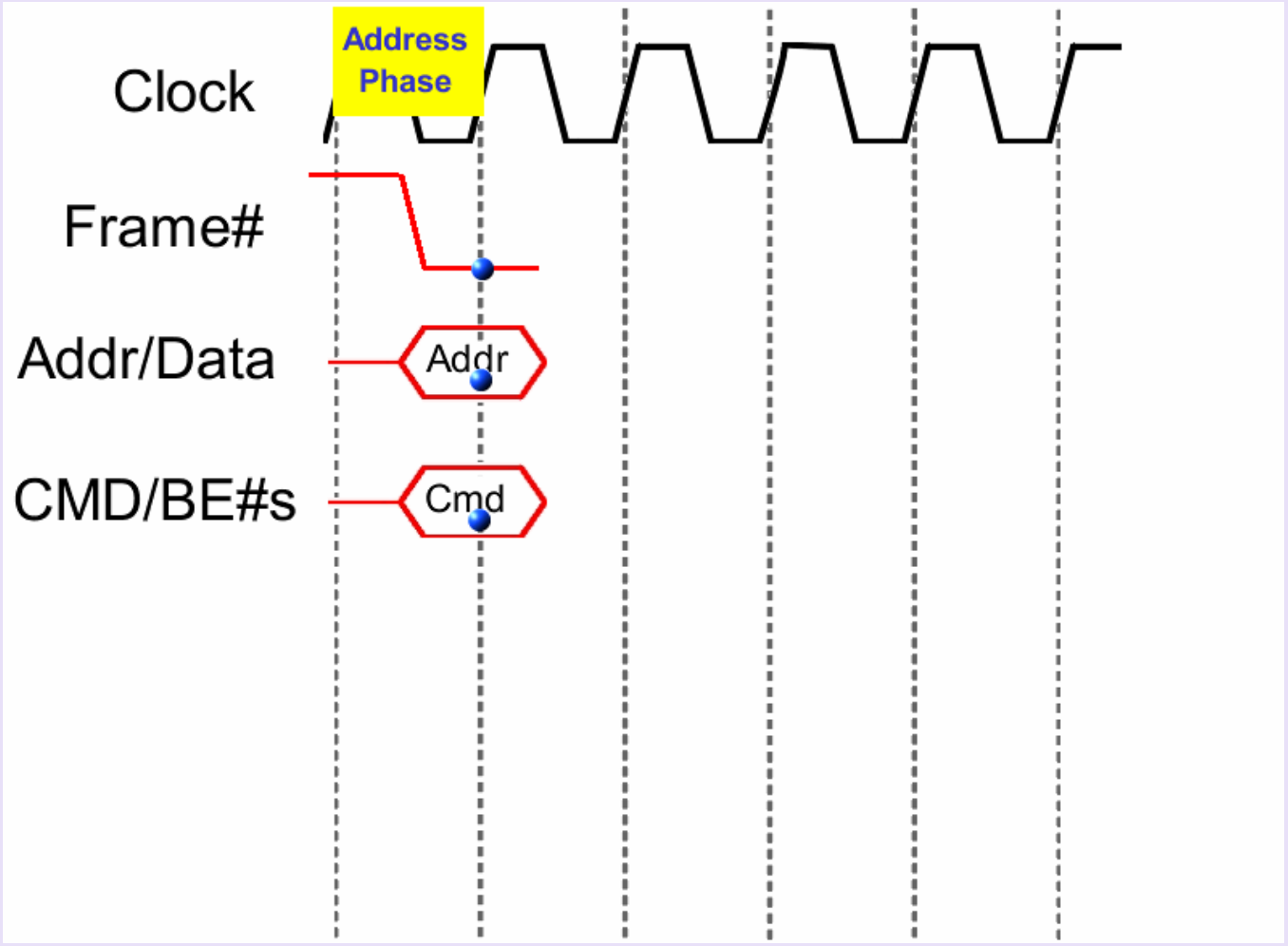


Address Phase

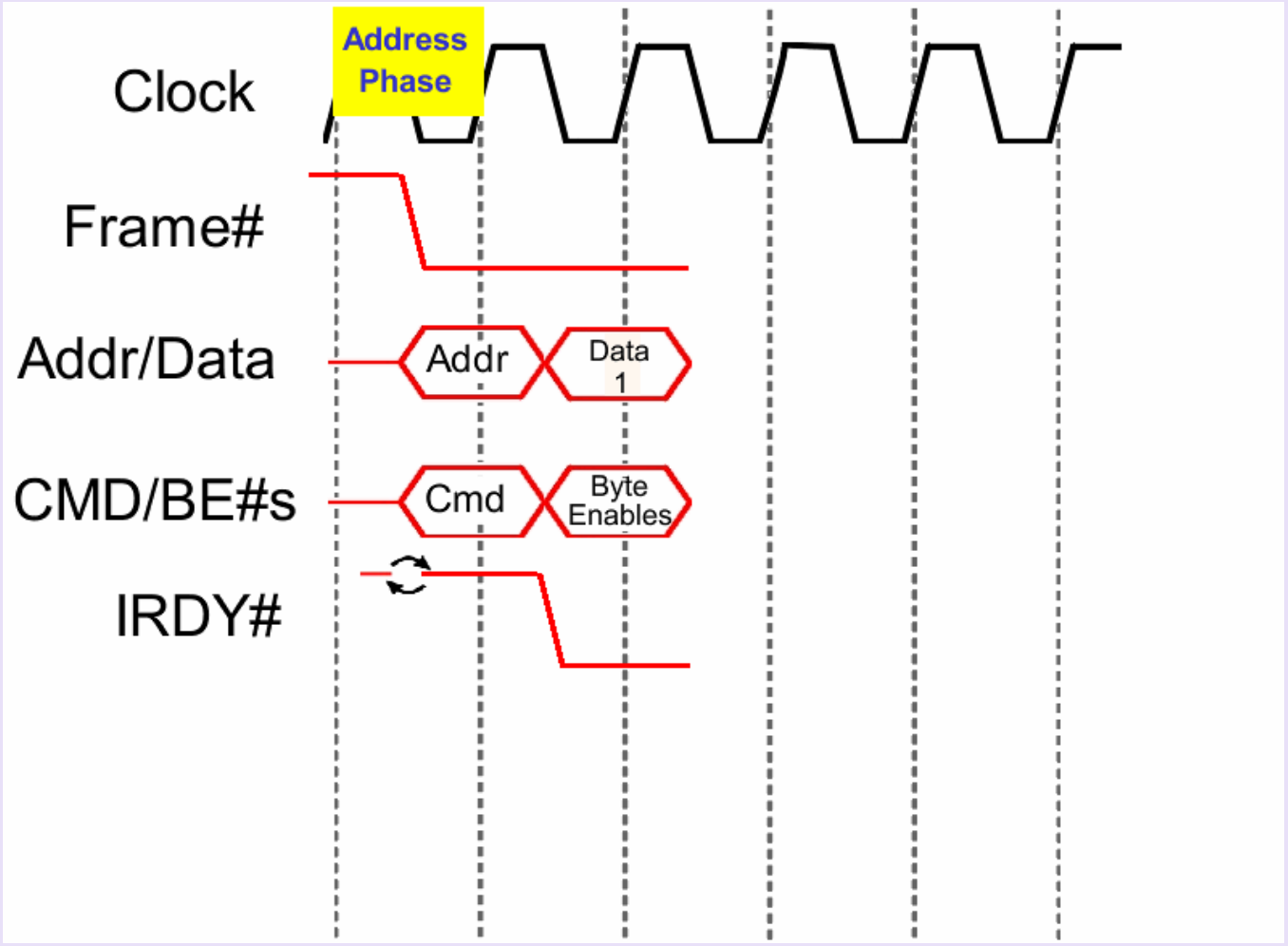




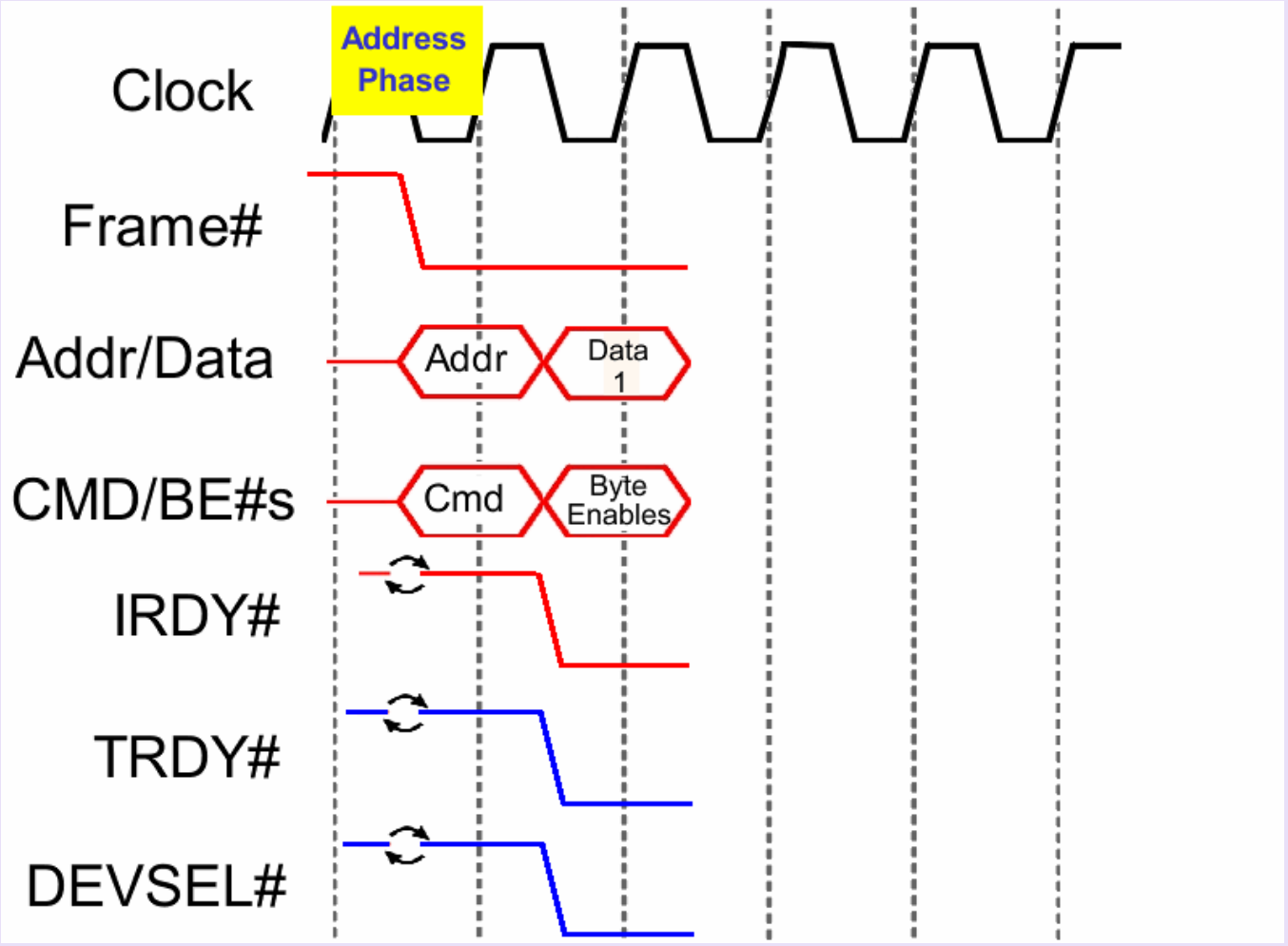


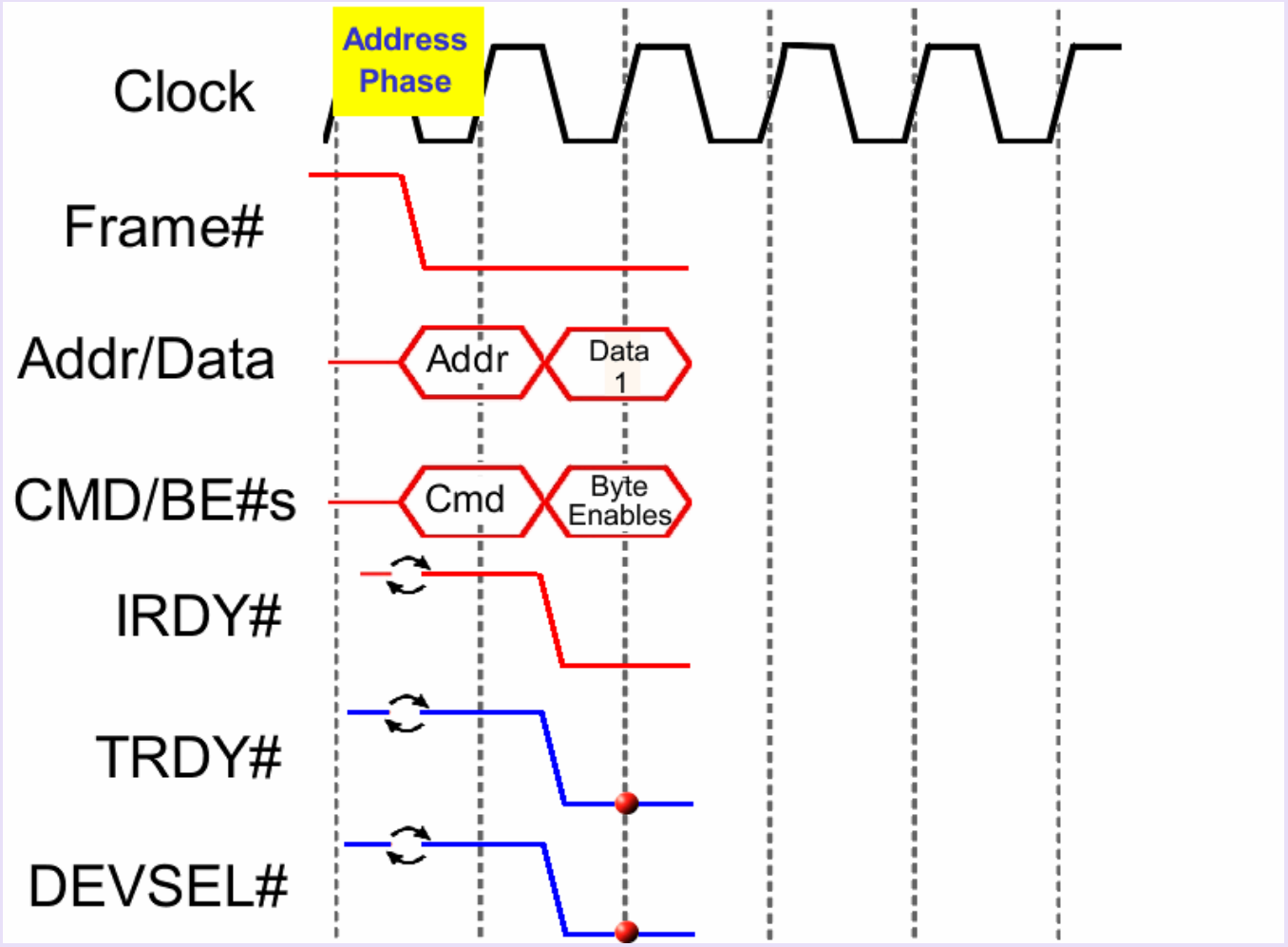


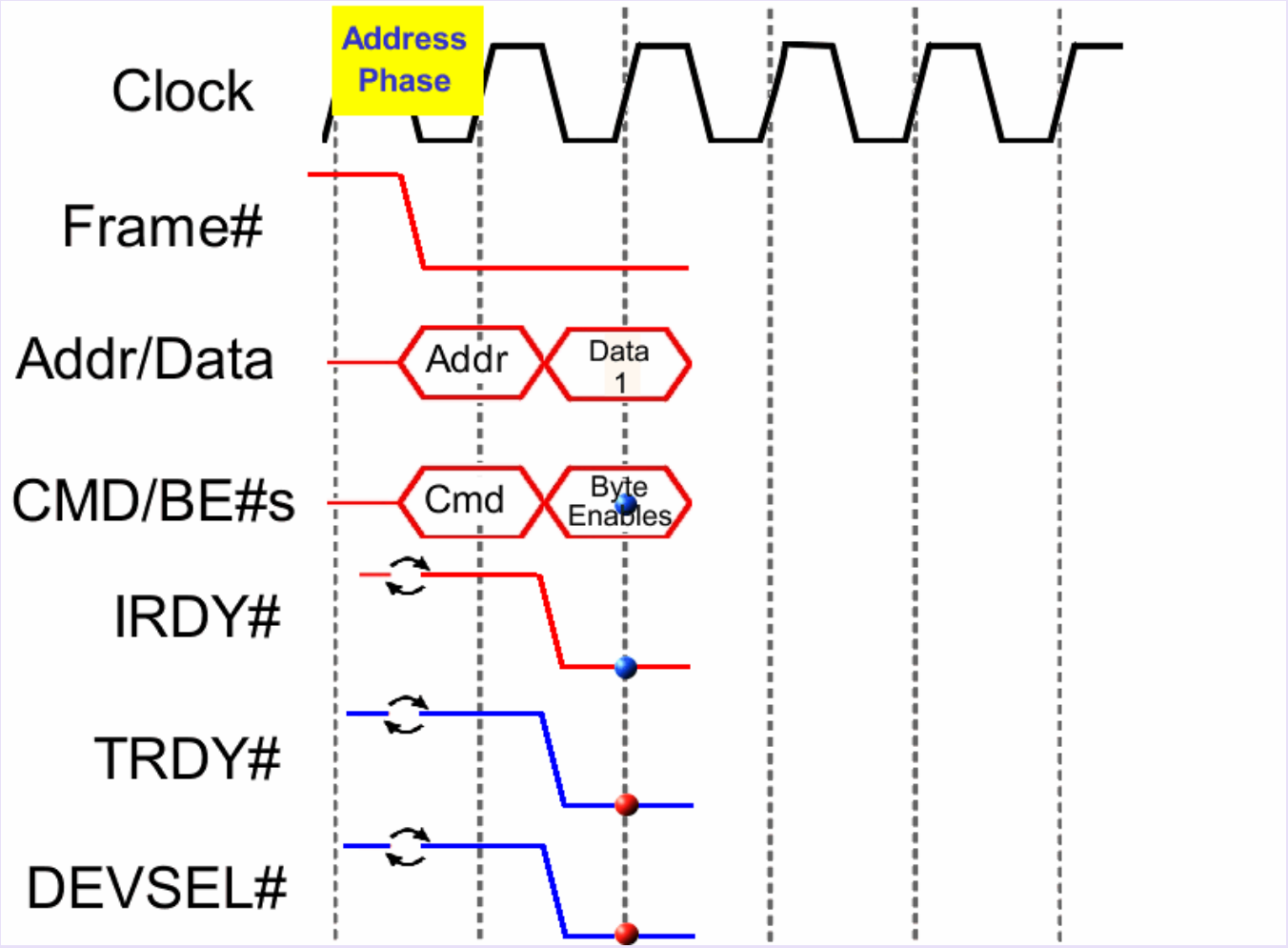
Data Phases

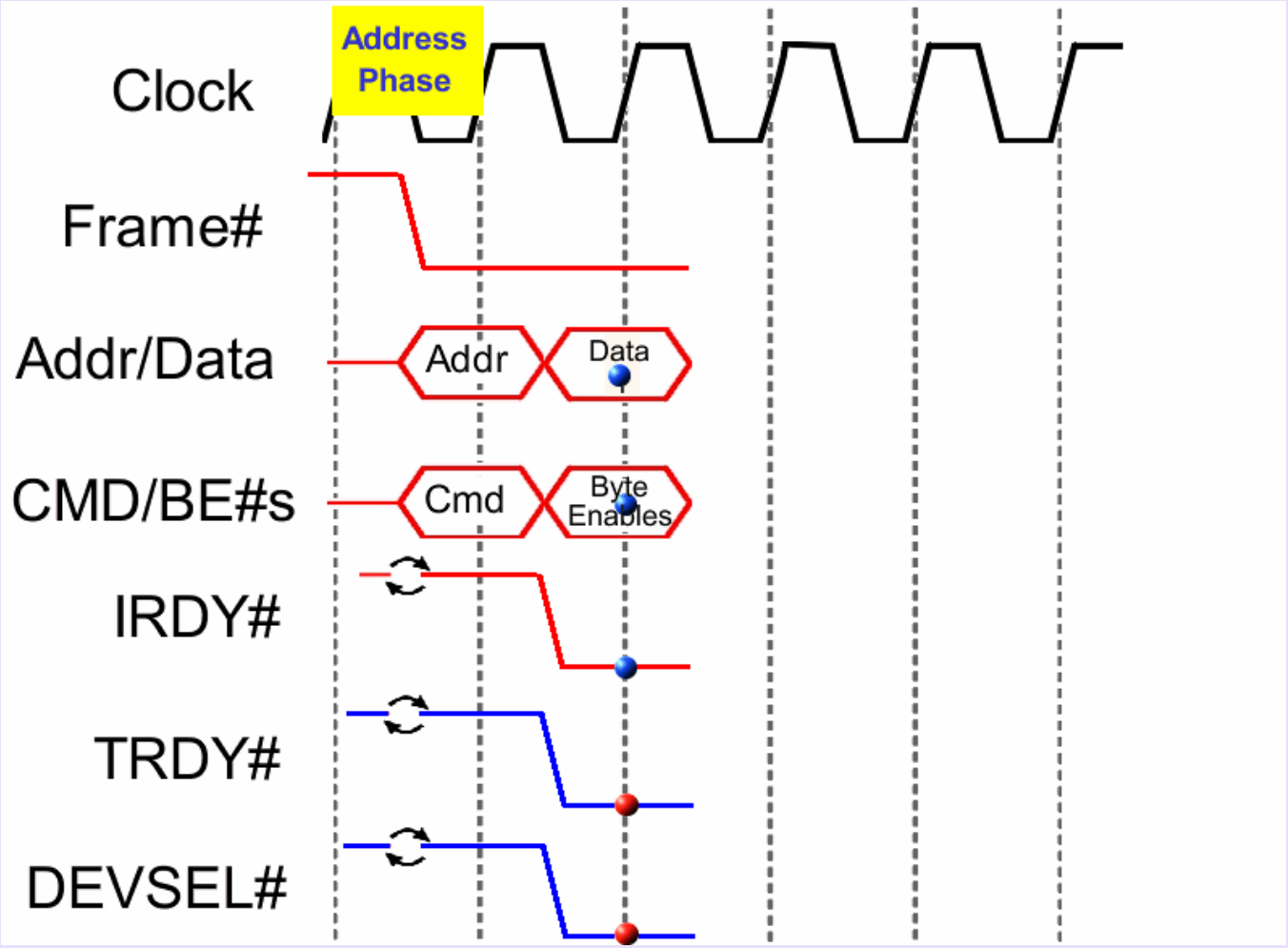


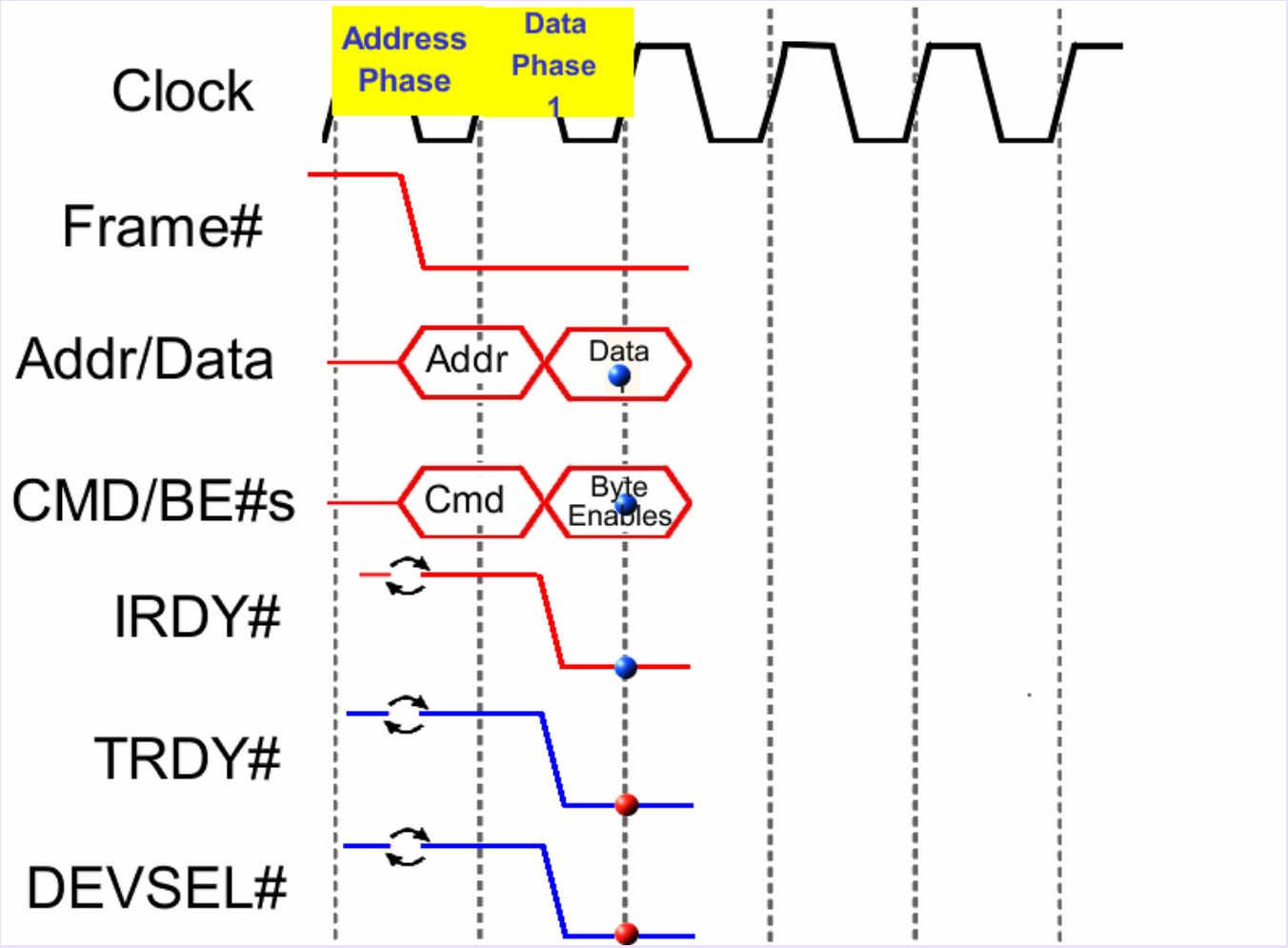
Claiming the Transaction

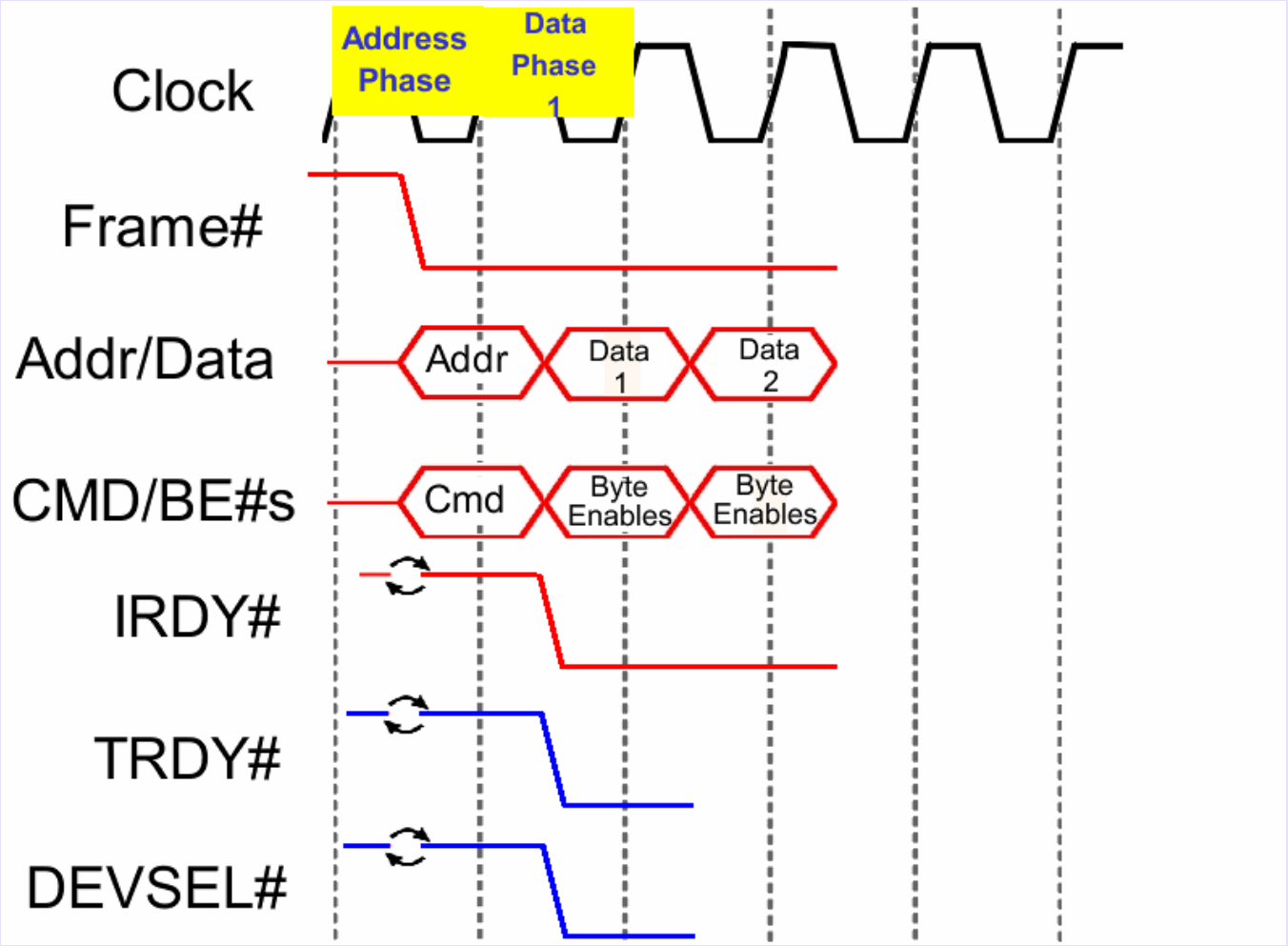


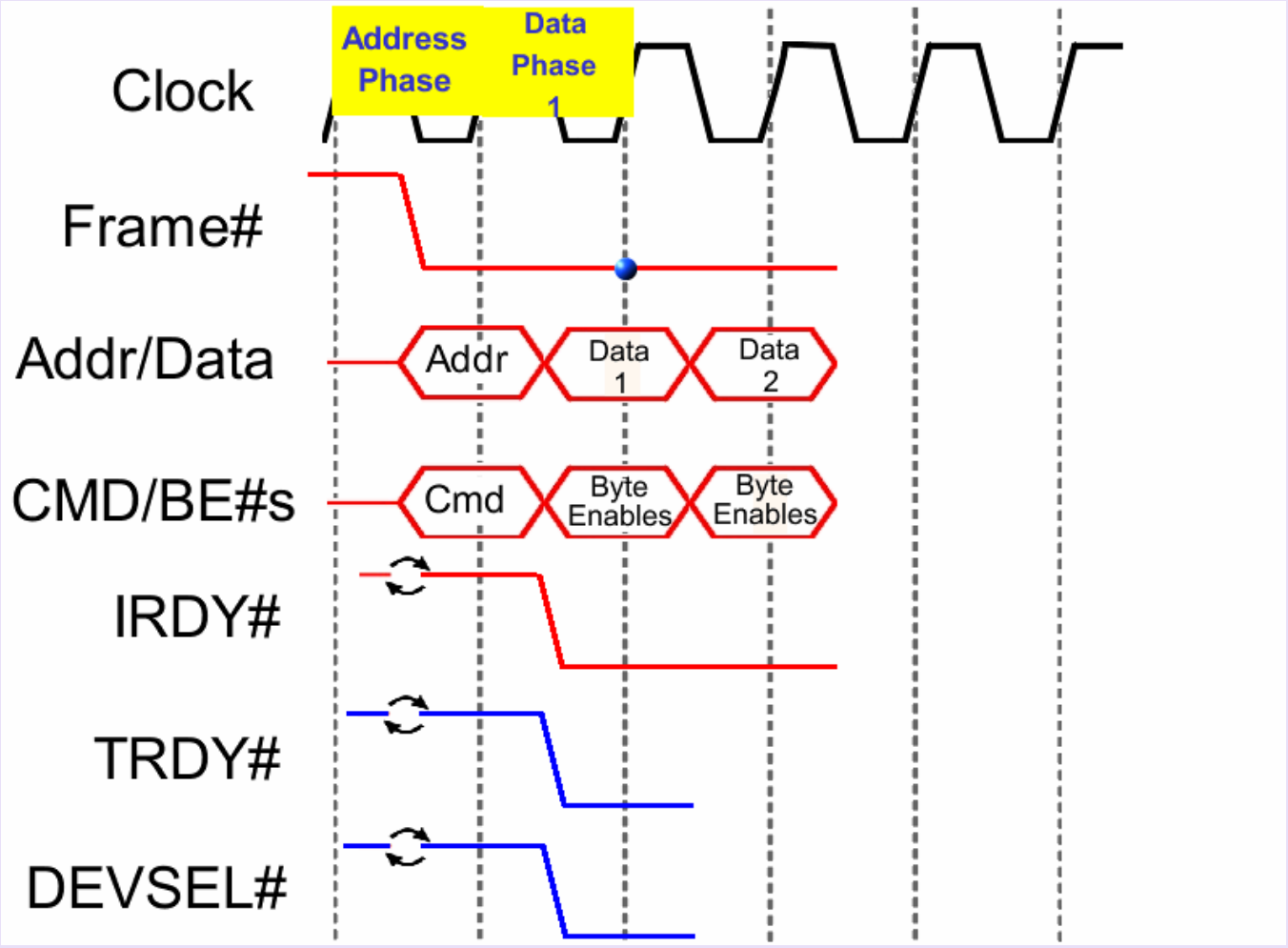


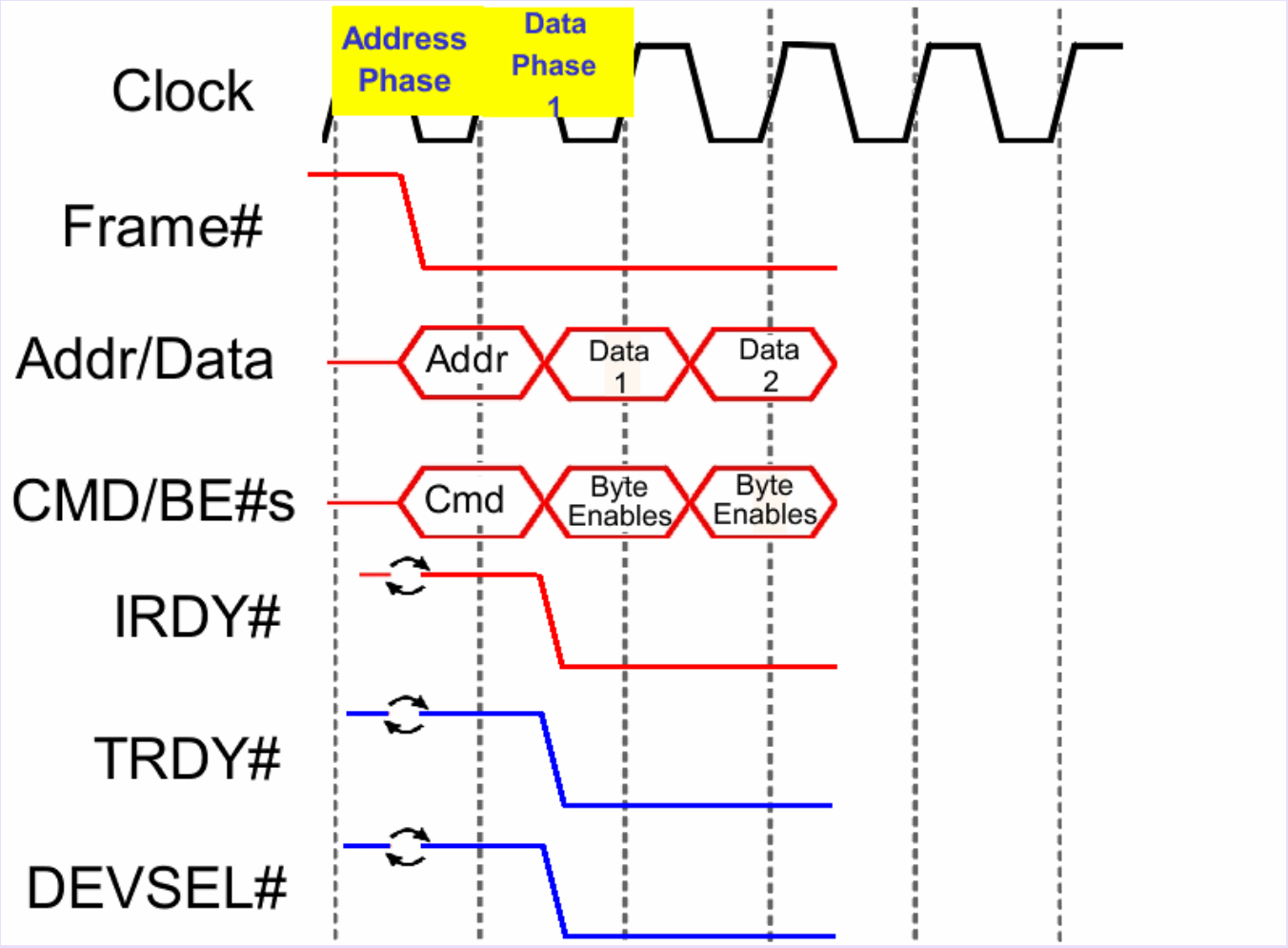


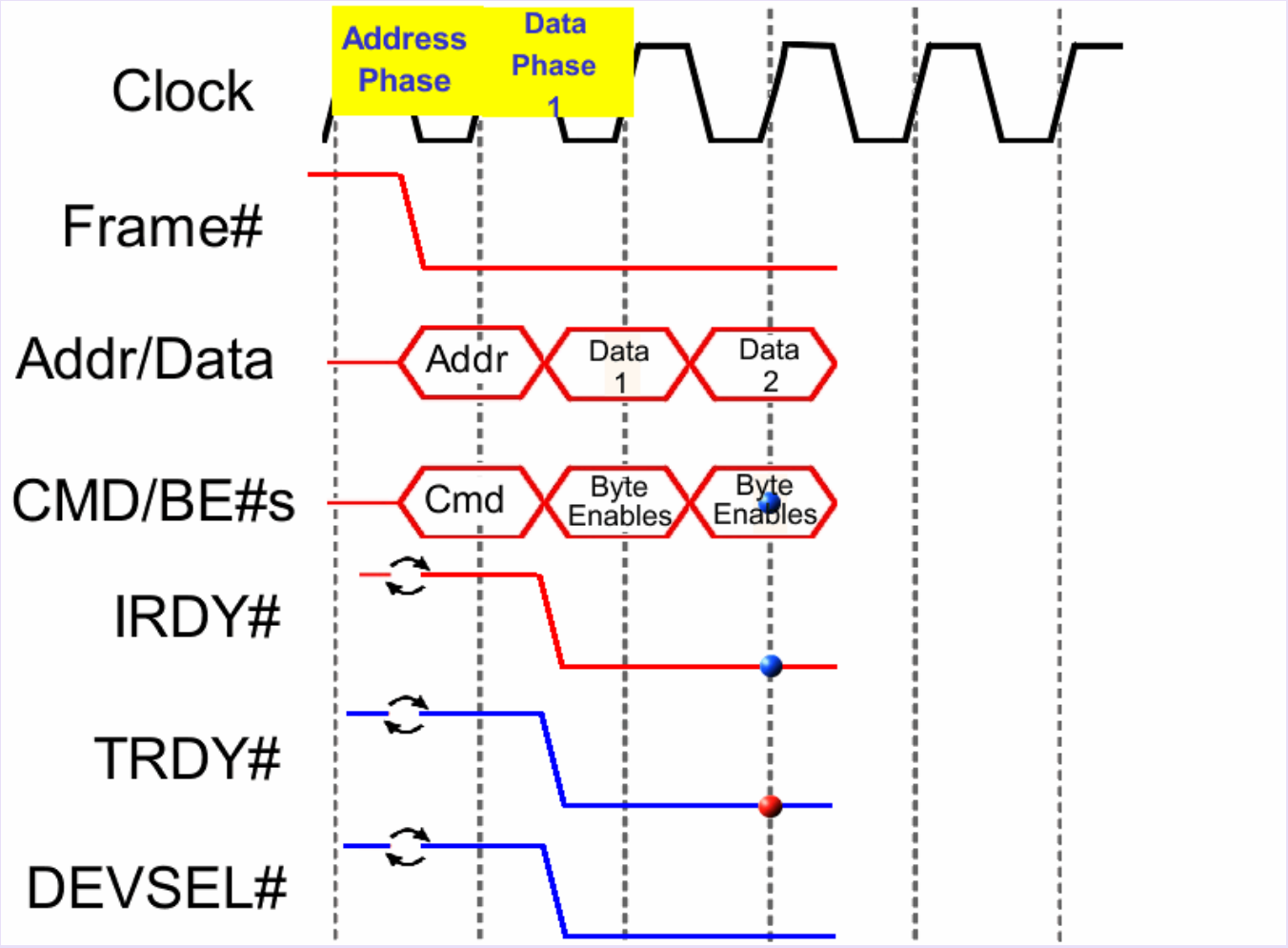


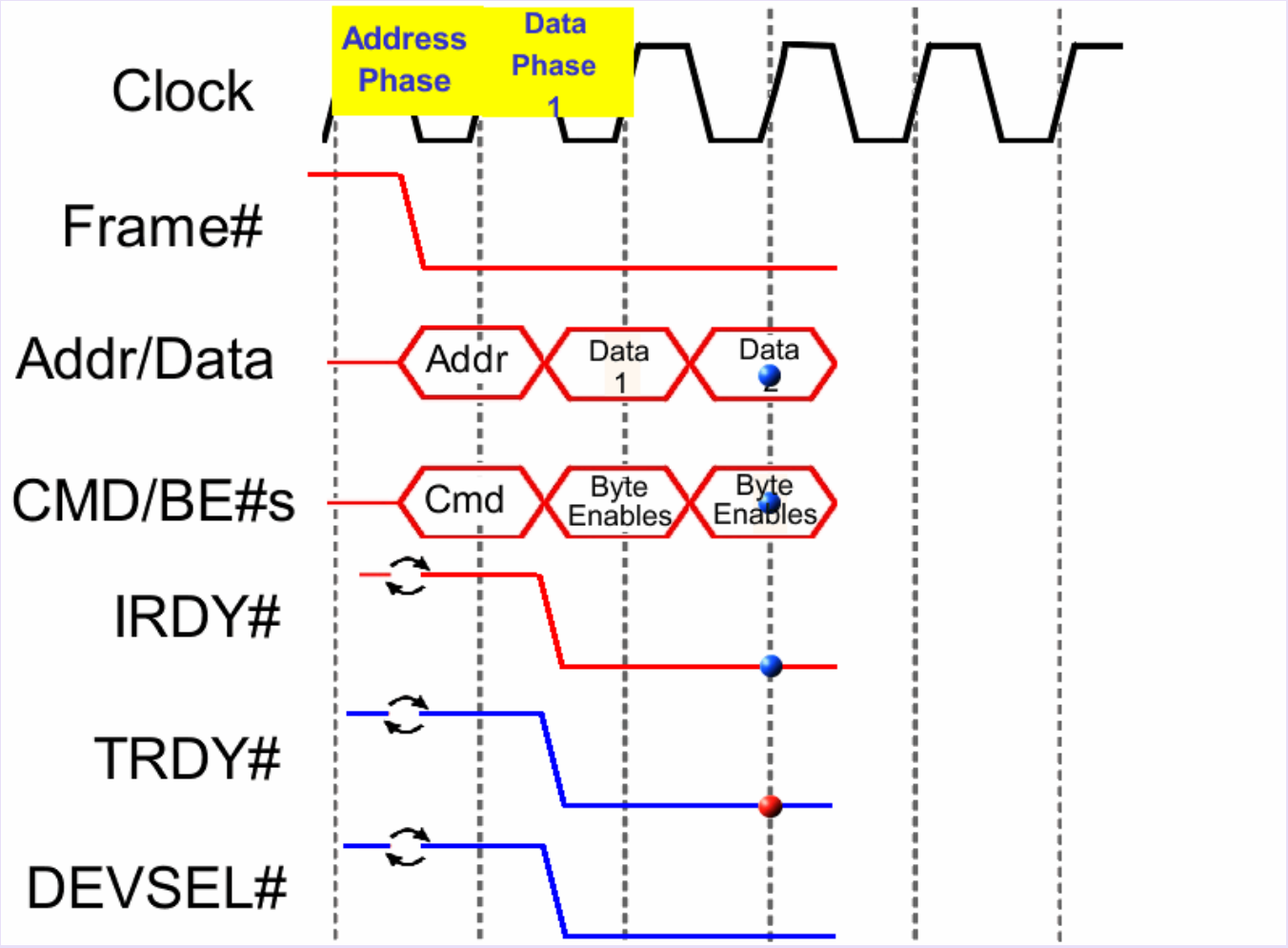


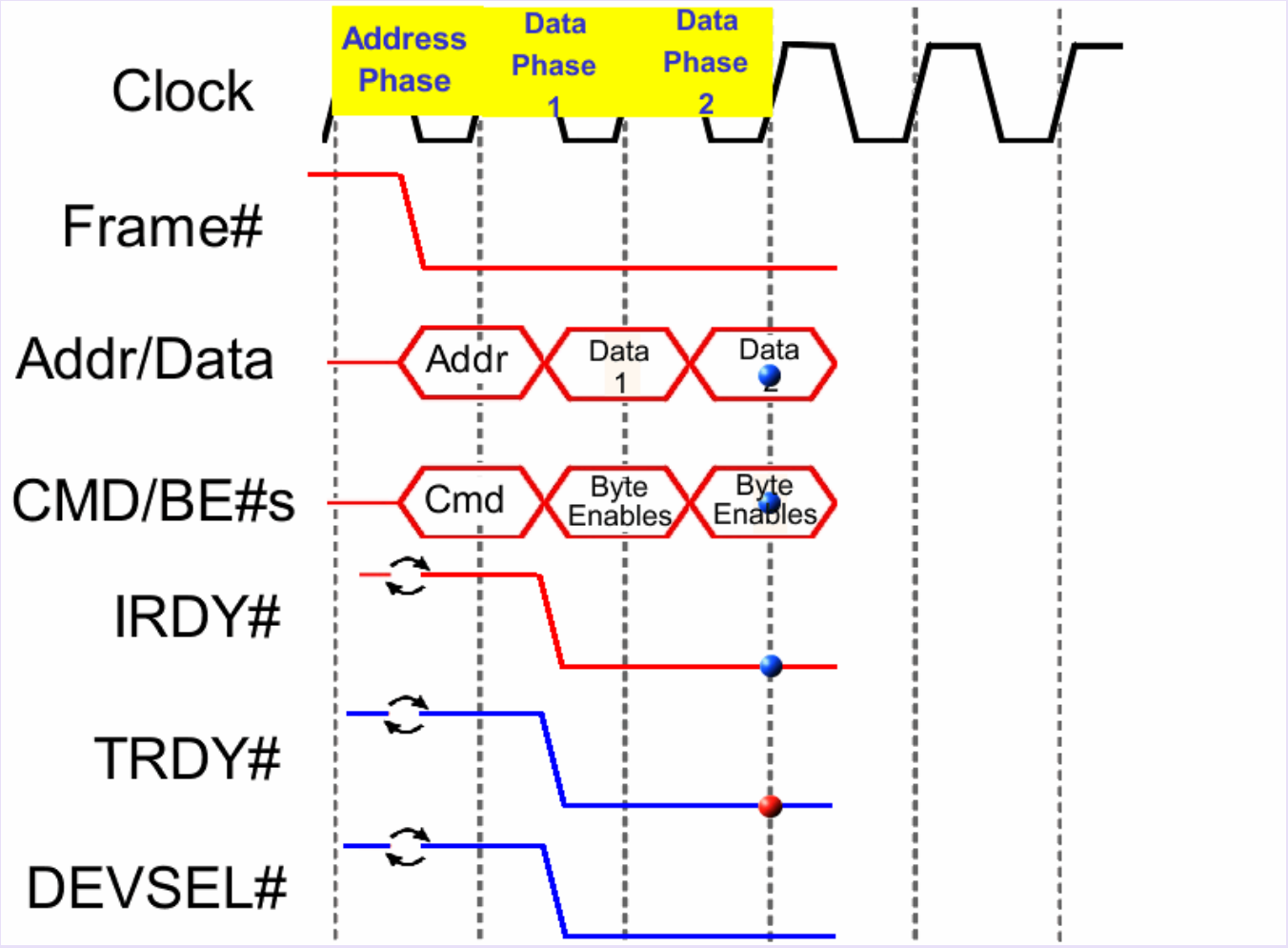




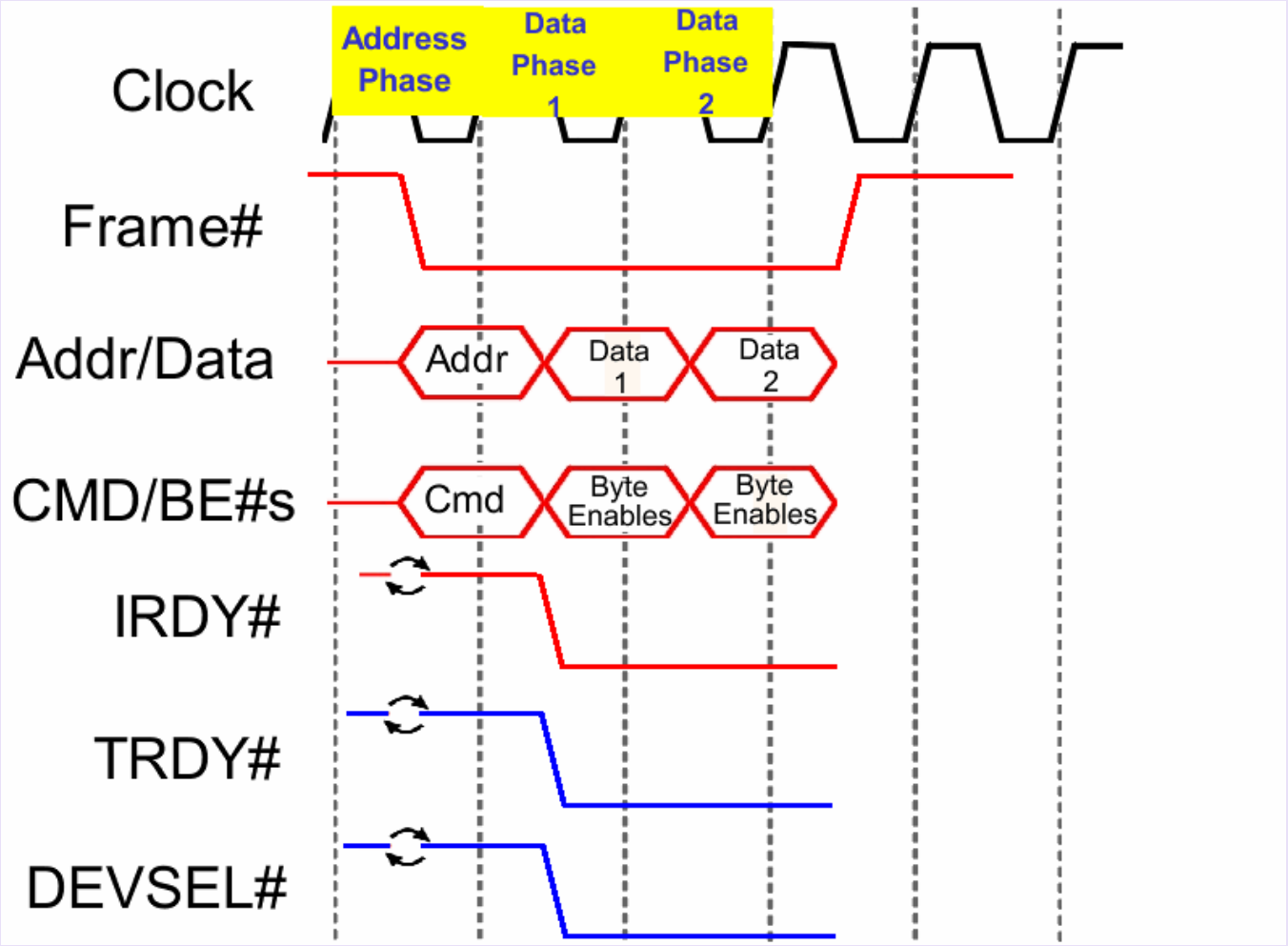


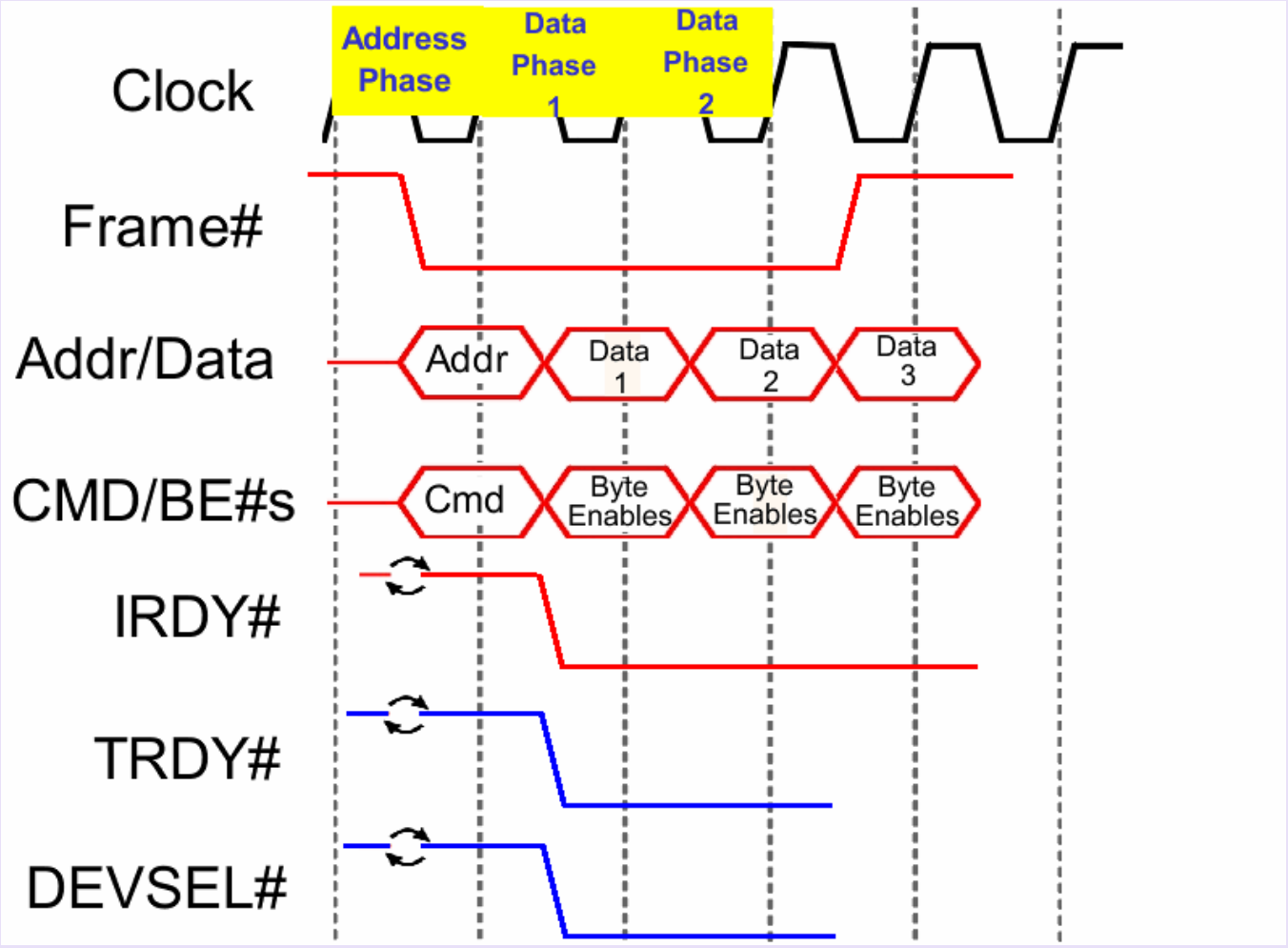


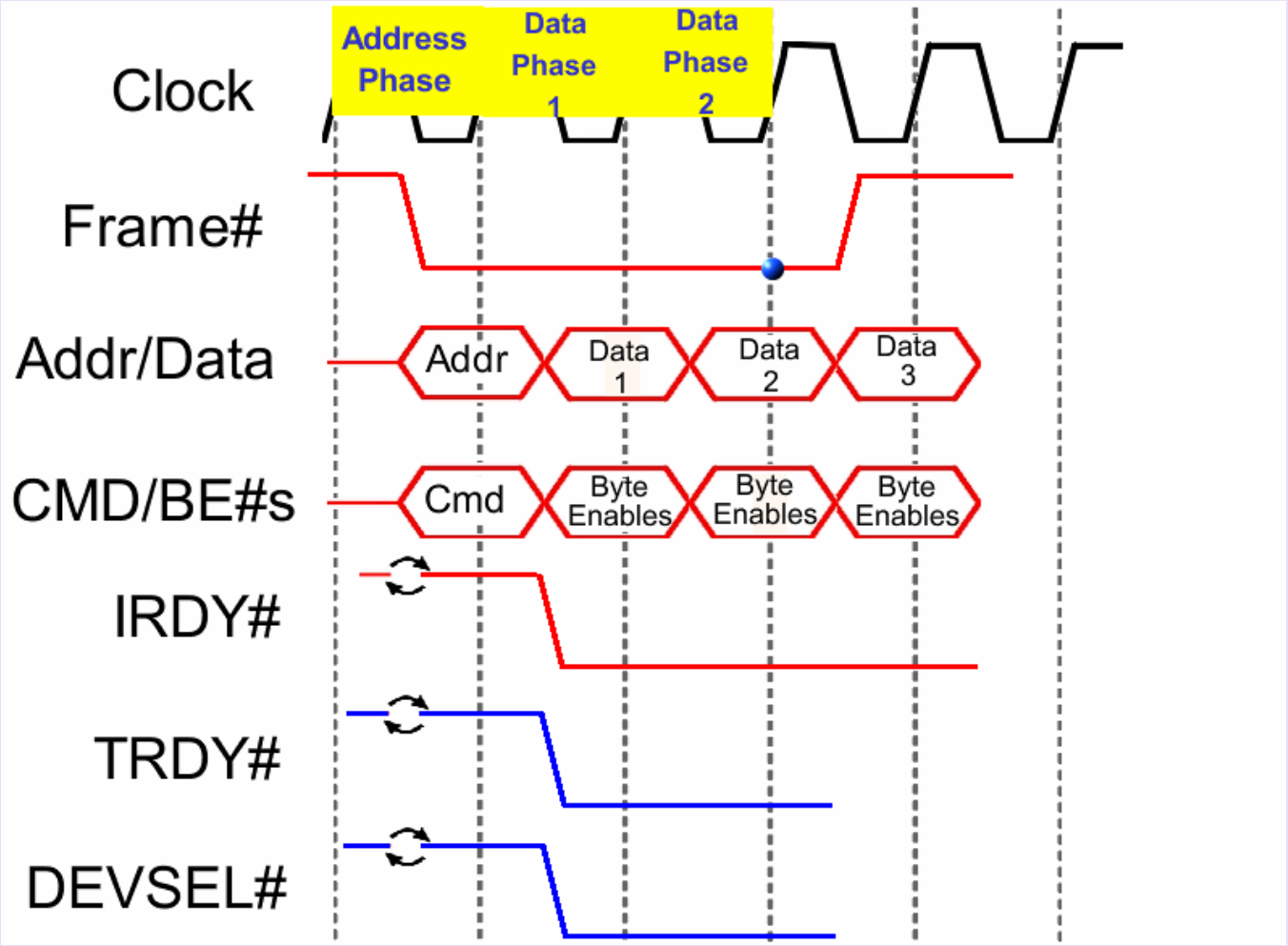


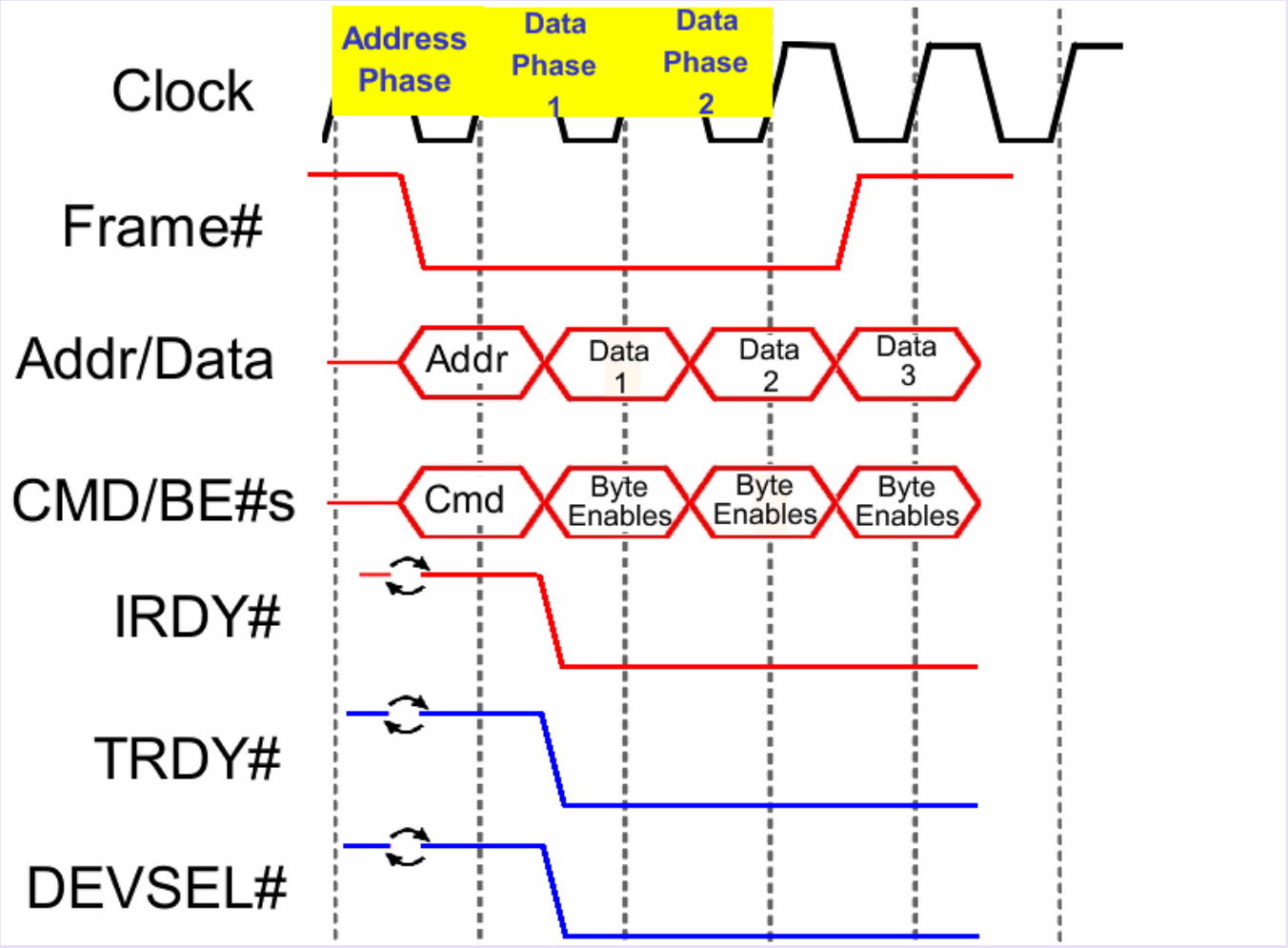


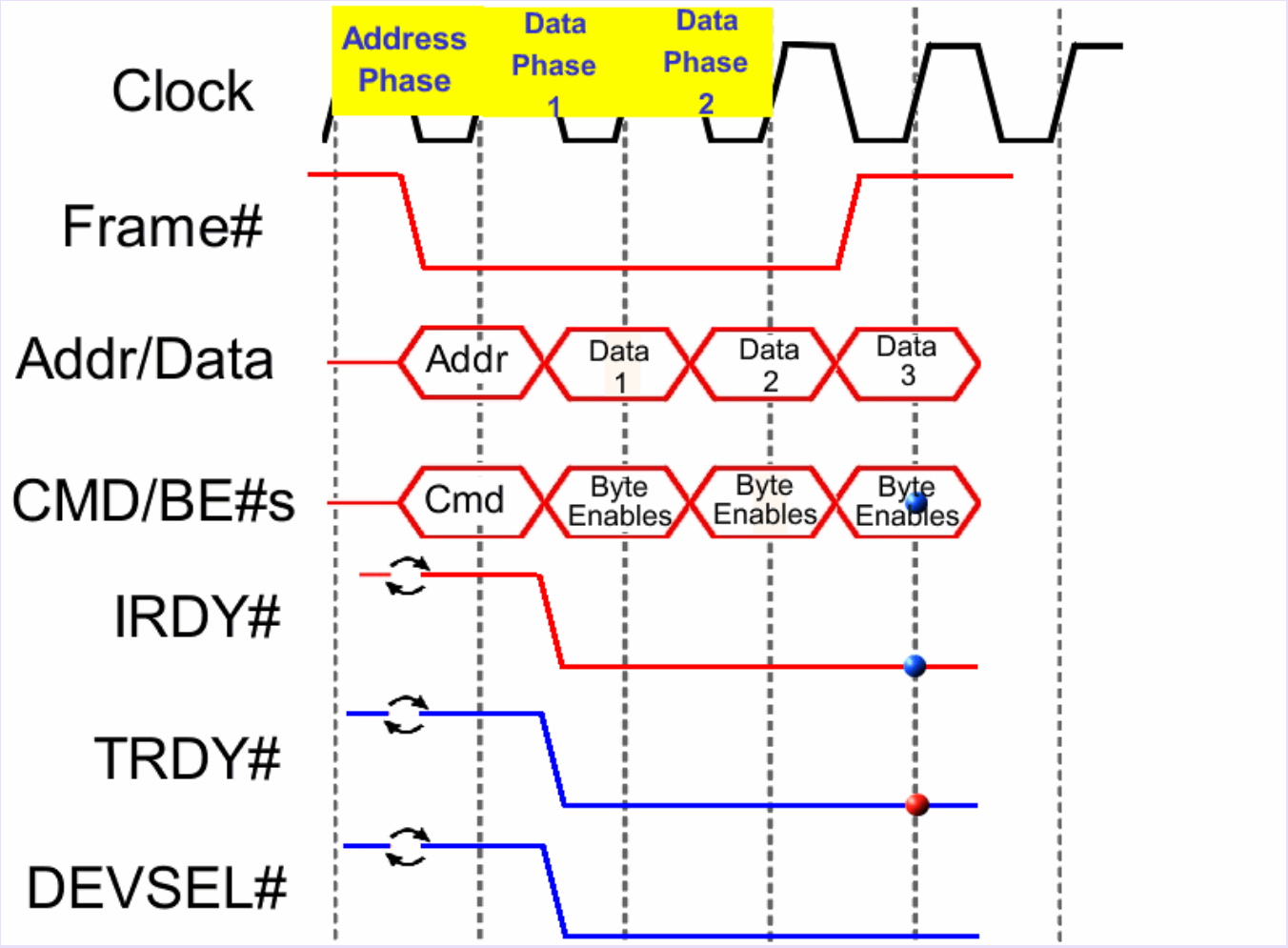
The Last Data Phase

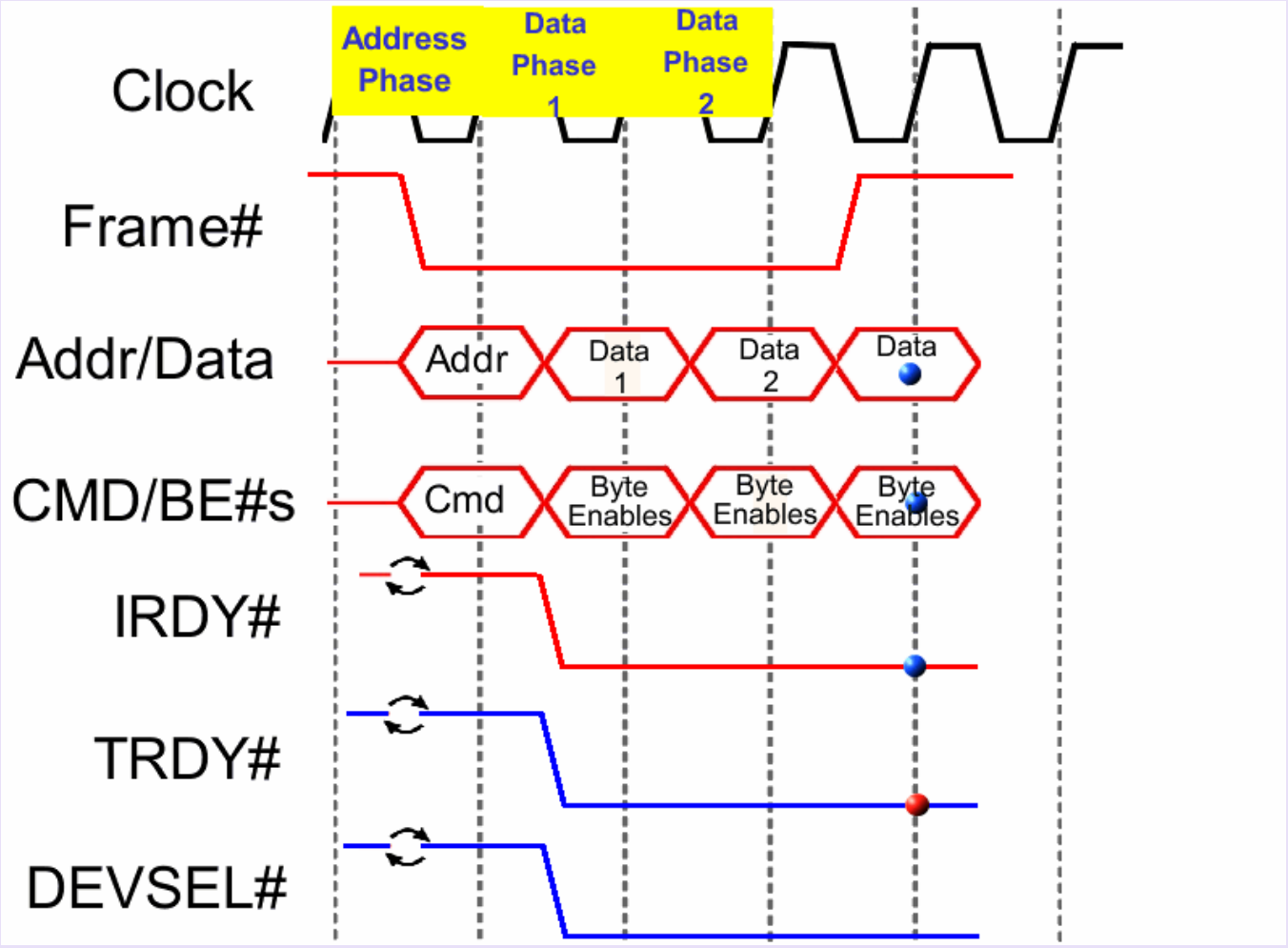


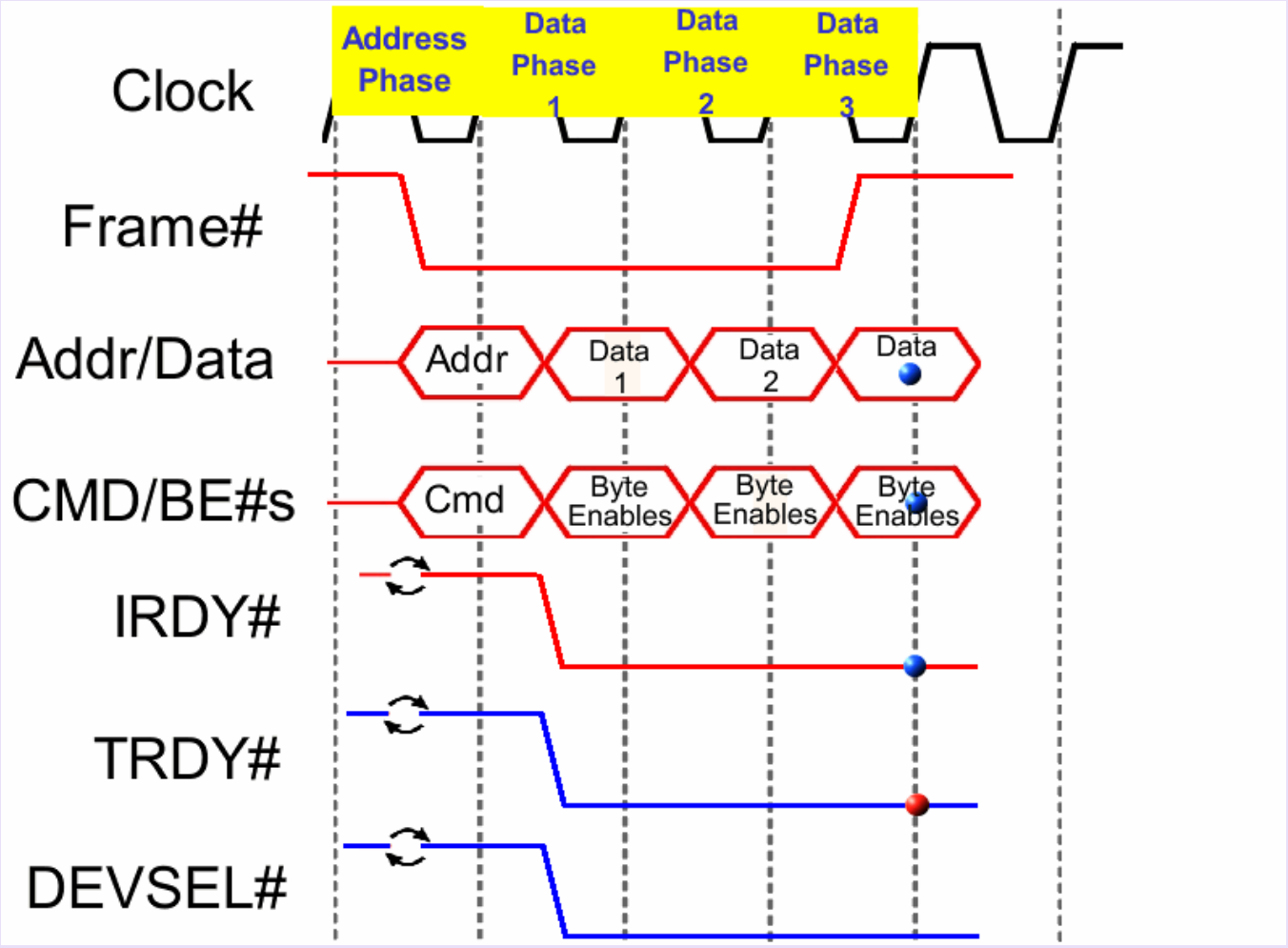


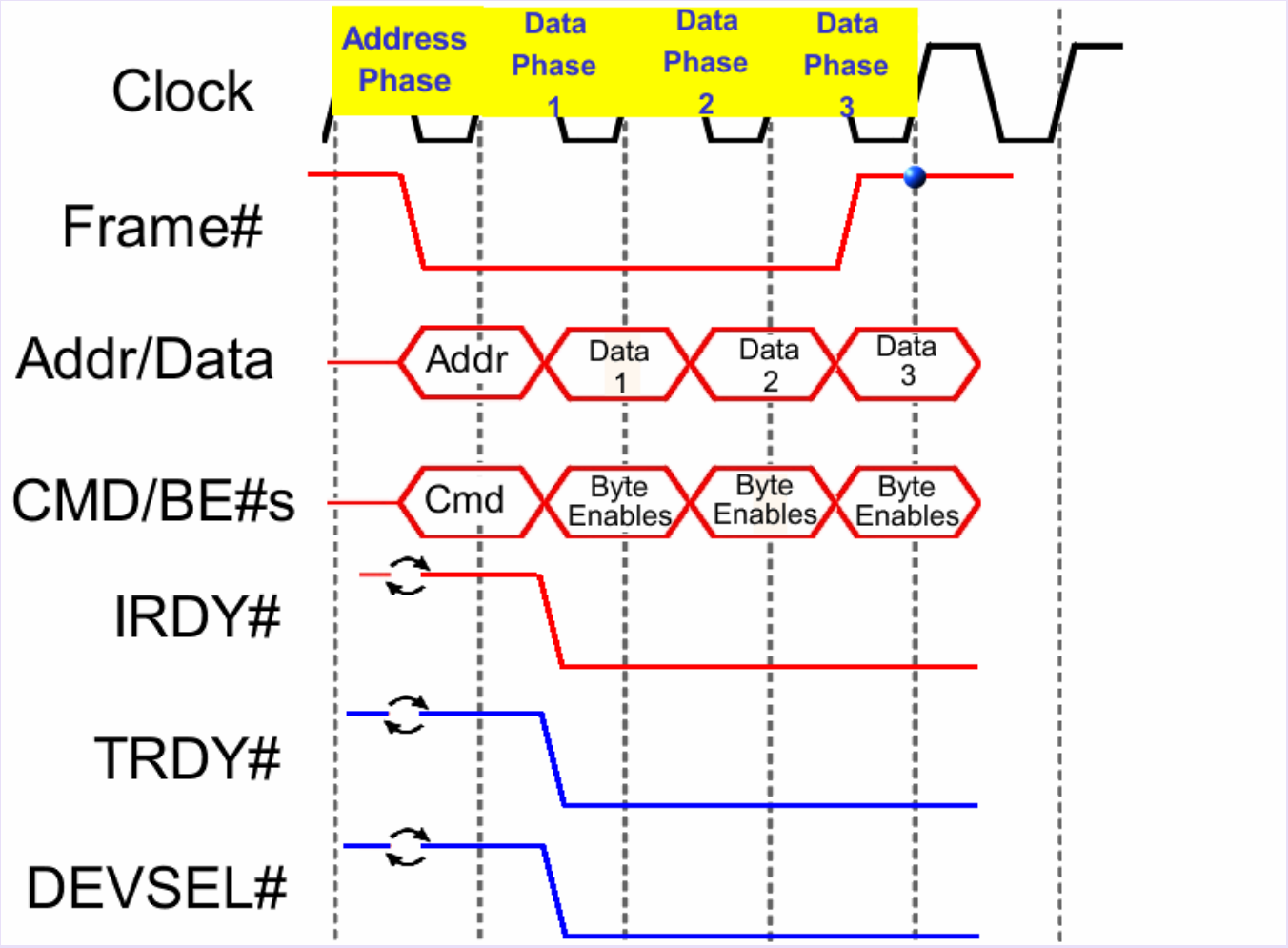


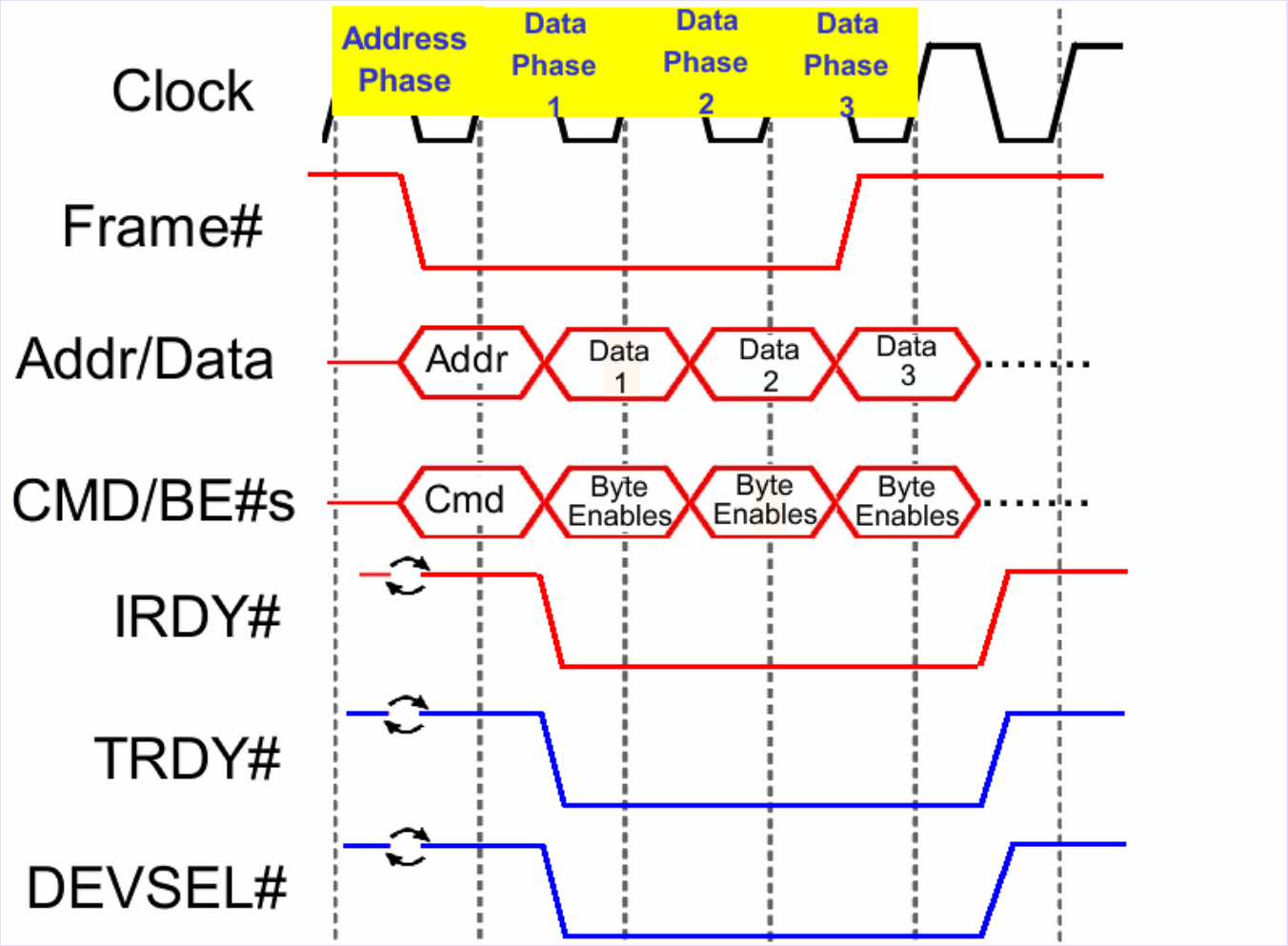


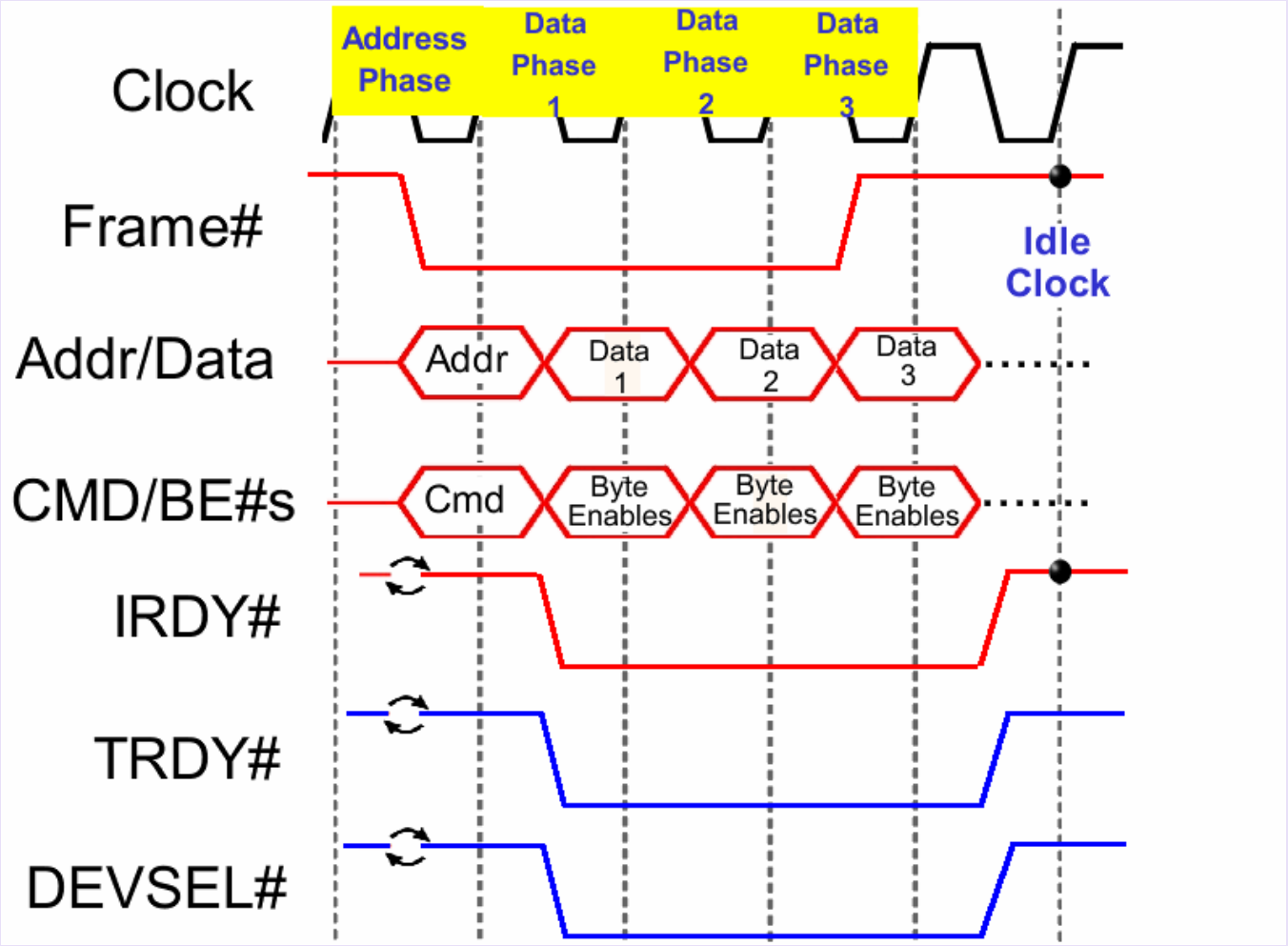




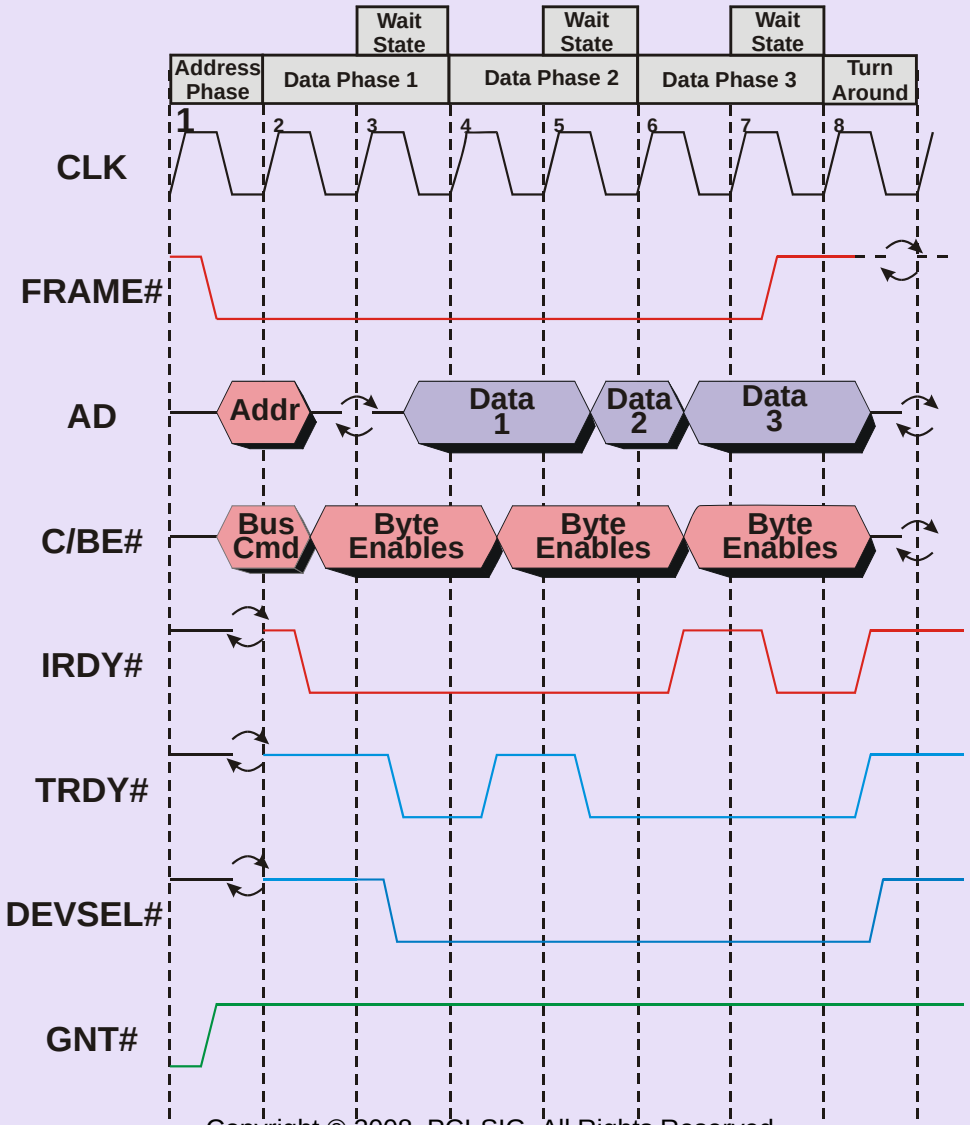




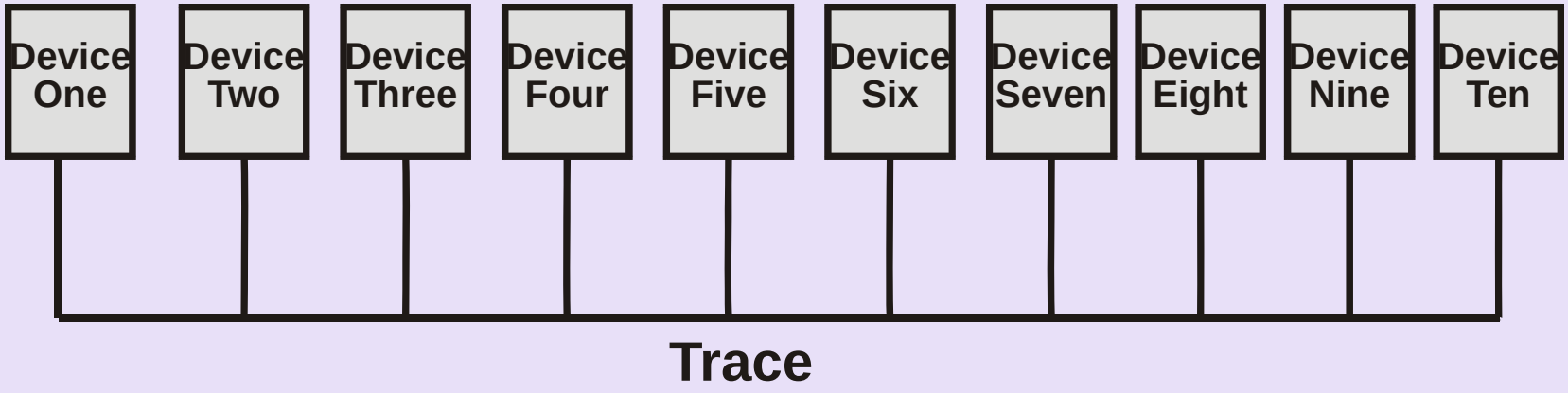


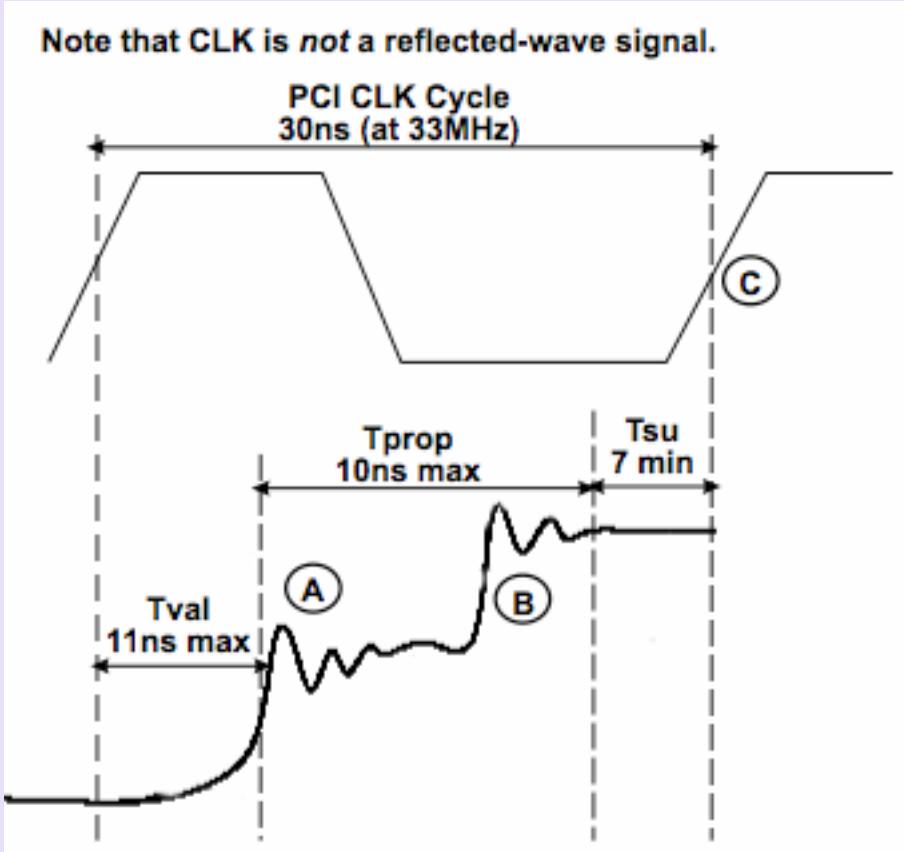


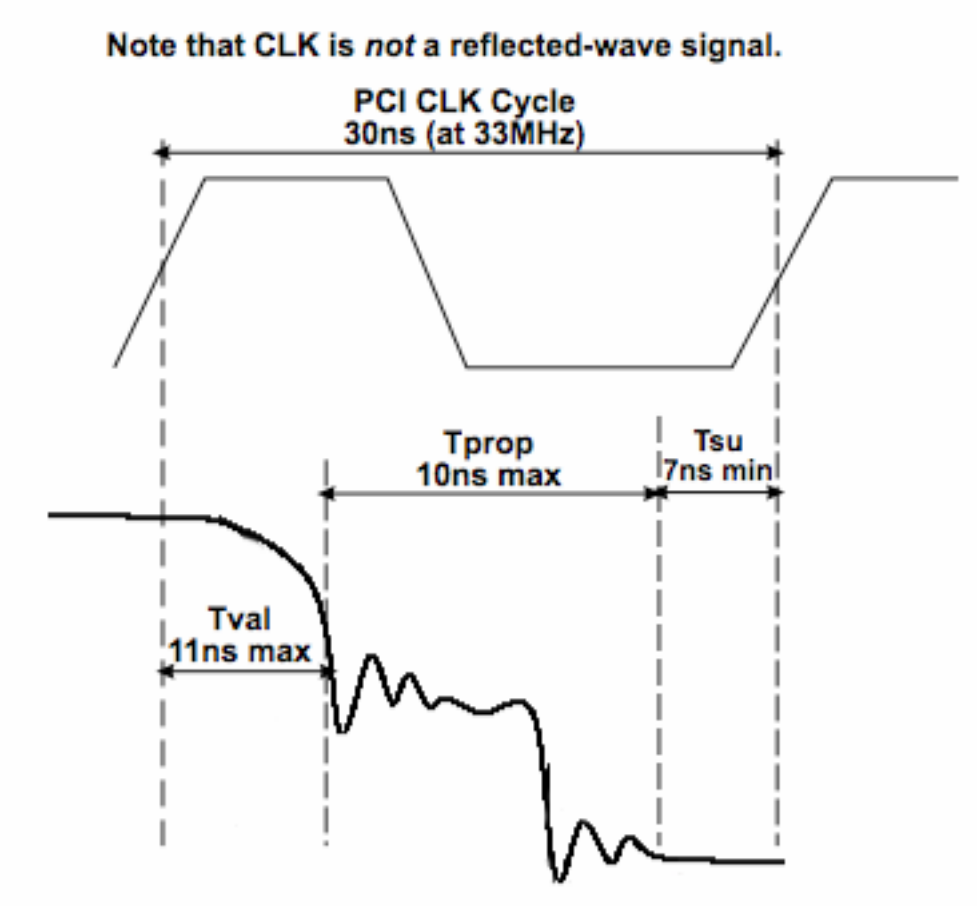
Memory Read Example



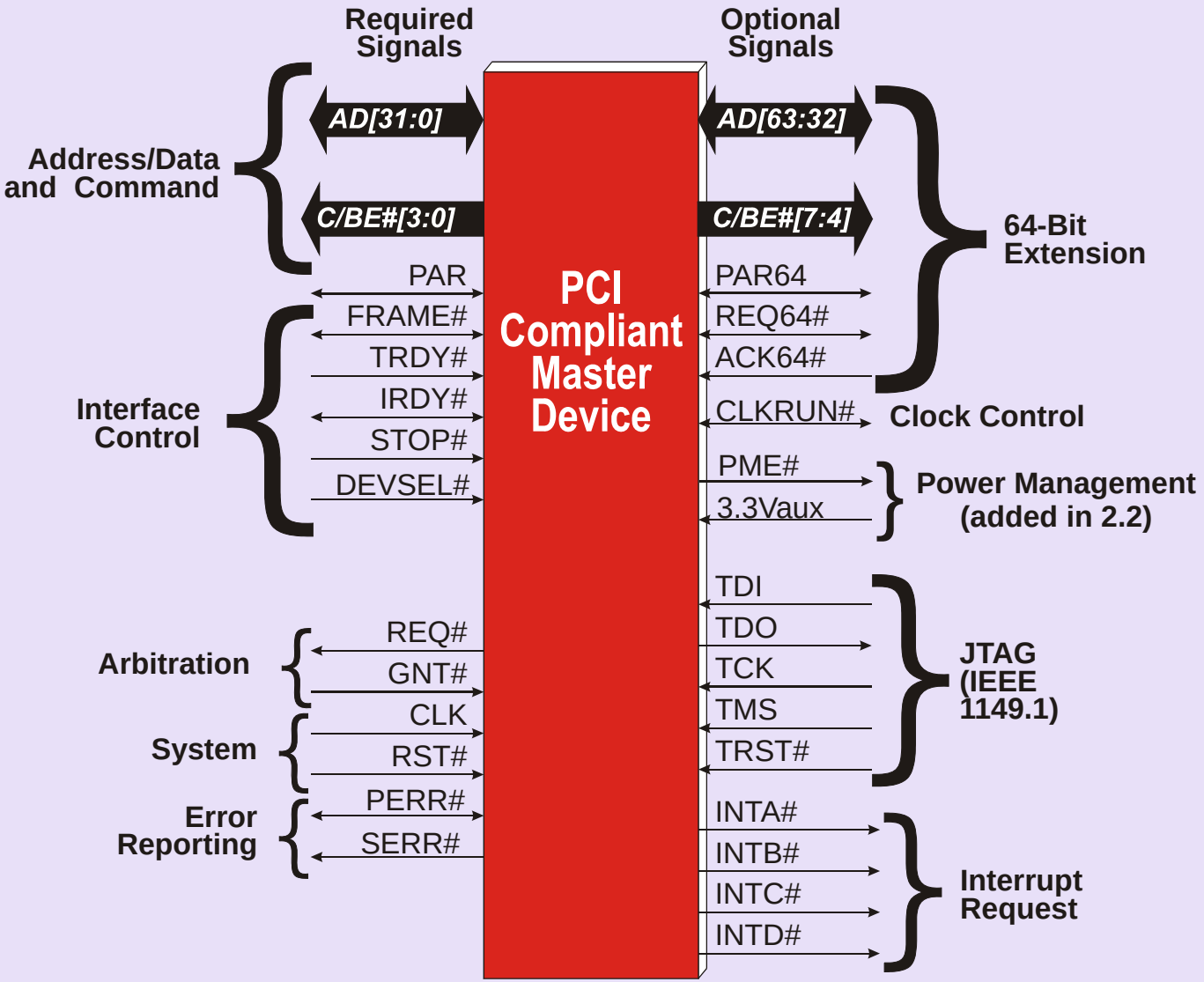
Reflected Wave Switching



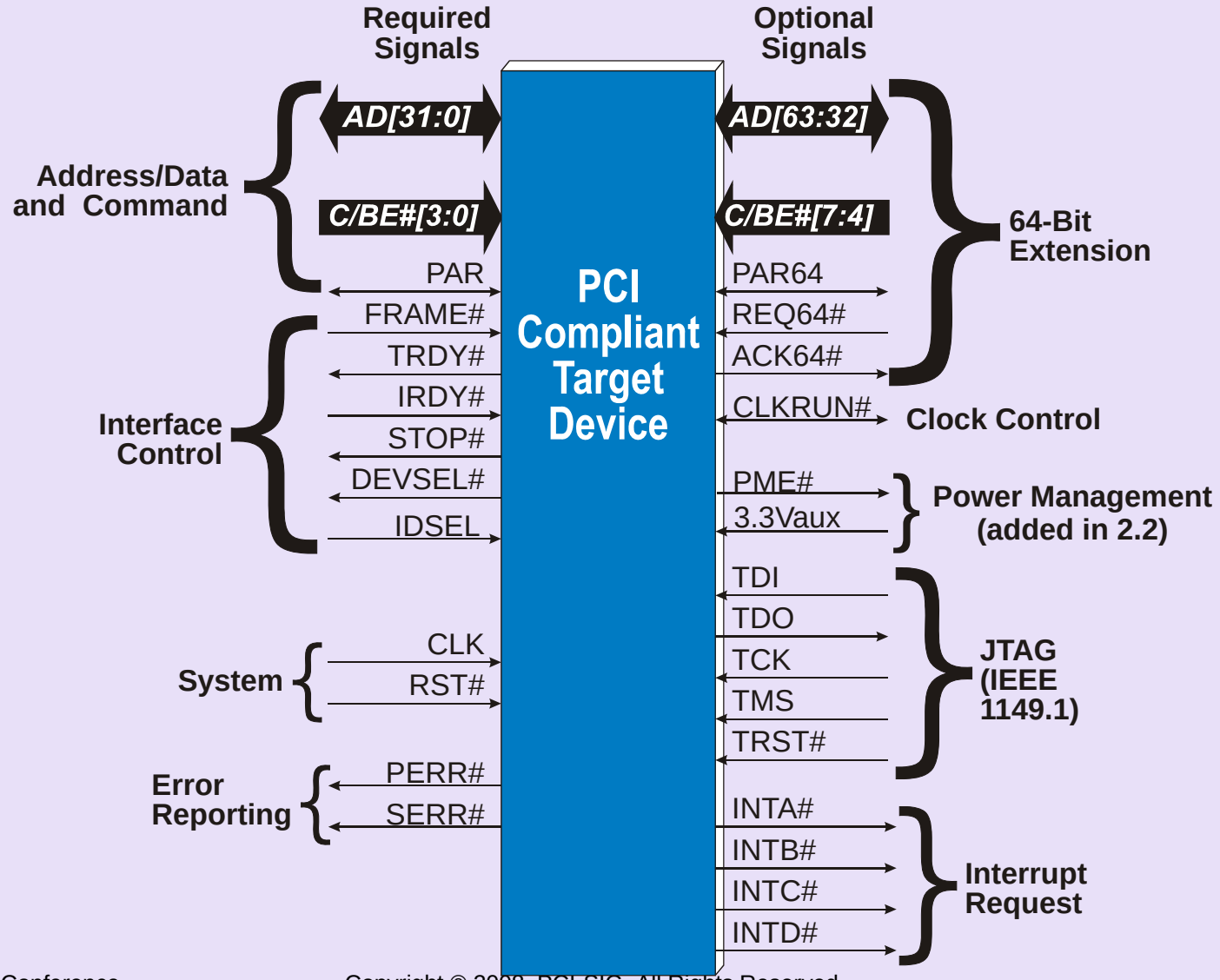




Bus Master-related Signals

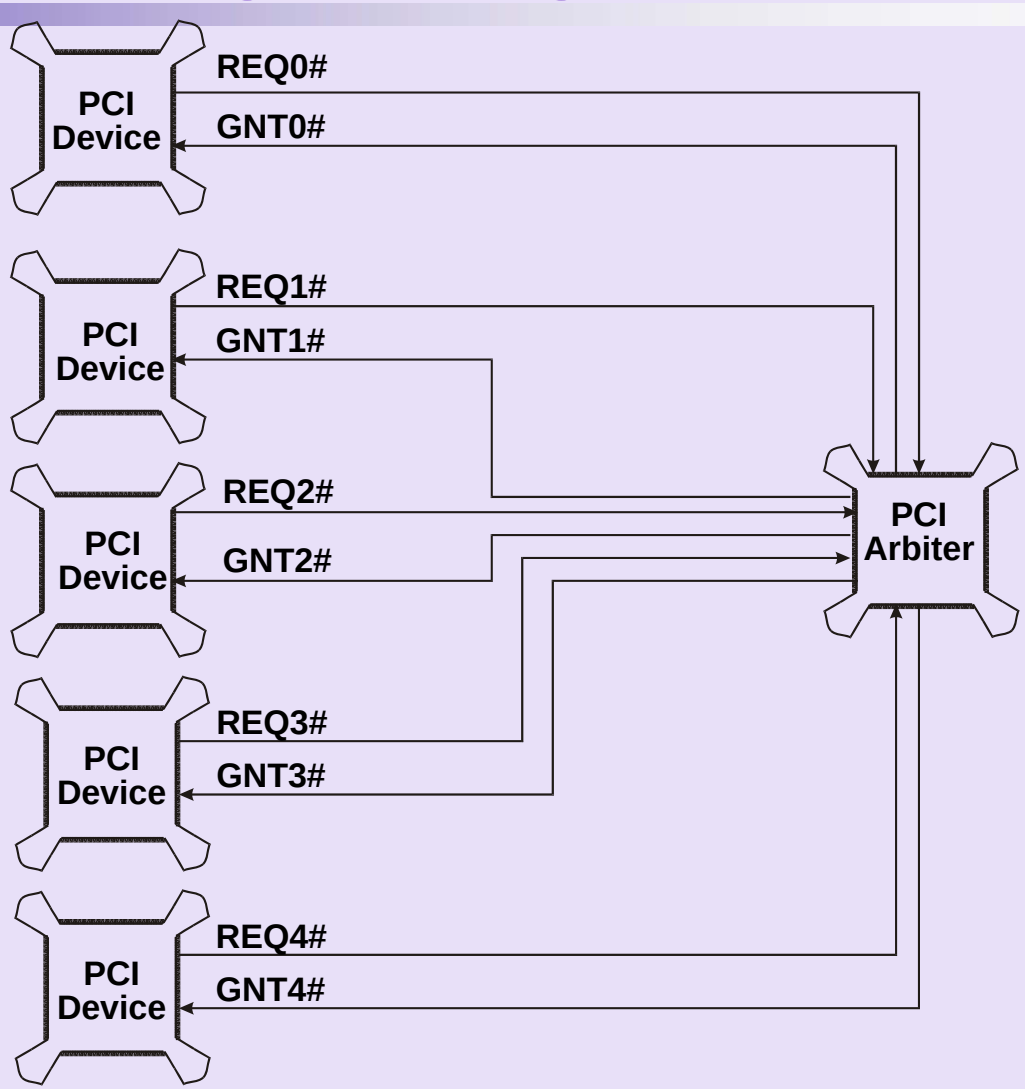


Target-related Signals



Arbitration Signaling

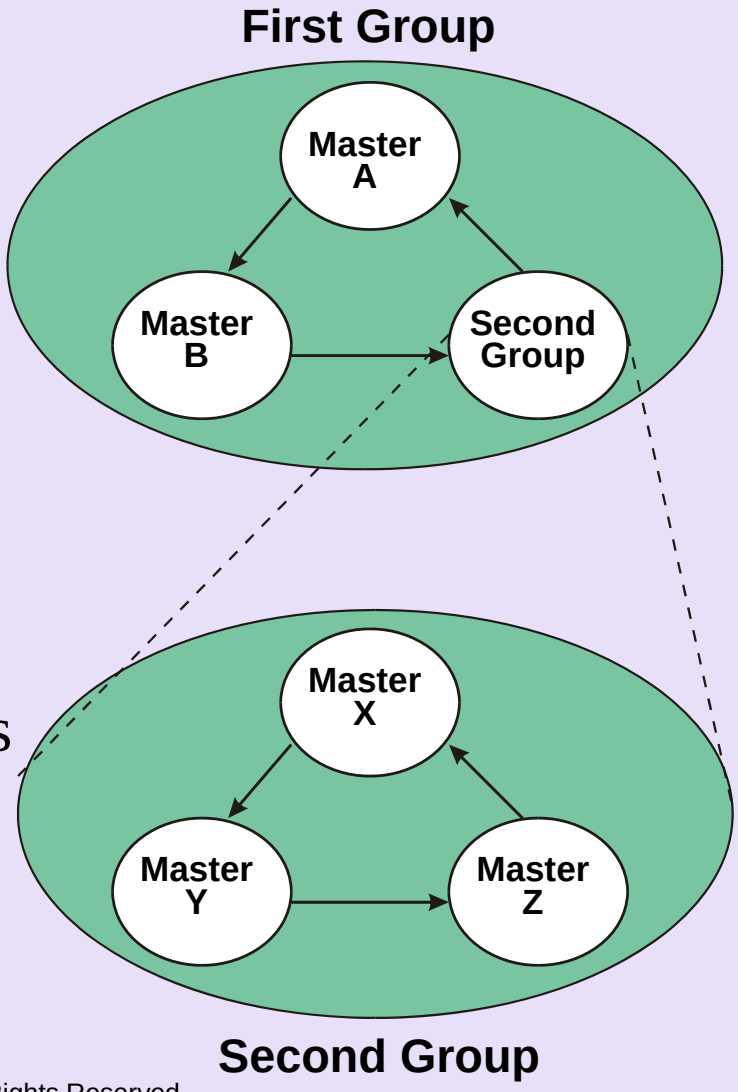
Hidden Bus Arbitration



Example Arbiter with fairness

First Group: Short Latency Devices

Second Group: Long Latency Devices

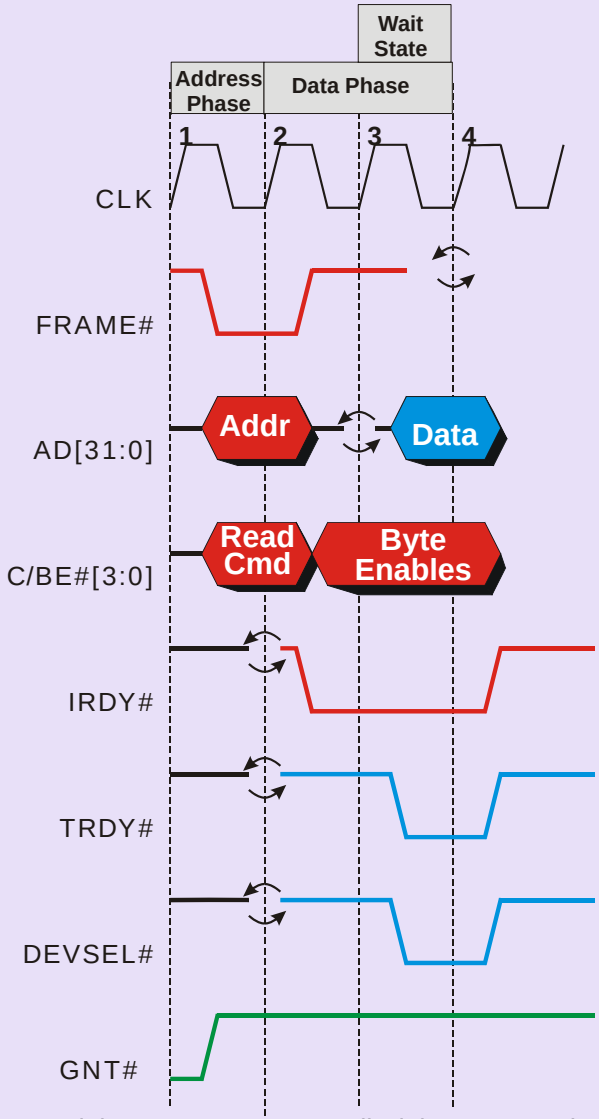


The Command Set

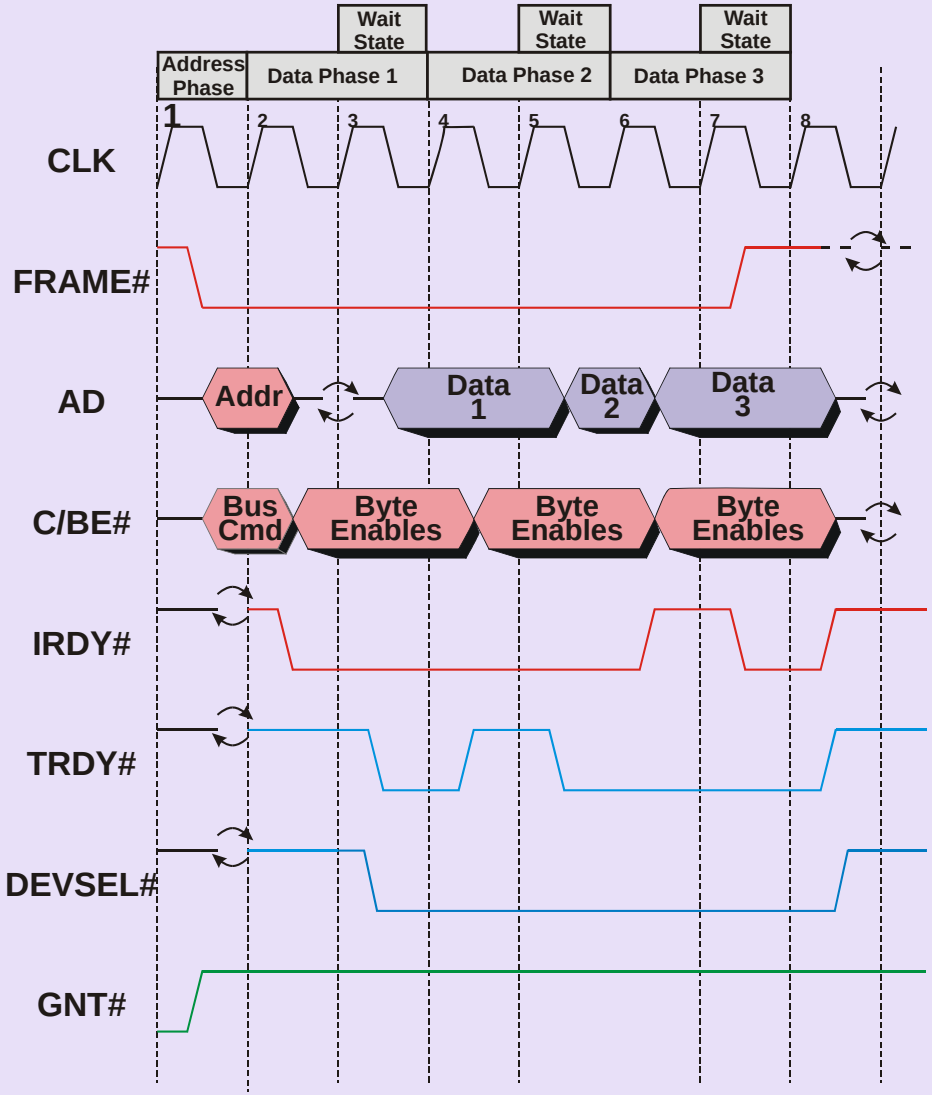
Table 1-1: PCI Command Types

C/BE[3:0]# (binary)	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write-and-Invalidate

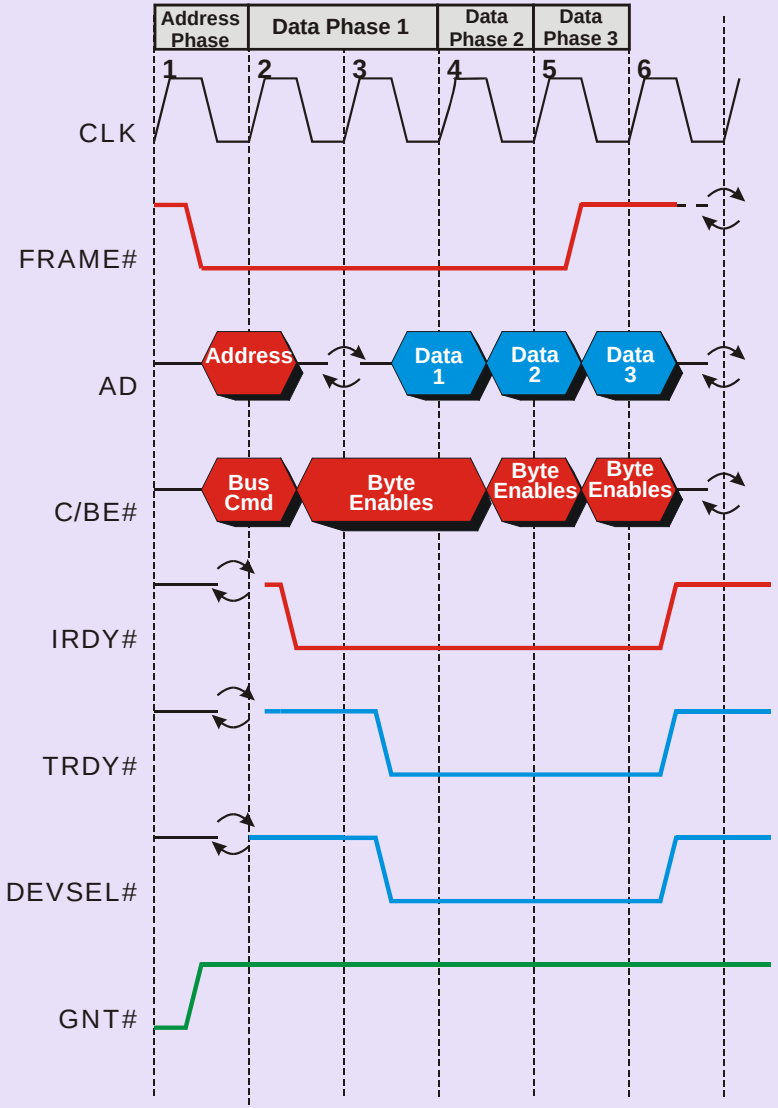
Single Data Phase Read



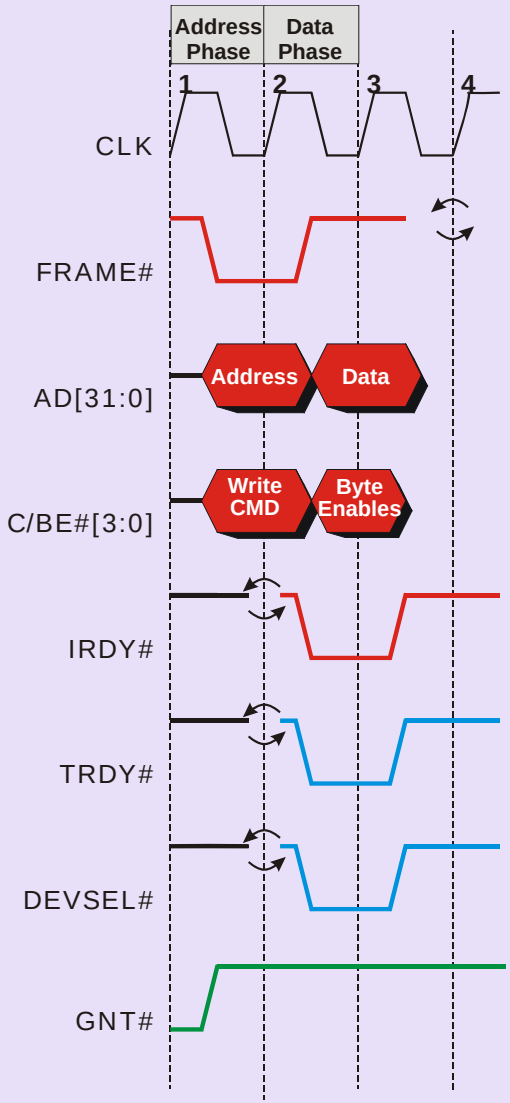
Example Burst Read



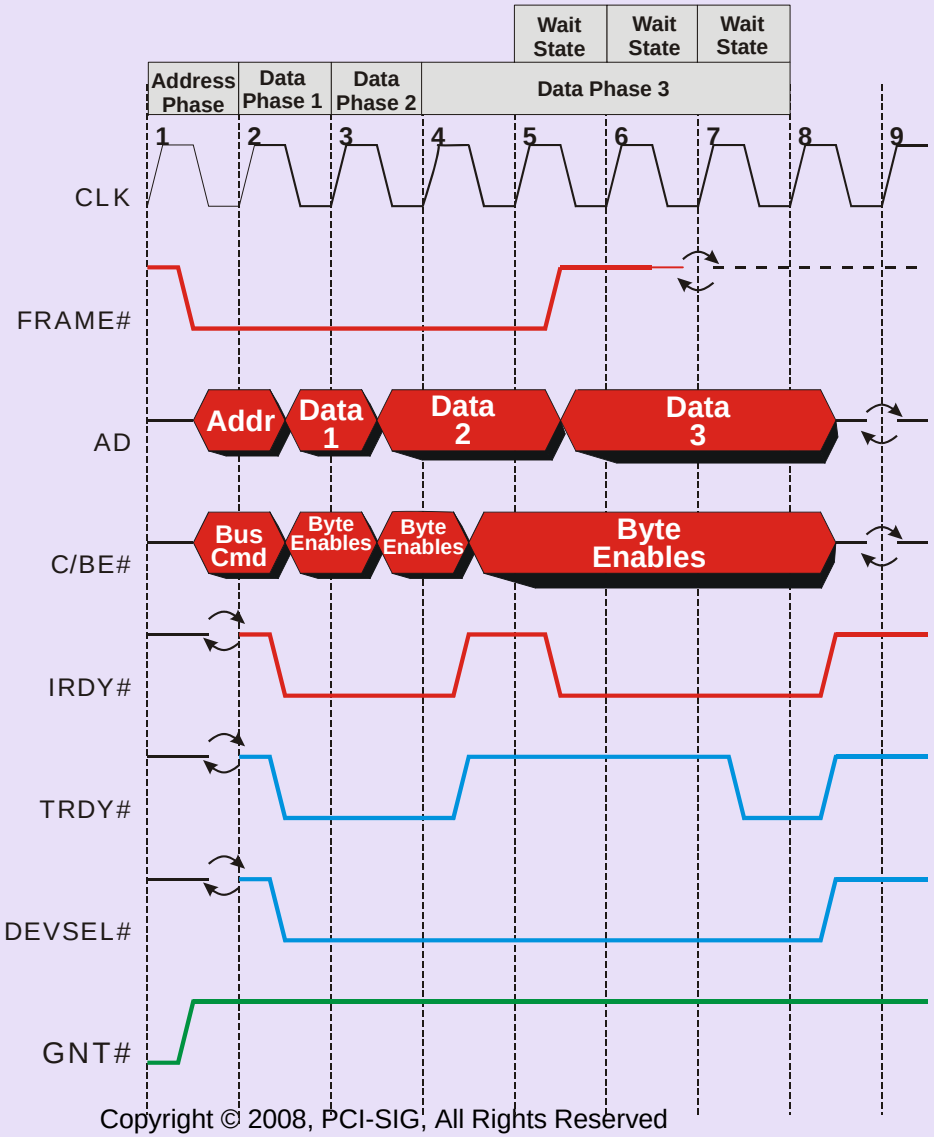
Optimized Burst Read



Single Data Phase Write

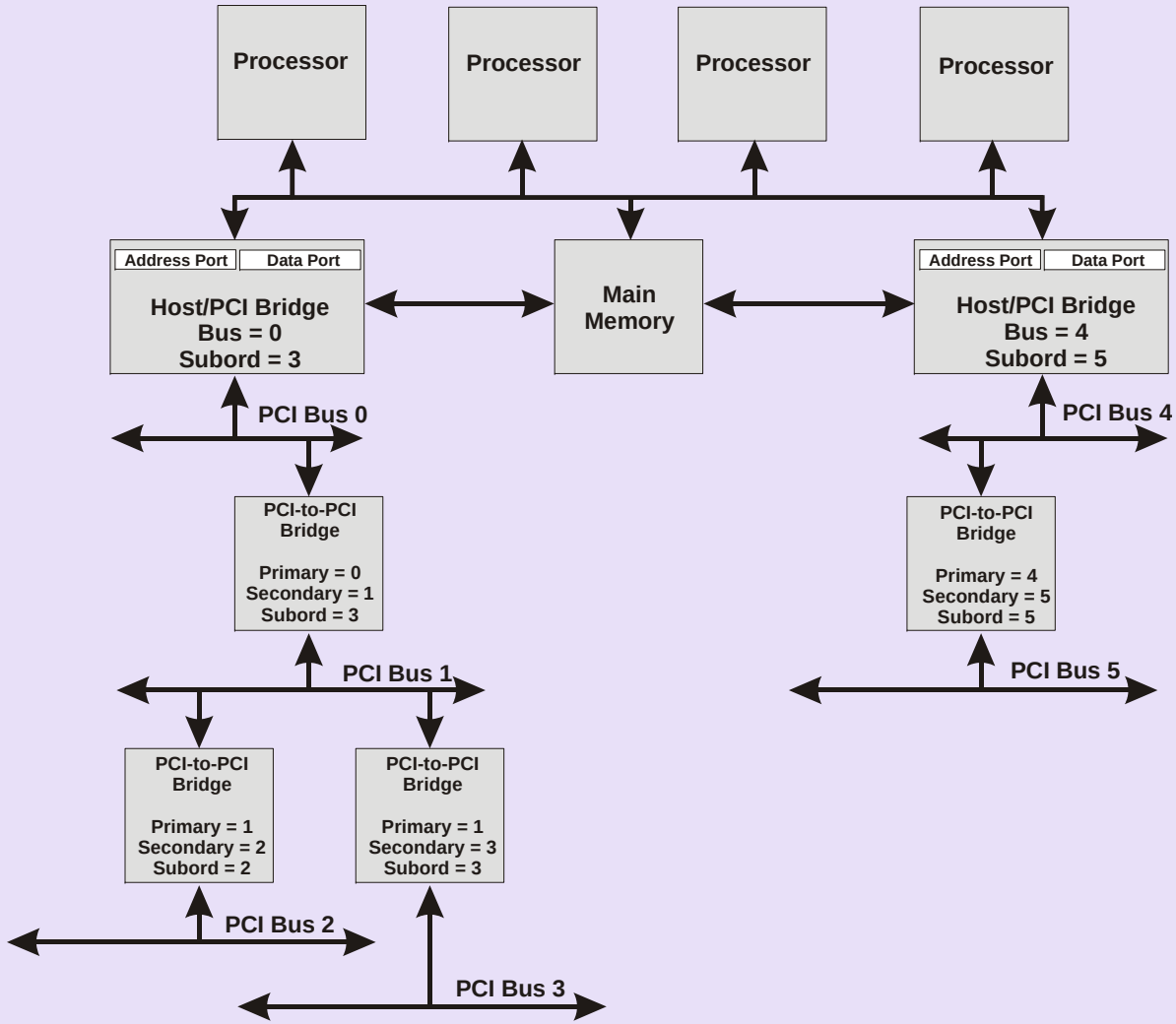


Burst Write



Configuration Transactions

- Each PCI device must be identified and configured.
- Devices are identified by:
  - ✓ Bus number on which they reside
  - ✓ Device number
  - ✓ Function number within the device
  - ✓ Byte location with 256 Bytes of config. space



Configuration Address Generation (mechanism #1)

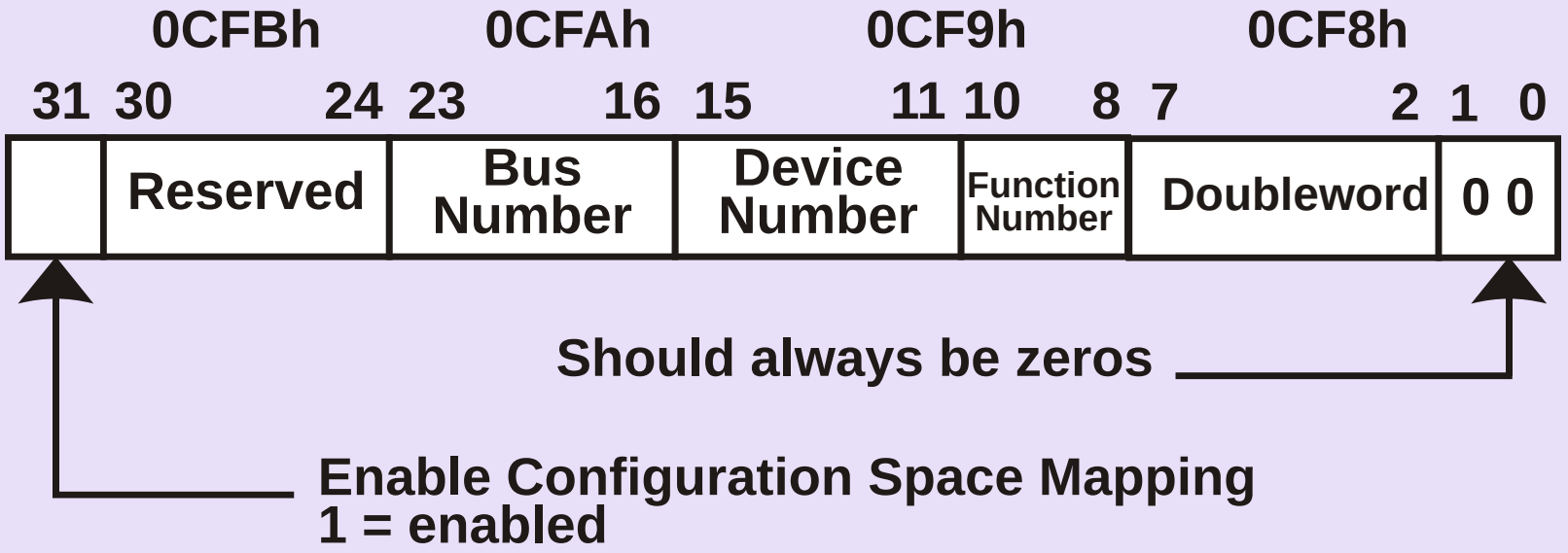
Configuration Address Register

Writes to the Configuration Address Register
Identifies configuration location to be accessed.

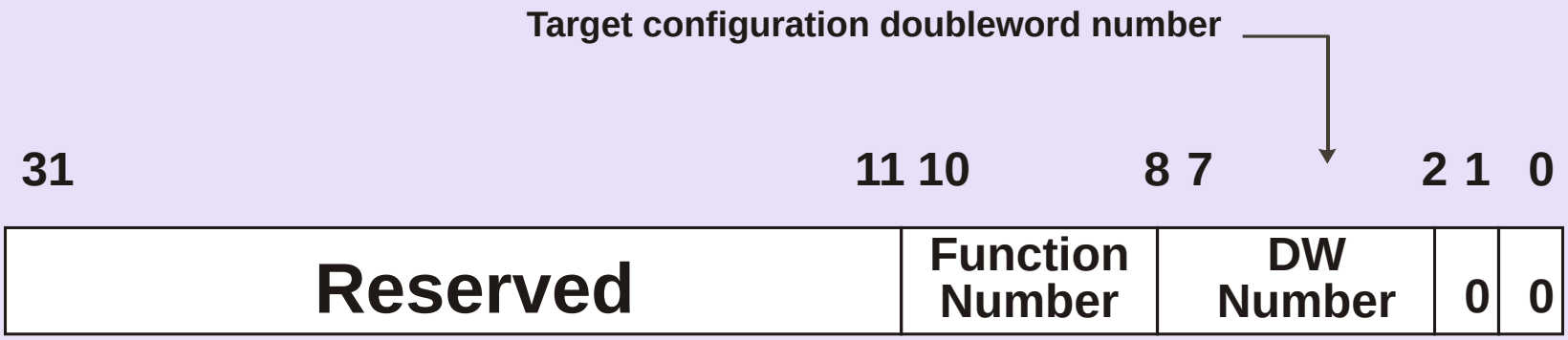
Configuration Data Register

Reads from or Writes to the Configuration Data Register
Causes a configuration read or write transaction to be Performed.

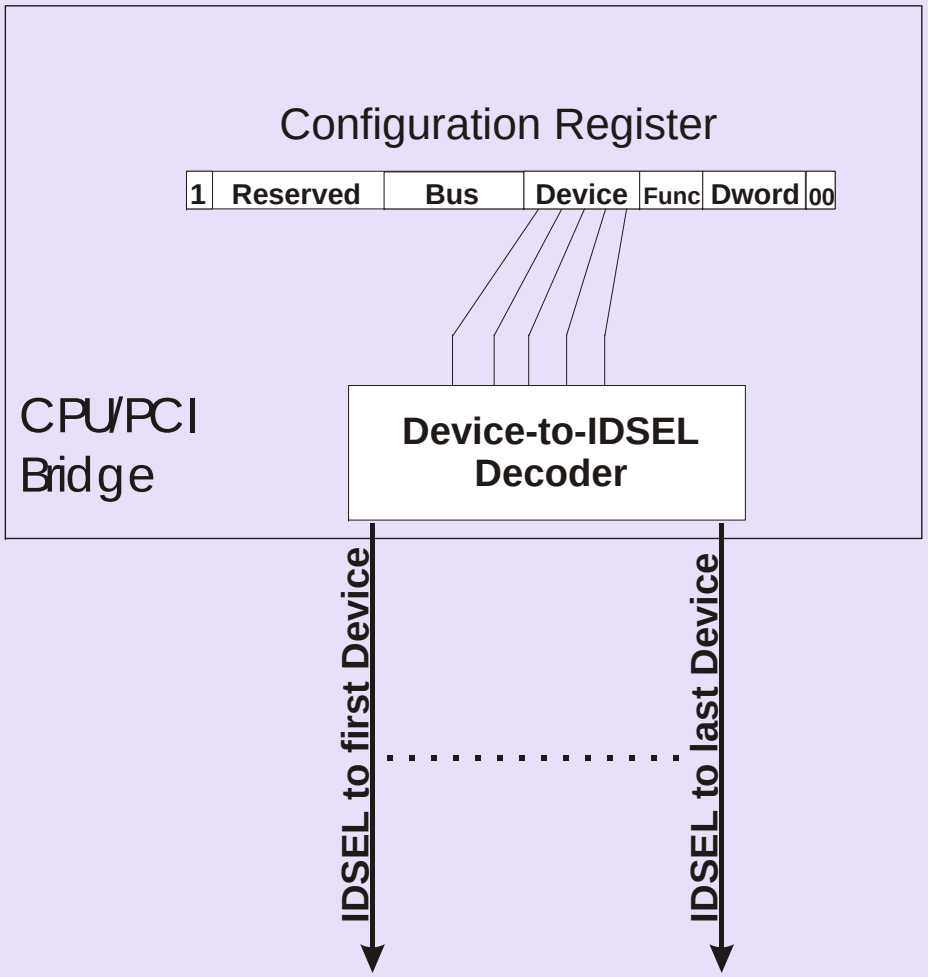
Configuration Address Registers



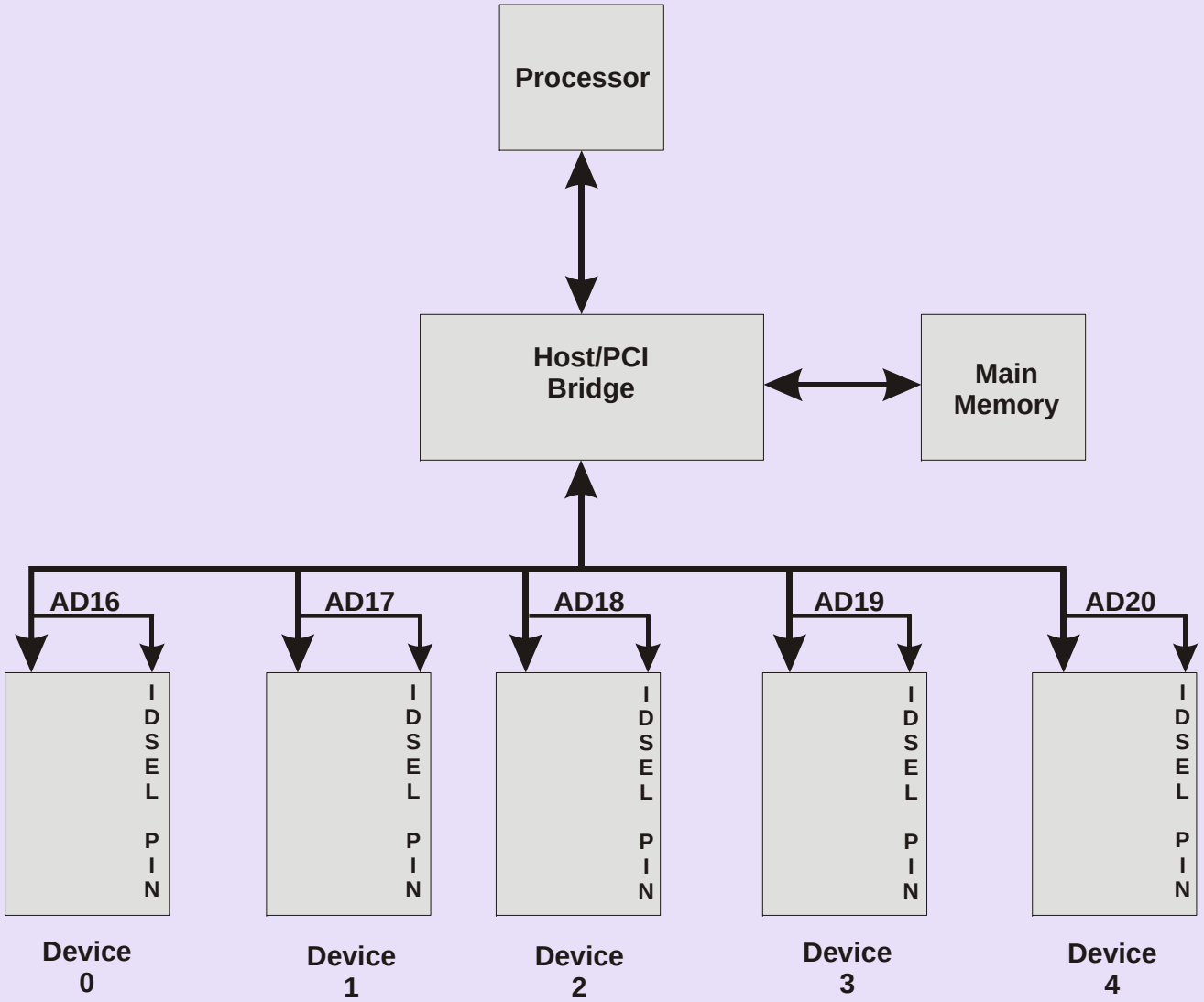
Config. Cycle Address Bus Contents



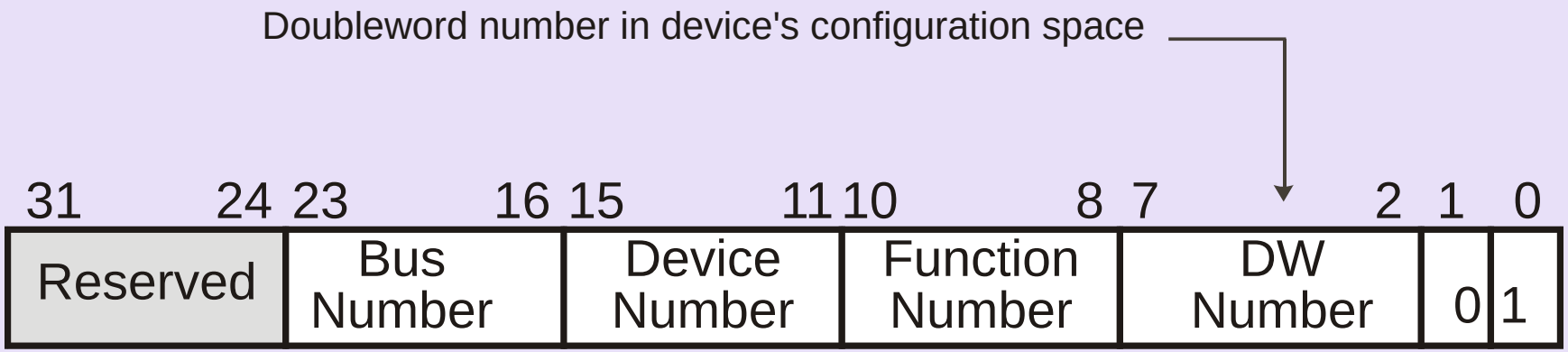
IDSEL Generation



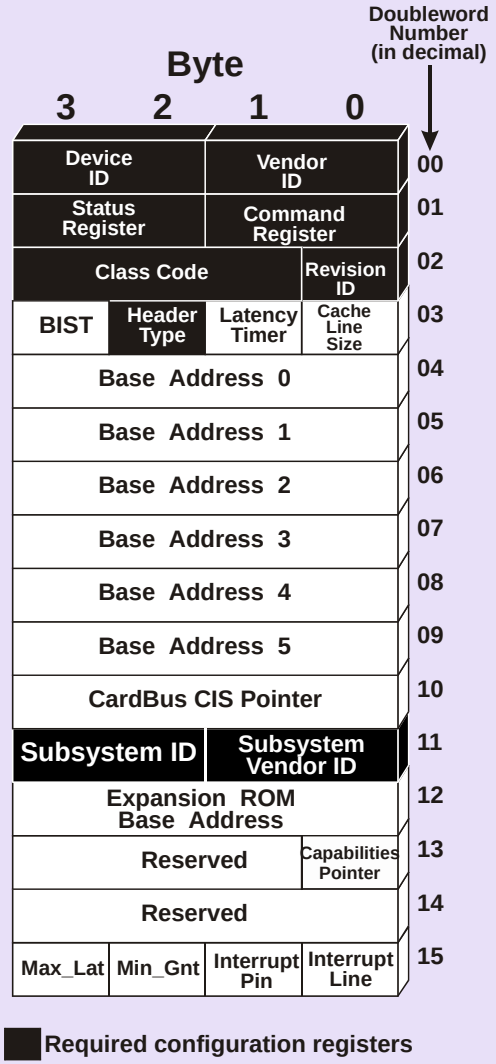
IDSEL Generation



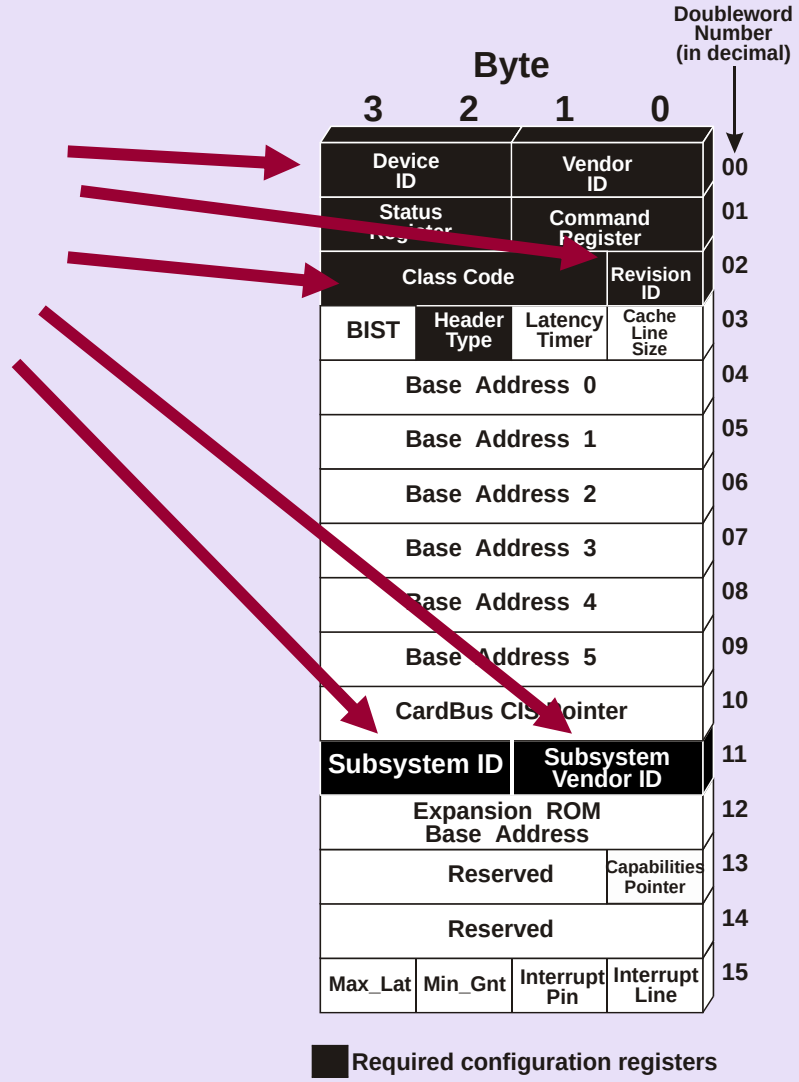
Type 1 Configuration Transactions



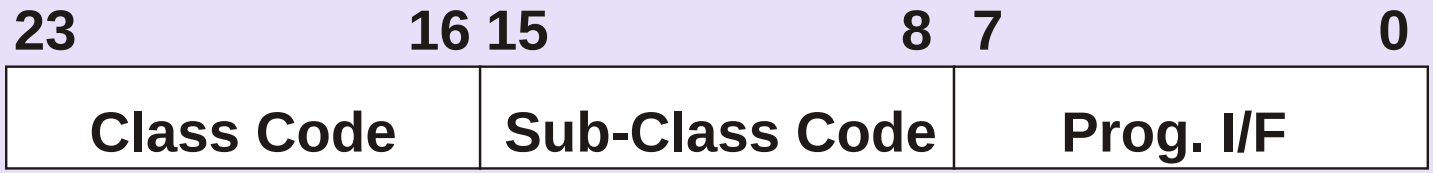
Header Type Zero



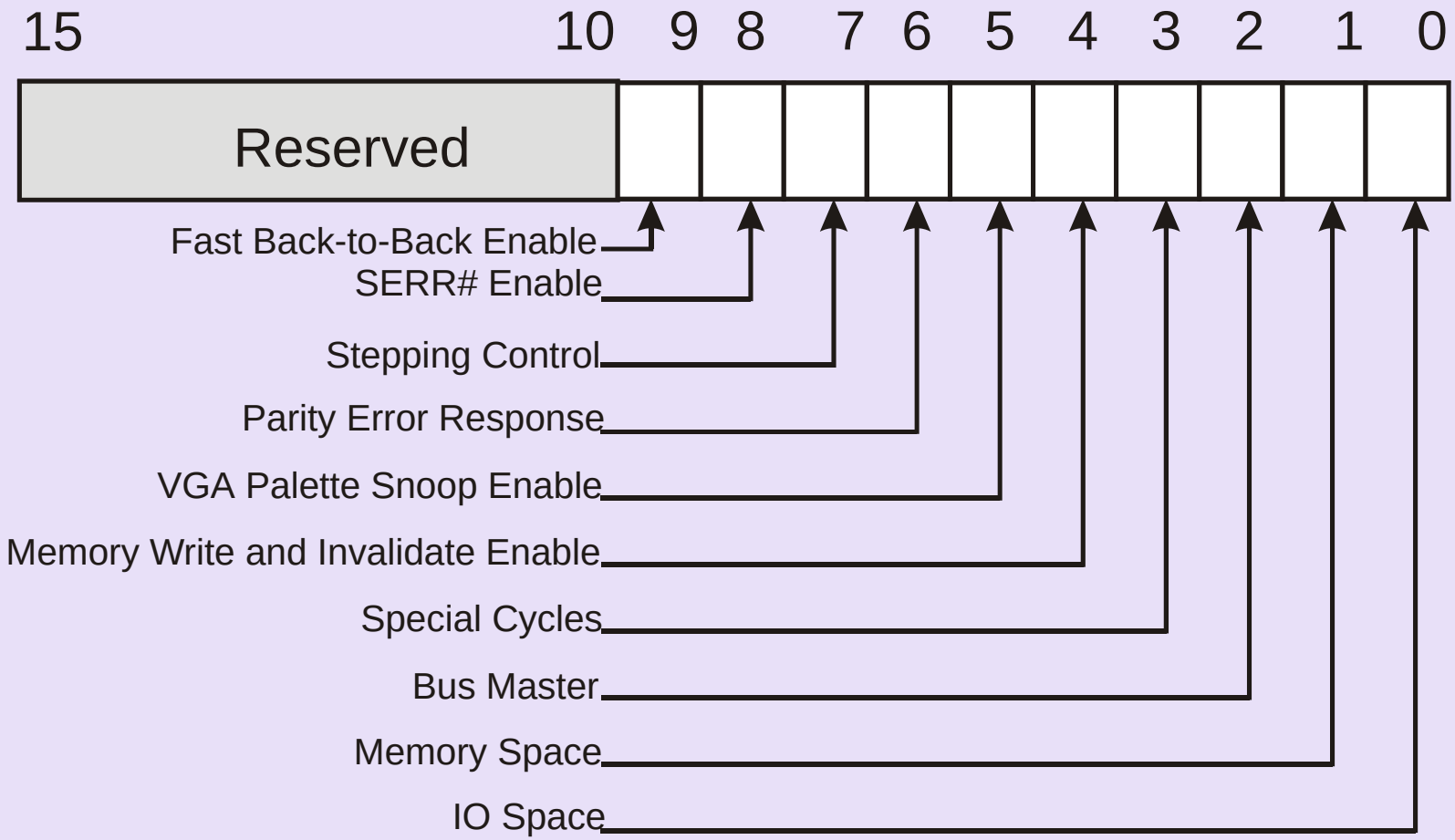
Registers that ID the Device



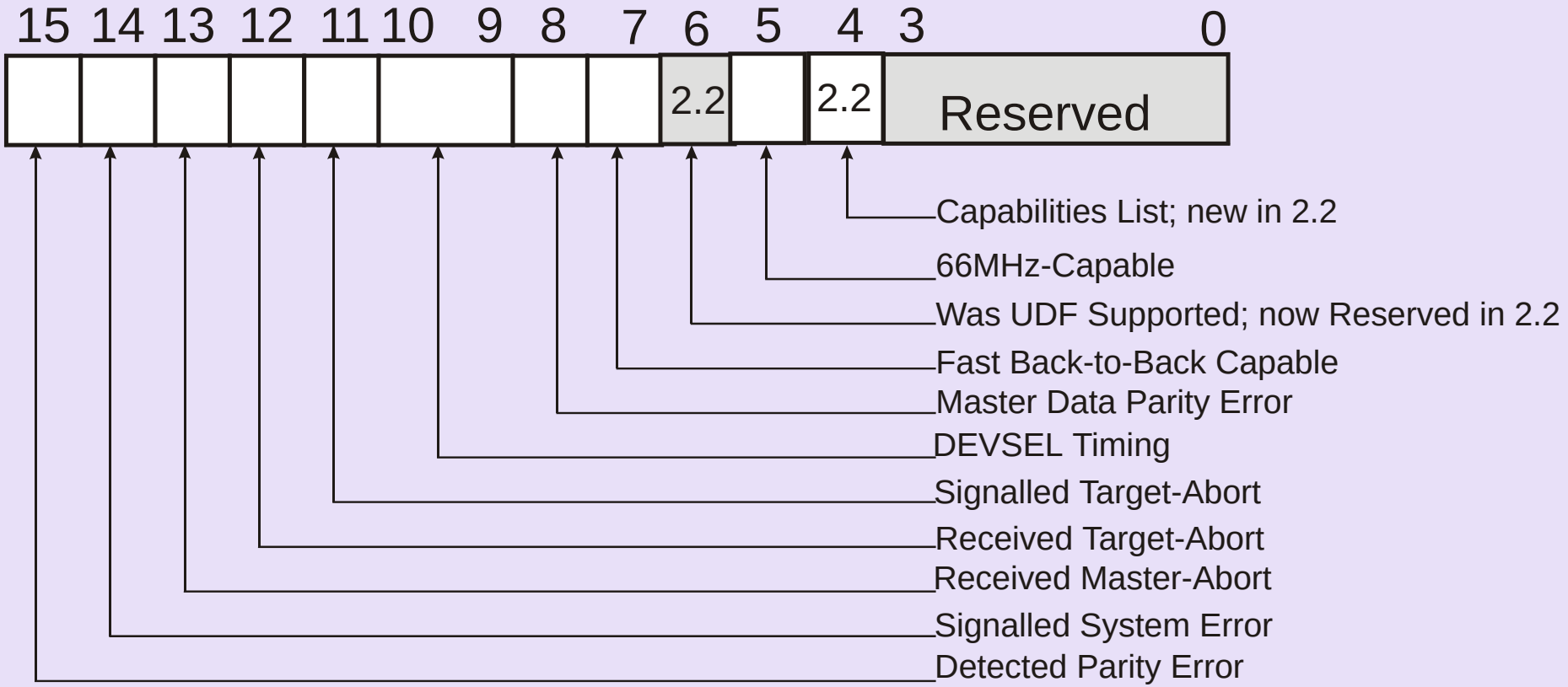
Class Code Register Format



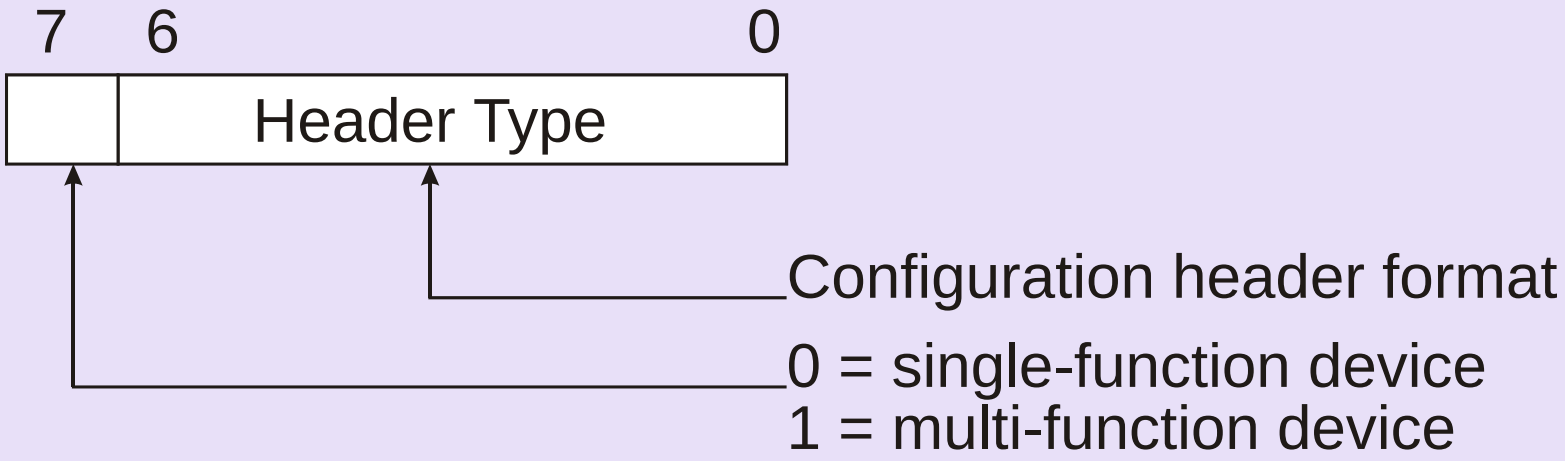
Command Register Format



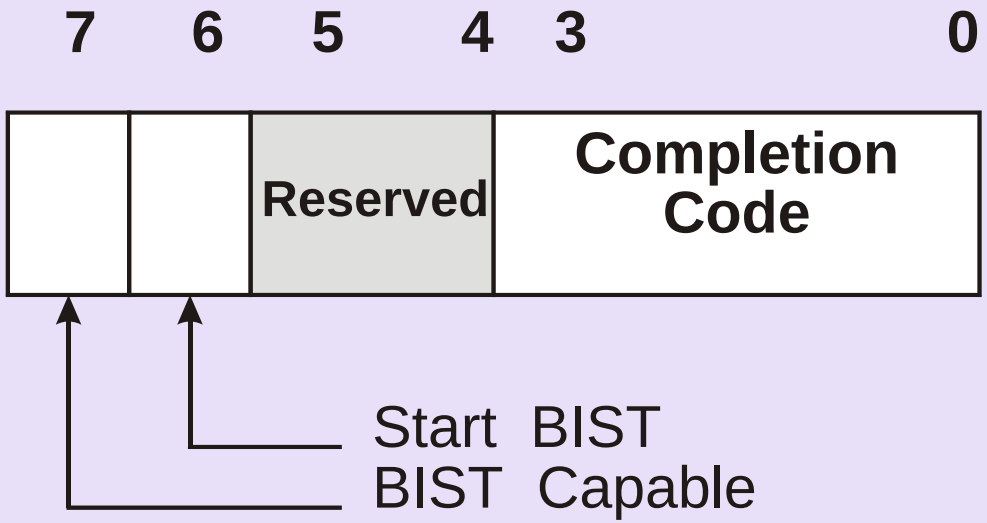
Status Register Format



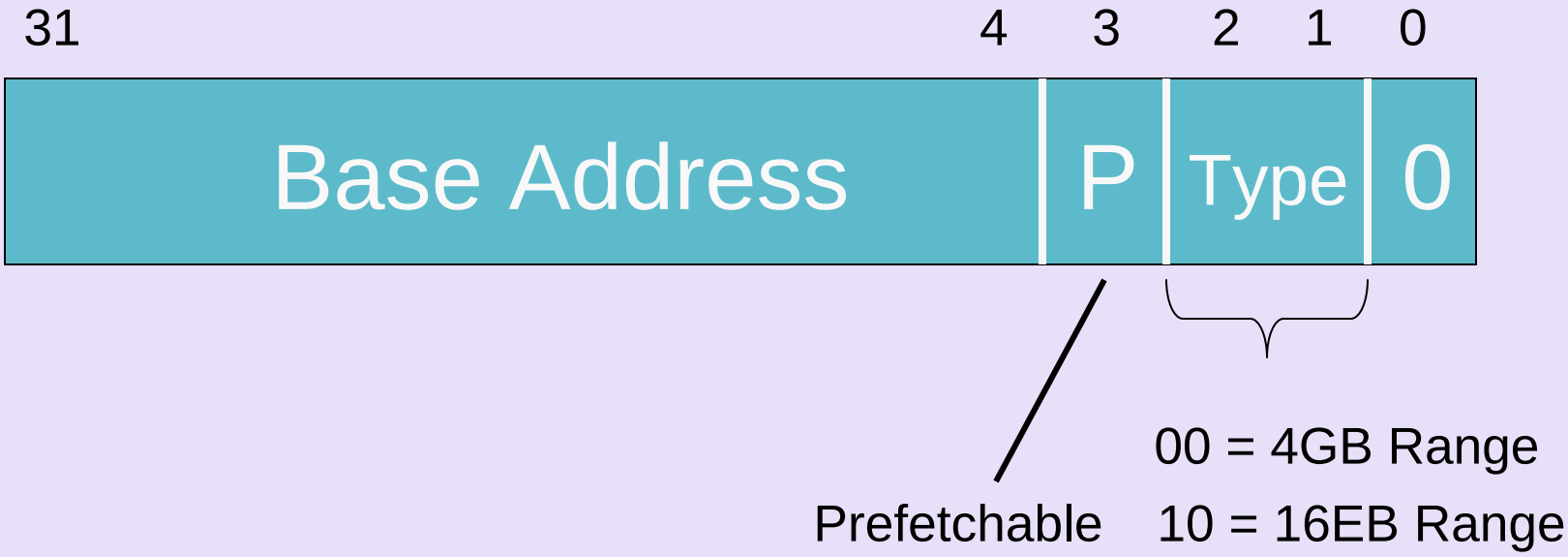
Header Type Register Format



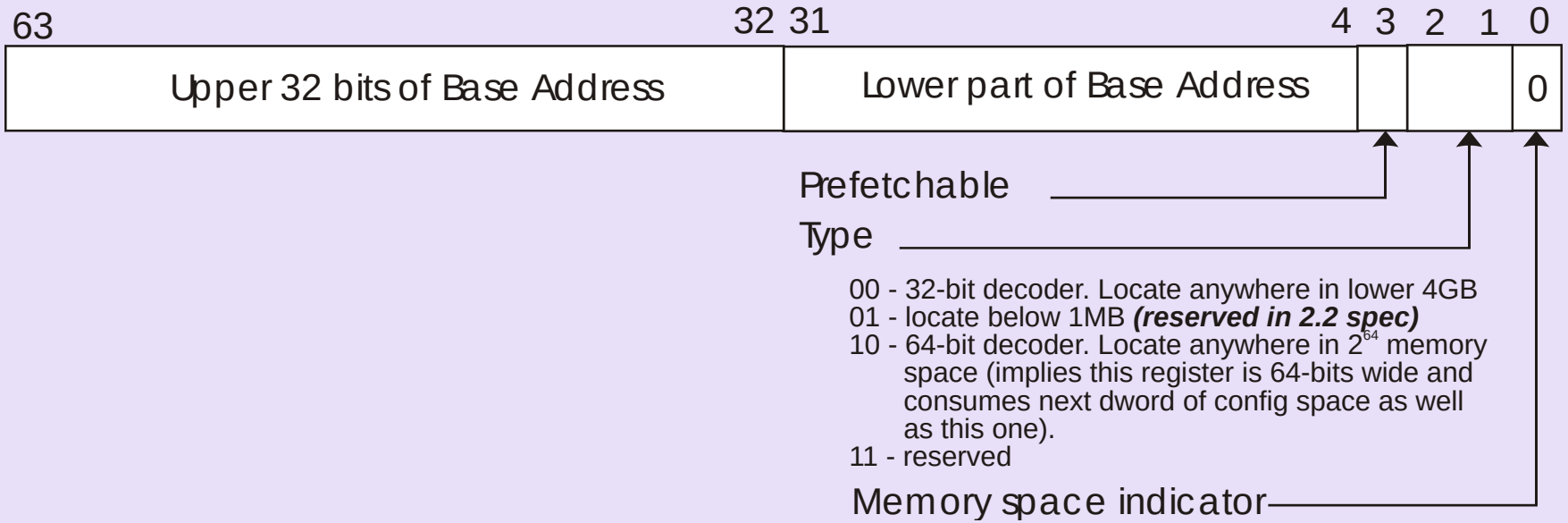
BIST Register Format



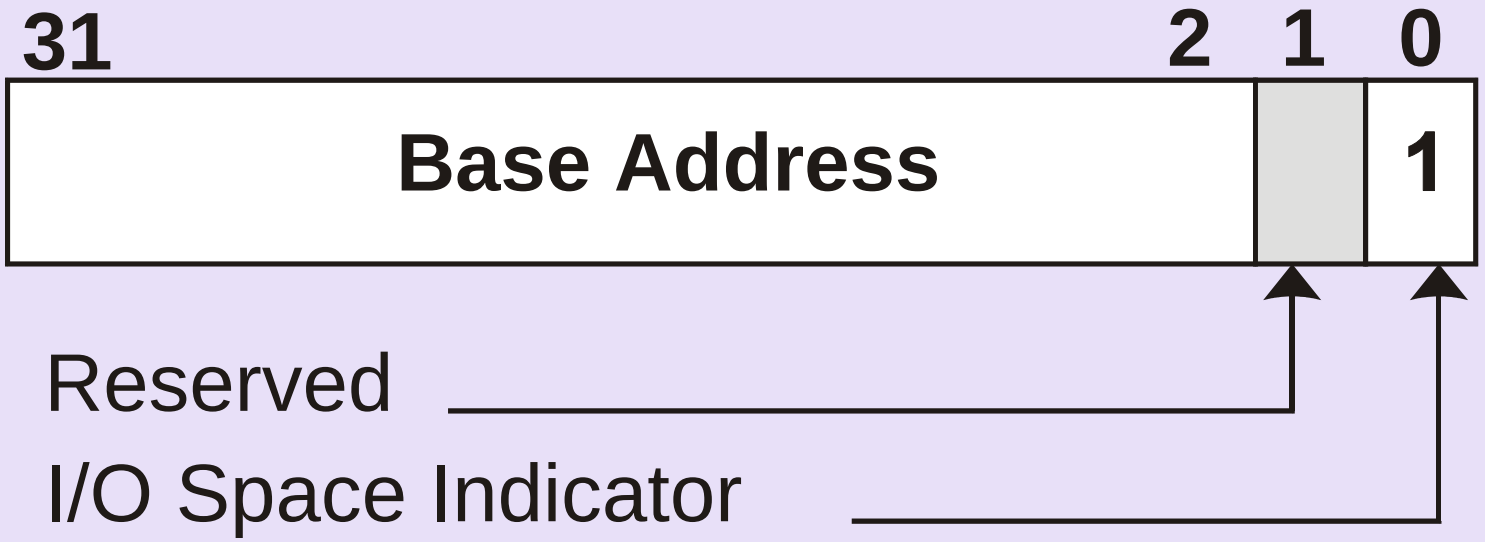
32-Bit Memory Bar



64-Bit Memory Bar



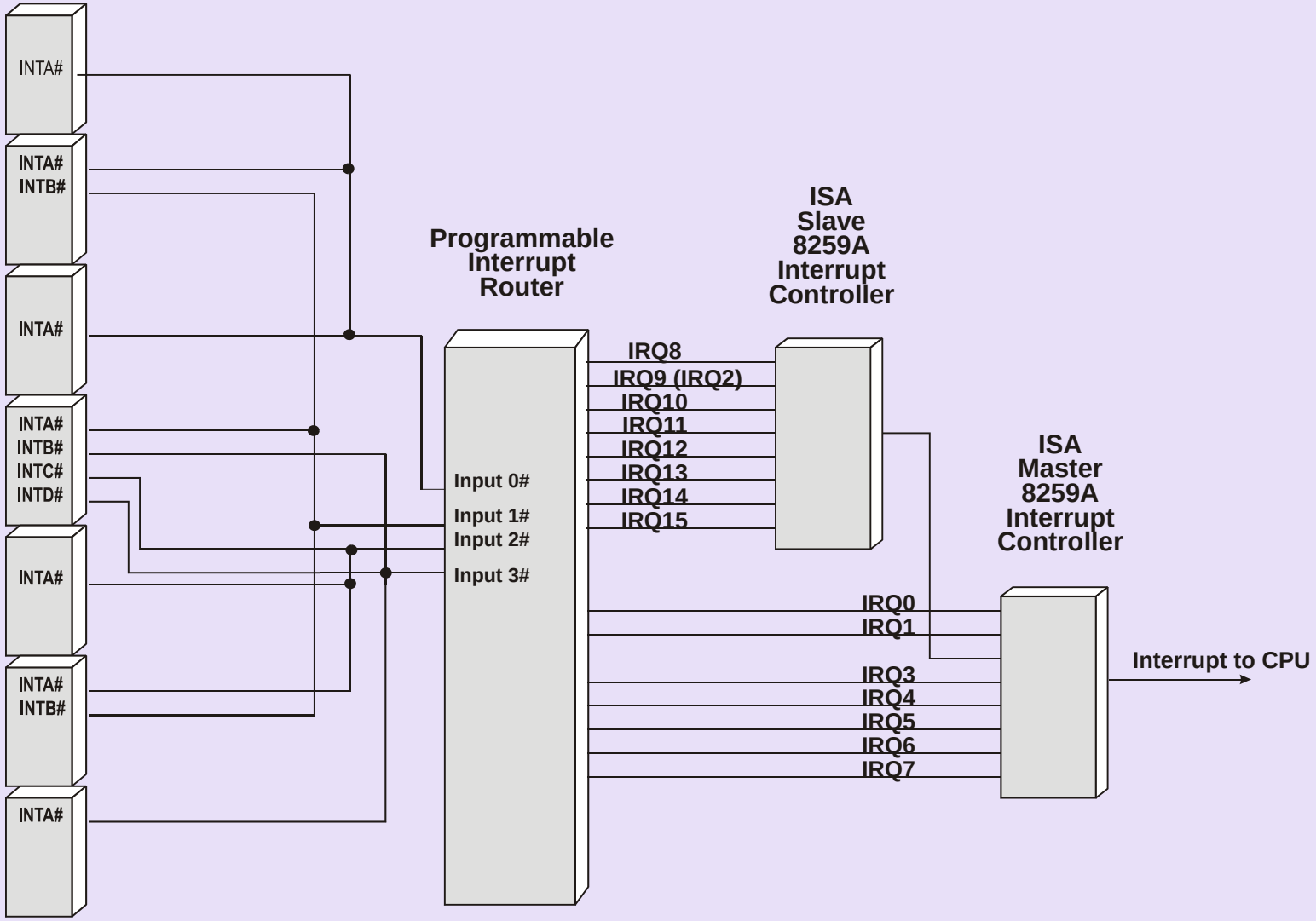
IO Bar



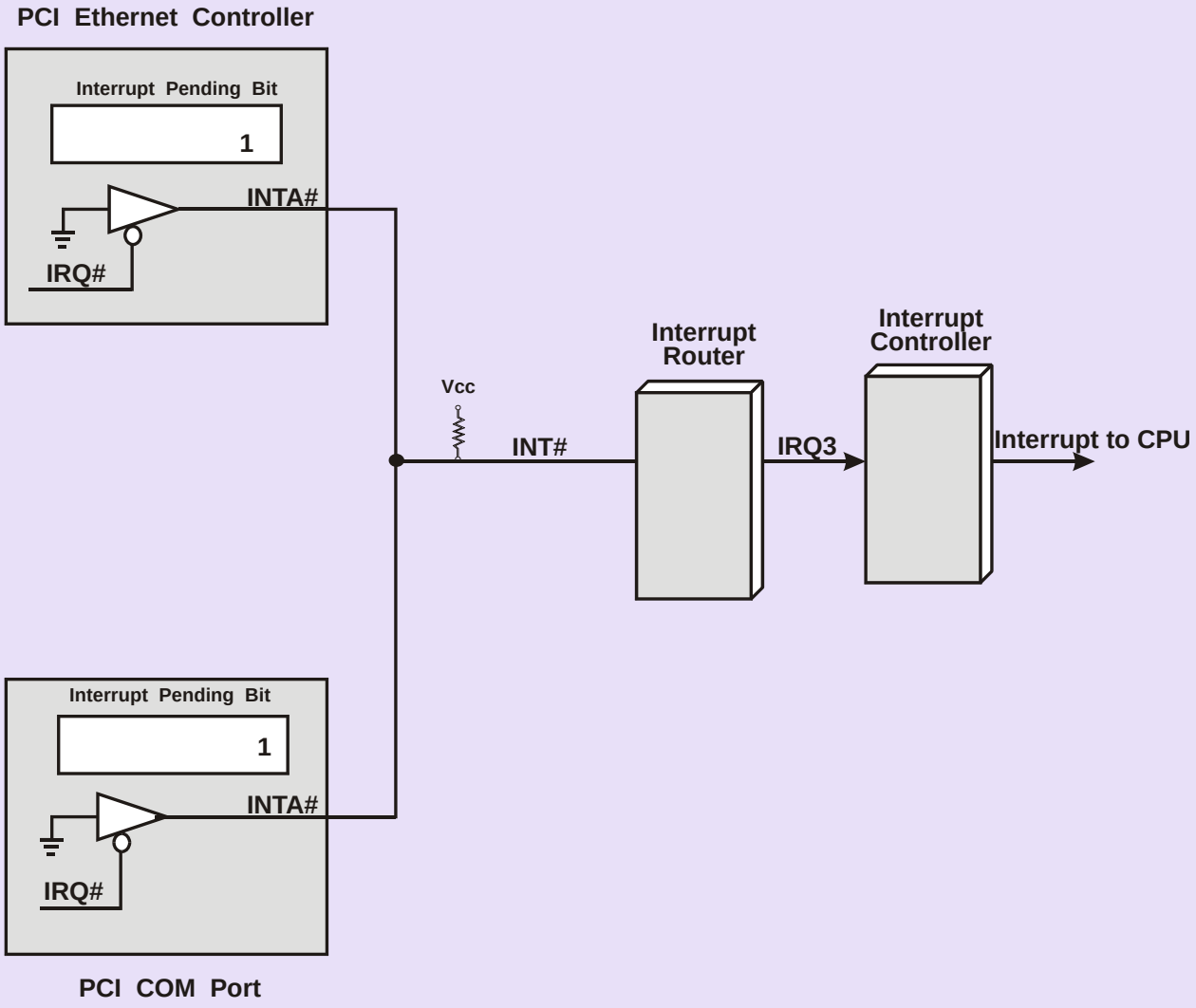
PCI Interrupt Deliver Mechanisms

- INTx Interrupt Delivery (x=A, B, C, or D)
- Message Signaled Interrupts - MSI (via Memory Writes)
- Enhanced Message Signaled Interrupts - MSI-X (via Memory Writes)

Interrupt Signal Routing



Interrupt Sharing



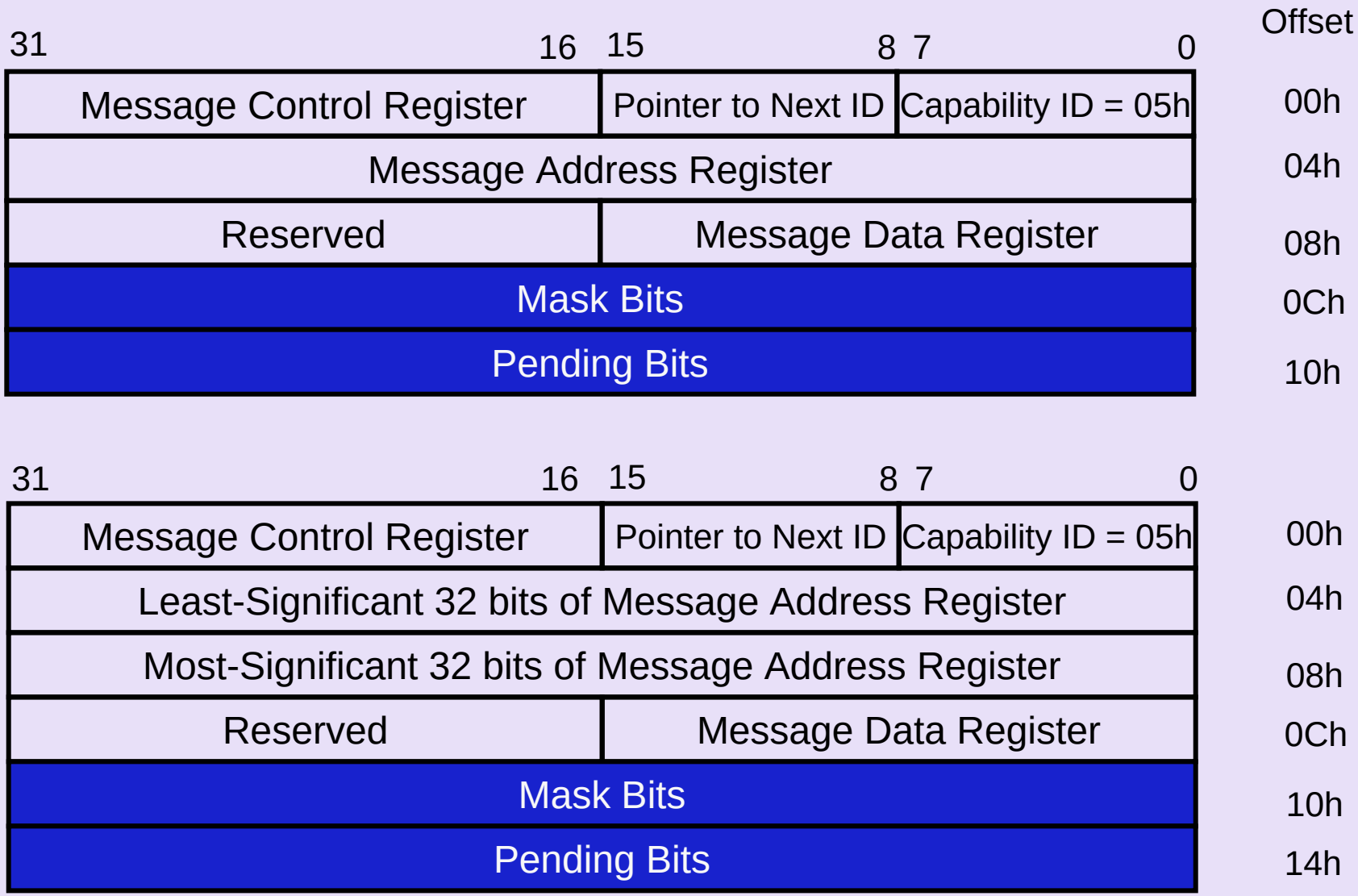
Message Signaled Interrupts

- Allow master to send interrupts via Memory Write transaction.
- Software assigns memory address location to write to within CPU/PCI bridge and assigns data value to be written.

Advantages of MSI

- No interrupt traces required
- No interrupt sharing
- No device driver chaining
- MSI can identify the service to be performed
- No read needed to ensure write buffers are flushed

MSI Capability Register 32 & 64 Bit Versions



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