A Built-In Mixed-Signal Test Architecture for a PCIe® PHY in 90nm and 130nm CMOS

Kannan Krishna

R&D Engineer

SYNOPSYS®

Outline

- PCIe® IP
- Testing Overview
- Analog Test Architecture
- PCIe Characterization Test Examples
- ATE Versus Characterization
- Conclusions

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Synopsys PCIe® IP Perspective

- Customers buy IP blocks to implement PCI Express® on their chips
- Synopsys provides a complete PCIe solution
  - ✓ PHY Hard Macro – Mixed-Signal IP
    - Analog and Digital
  - ✓ Complete Protocol Stack – Soft Digital IP
    - RTL gets added to ASIC design
  - ✓ Verification IP
    - Provides verification of the entire implementation
    - But it's not sufficient for testing the PHY
- Testing the PHY is not covered by traditional verification techniques

Testing PCIe® IP

- Final customer chip with PCIe® is a mix of high-speed analog and digital
- Digital can be tested using standardized test methodologies on low-cost digital testers
- Analog circuitry can be difficult to test
  - ✓ Two type of faults:
    - Functional
    - Parametric
  - ✓ PCIe® PHY is a small portion the of ASIC area. Functional yield primarily dictated by ASIC area but test escapes in the analog directly impact the quality level (DPM).
- Does it have to be hard to test the high-speed analog part of PCIe to meet your quality goals?
- Will test make it hard to adopt PCIe?
- This talk will concentrate on methodologies to make testing the analog portions of the PCIe PHY easy.

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Testing Overview: Digital

- Mature
  - ✓ Fault models provide possible failure modes
    - – Stuck at faults
    - – Bridge faults
  - ✓ These are used to generate patterns to detect failures
    - – Given a vector input x, do the circuits produce the output vector y?
    - – Observability needed in digital circuits
- Standard Techniques
  - ✓ Built into many EDA synthesis tools (Mux-D Scan
  - ✓ IDDQ
- JTAG standard (IEEE 1149.1) enables observability of internal signals as well as pins

Testing Overview: PCIe®

- But PCIe PHY is analog in nature
  - ✓ How do we do boundary scan for AC coupled links?
  - ✓ Termination resistance – Not just are we terminated, but how close to 50Ω?
  - ✓ TX output has boost and variable magnitude – How do we measure them?
  - ✓ Electrical idle detect threshold levels – Not just do we detect electrical idle, but what is our detect threshold?
  - ✓ Phase and voltage margining – Not just does the PHY work, but how well does it work?
  - ✓ What does the received eye look like?

Testing Overview: How to Test Analog?

- Not as mature a field as digital
  - ✓ No universally accepted fault models
  - ✓ Parametric issues – measurements are often continuous analog values
- Few Standard Techniques
  - ✓ Not built into analog design tools
  - ✓ Different circuits often require different types of measurements
  - ✓ Different types of measurements often require different types of test equipment
- Hard to access internal analog circuit nodes after fabrication

Conventional Analog Test Methodology

- Requires external test equipment and fixtures
  - ✓ Ohmmeters, voltmeters, scopes
  - ✓ Fixture to add noise to degrade margin
  - ✓ External equipment often expensive
- Done using techniques akin to those used in digital circuits from pre-JTAG days
  - ✓ Internal probe pads
  - ✓ Extra ‘test only’ pins
- Different testing methodology from digital
  - ✓ No concept of binary test vectors
  - ✓ Need tester that can do analog as well as digital testing

Built-In Analog Test Methodology

- Minimize need for external test equipment
  - ✓Analog measurements done on-chip
  - ✓On-chip margining circuitry
- Does not require external test hooks into chip
  - ✓No probe pads
  - ✓No extra test pins for analog
- Use testing methodology similar to digital
  - ✓Ability to use digital tester for analog test

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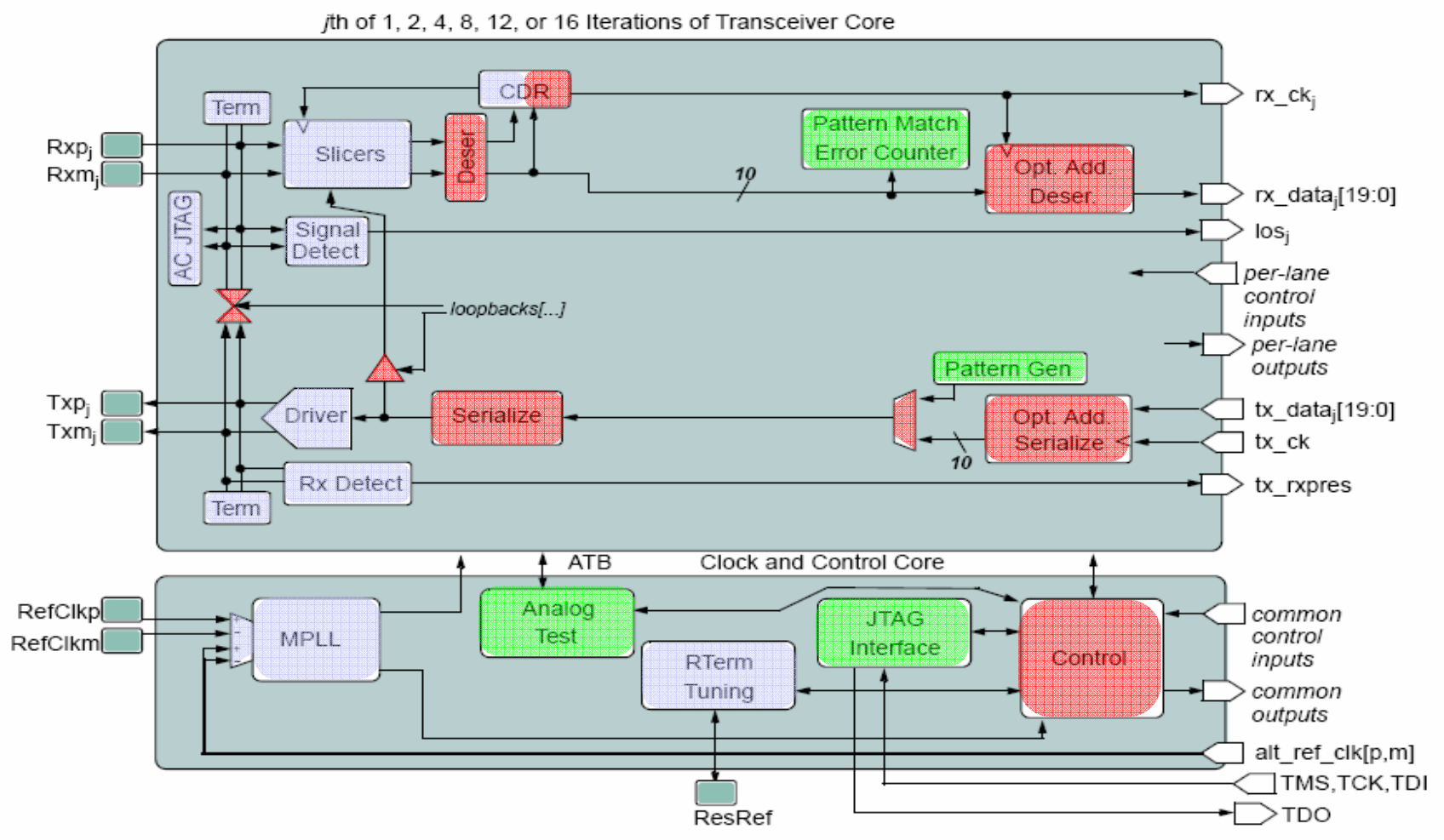
Synopsys IP: PCIe® PHY Block Diagram



red = digital, blue = analog, green = test

Analog Test Architecture

- How can built-in analog self-test work?
  - ✓ Don’t you need an external voltmeter that is ‘accurate’ ?
  - ✓ Don’t you need pads to probe these voltages?
  - ✓ Won’t it cost a lot in area and power?
- 3 concepts
  - ✓ Bandgap voltage
  - ✓ Resistor ratios
  - ✓ Analog Test Bus

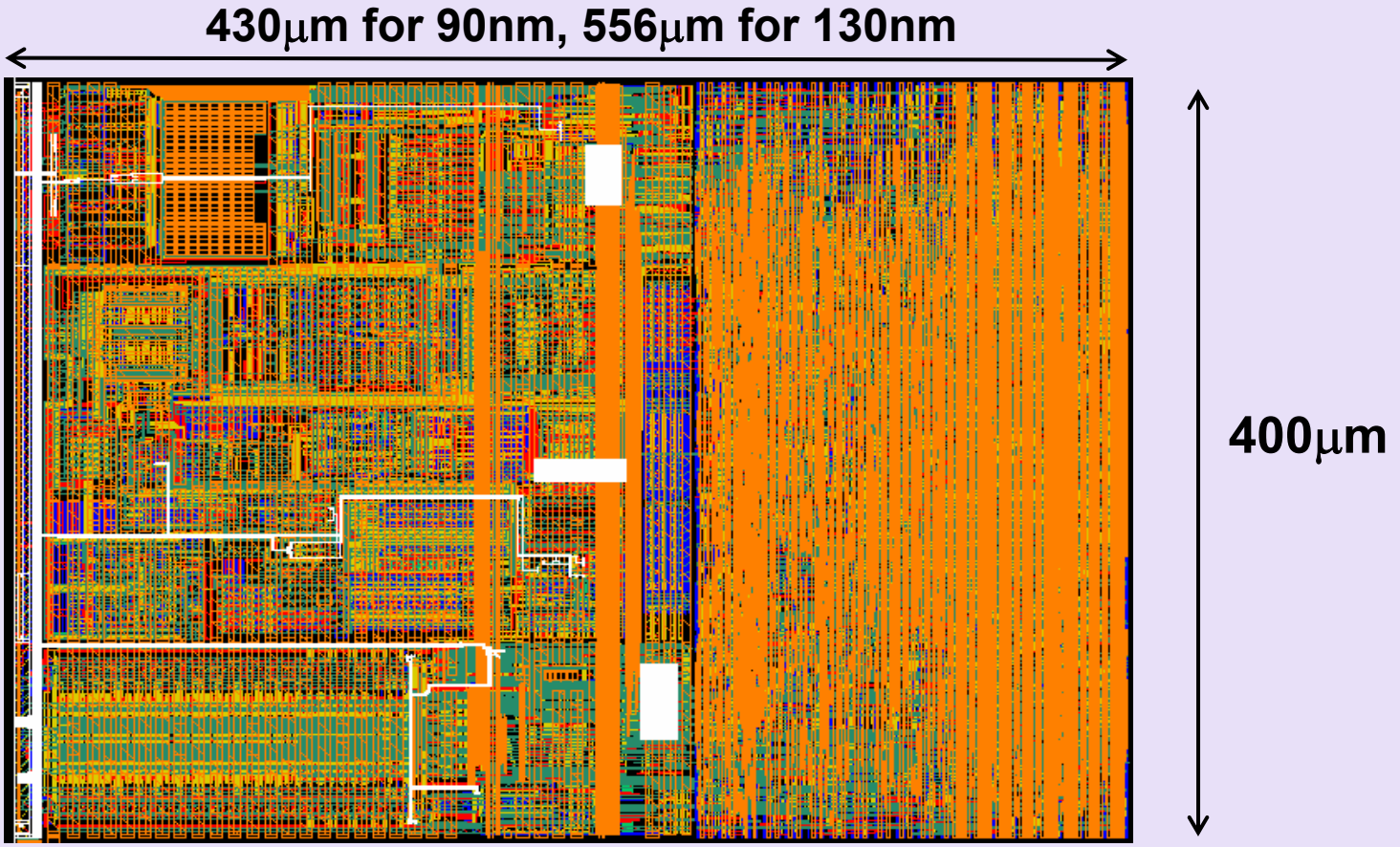
Analog Test Architecture

- Only additional circuitry is:
  - ✓ A resistor string DAC driven off of a known voltage
  - ✓ A low speed ADC that is accurate and compact in area
  - ✓ Analog Test Bus
- Every analog circuit block in the PHY should be built to:
  - ✓ Provide maximum observability without compromising performance (IEEE 1149.4)
  - ✓ Provide observability for failure modes specific to blocks
    - If sensitive to offset voltage between two nodes, provide access to measure their voltage difference

Analog Test Architecture

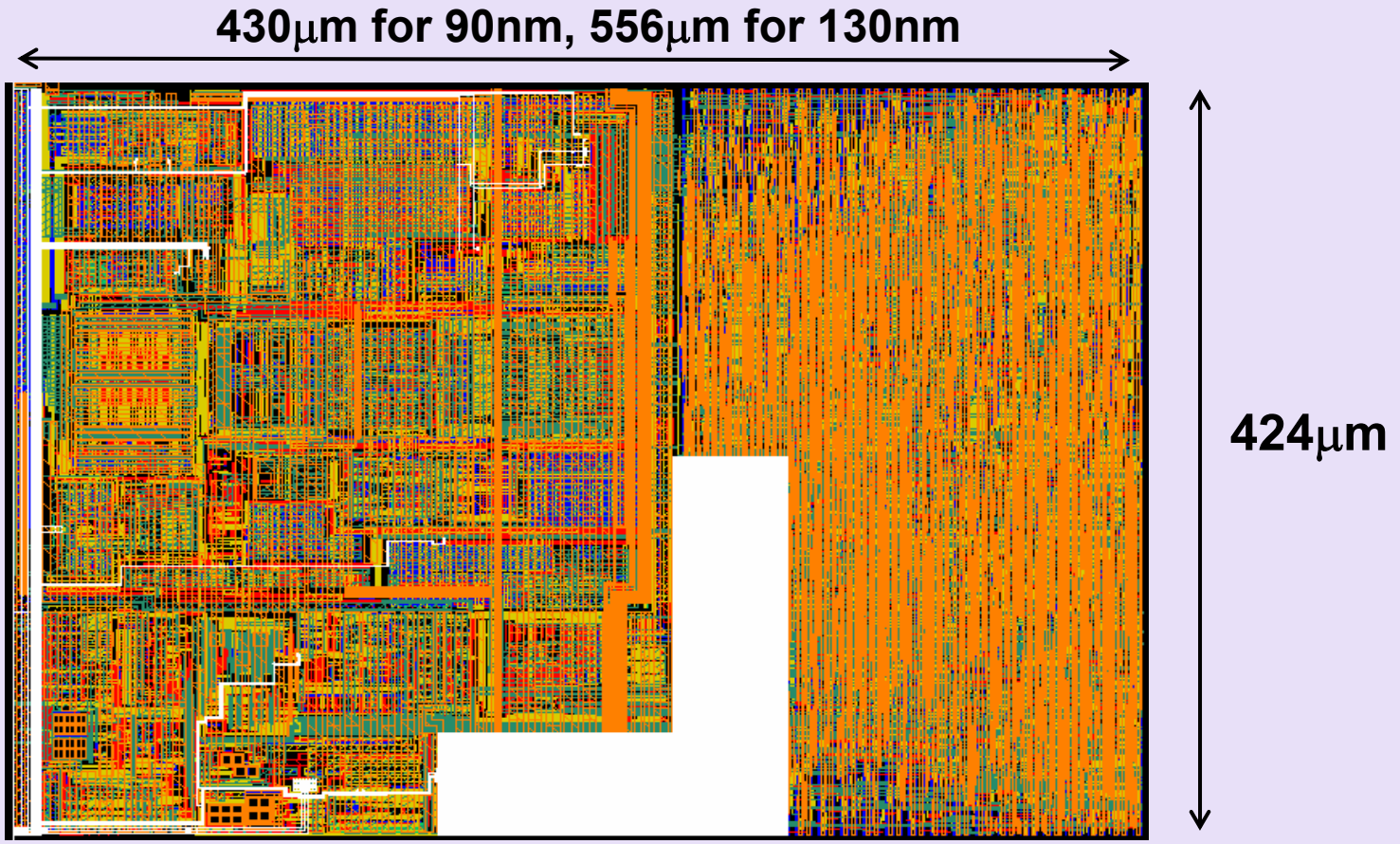
- Analog test circuits in control core
  - ✓ DAC, ADC, support logic
  - ✓ Zero power during normal operation
  - ✓ Control through digital port (e.g. JTAG)
- Analog Test Bus (ATB)
  - ✓ ATB goes through all lanes
    - Connects to Rx, Tx, and other important analog signals
  - ✓ ATB connects to control core
    - Analog test circuits (DAC, ADC)
    - MPLL, calibration circuits
- ACJTAG receiver in each lane for boundary scan of PCIe® links

Per Lane ATB Area



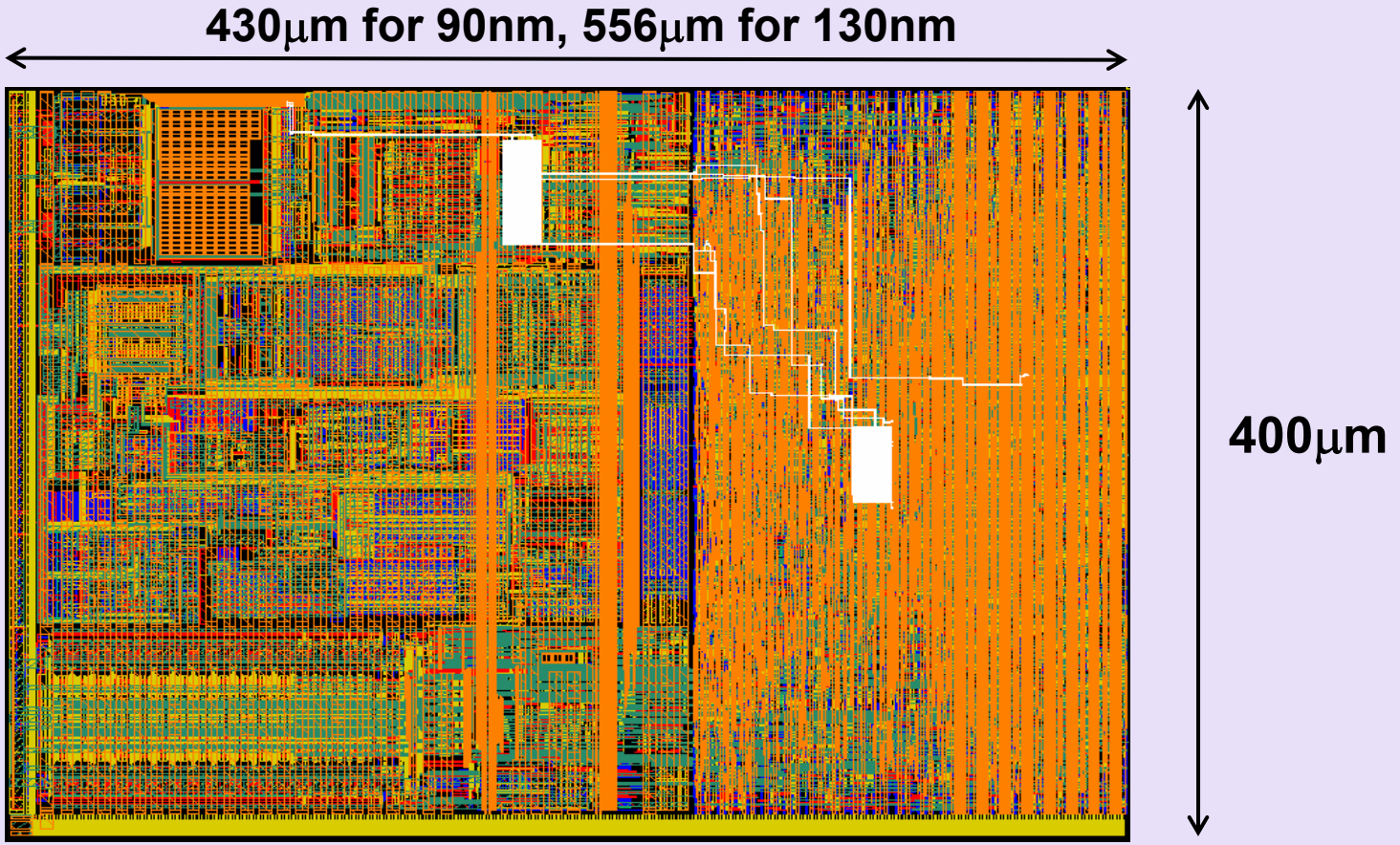
- ATB connects to relevant circuits in each lane. Highlights show bus and control registers.

Control Core ATB Area



- ATB connects to relevant circuits in control core. Highlights show bus and test circuits.

Per Lane ACJTAG Area



- Highlights show ACJTAG receiver, control, and signal paths. PCIe® transmitter used to send signals.

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Characterization Tests

- Needed to test device for:
  - ✓PCIe® compliance
  - ✓Guarantee no parametric yield loss in analog
- Test Methodology
  - ✓Part can be programmed to do all of its functions via digital interface (JTAG)
  - ✓Only digital data is sent to the part
  - ✓All results read back as digital vectors

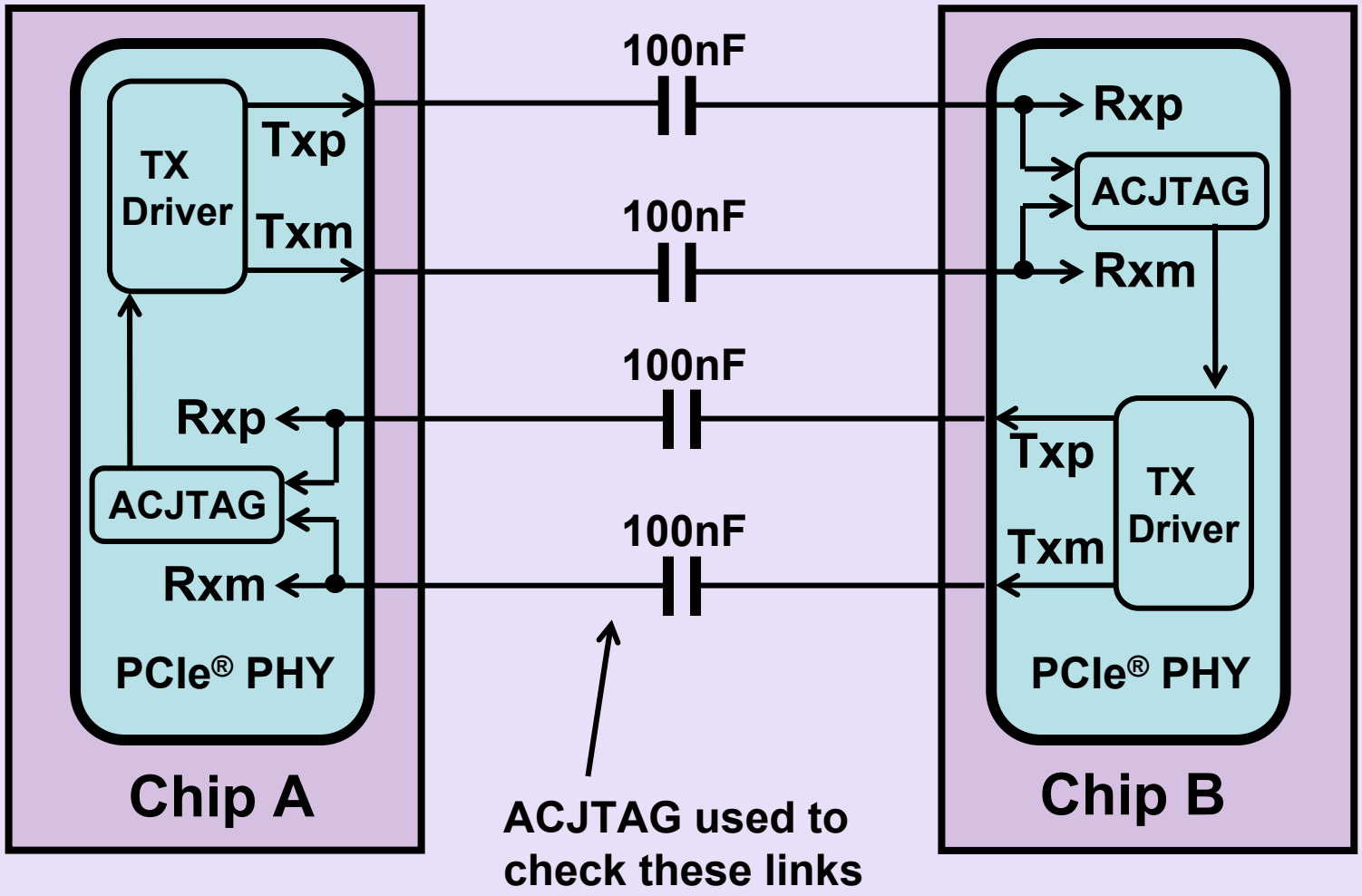
PCIe® Characterization Test Examples

- ACJTAG
- Termination Resistance
- Transmit Magnitude and De-emphasis
- Electrical Idle Detect Threshold
- Temperature Sensor
- Eye Mask Tests
  - ✓ Voltage Margining
  - ✓ Phase Margining
- On-chip Scope

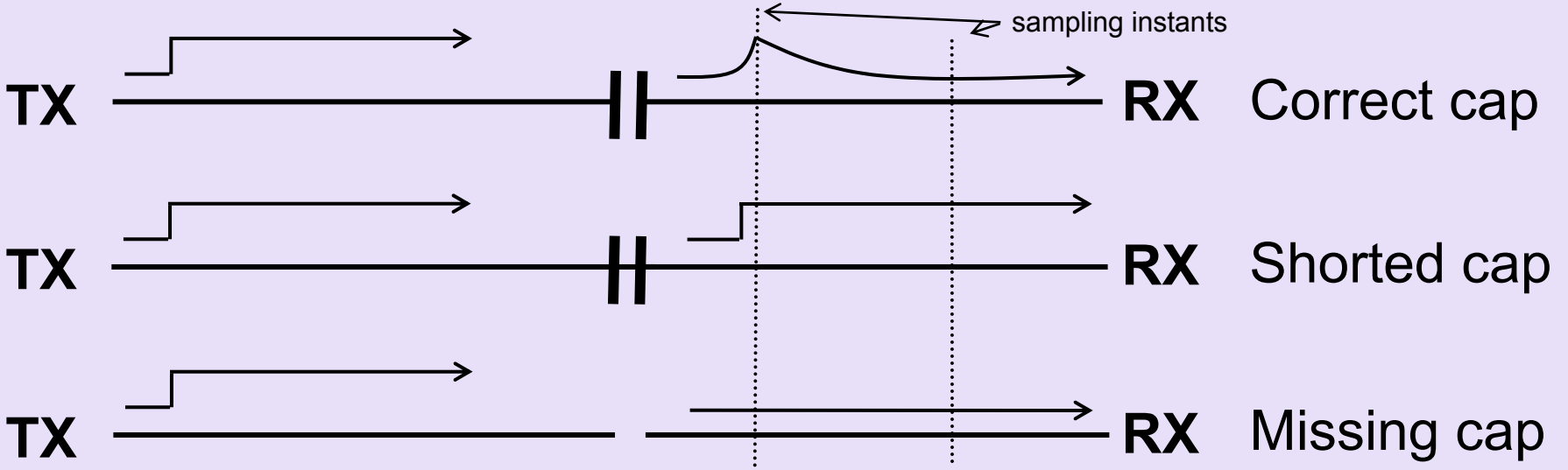
ACJTAG Motivation: Boundary Scan

- Regular JTAG (IEEE 1149.1) detects faults in DC coupled connections on PCB
- PCIe® uses AC (capacitive) coupling; needs ability to detect both:
  - ✓Shorted capacitors
  - ✓Missing capacitors
- ACJTAG (IEEE 1149.6) or similar technique is an invaluable part of any PCIe PHY

AC Coupled Links



ACJTAG Receiver Function



ACJTAG receiver can detect and distinguish between pulses and DC levels, both at PCIe® magnitudes, on a per pin basis. Requires dedicated analog circuit.

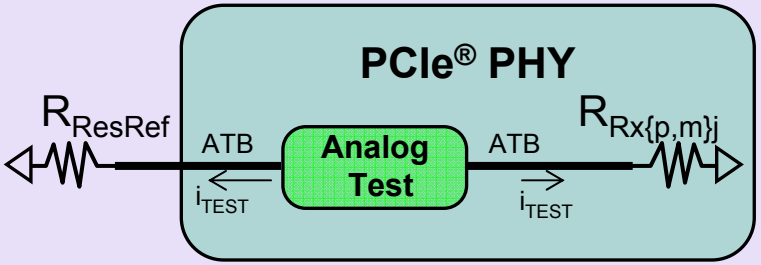
Signal Type	Missing Capacitor	Shorted Capacitor	Correct Capacitor
Pulse	Not Received	Received	Received
DC Level	Not Received	Received	Not Received

Termination Resistance Spec

- PCIe® Rx, Tx single-ended termination resistance spec is 40Ω-60Ω.
- Synopsys PCIe PHY calibrates Rx and Tx termination resistances at startup using external reference resistor, ResRef.
- How do we characterize these without external ohmmeters connected to all Rx and Tx pins?

Termination Resistance Measurement

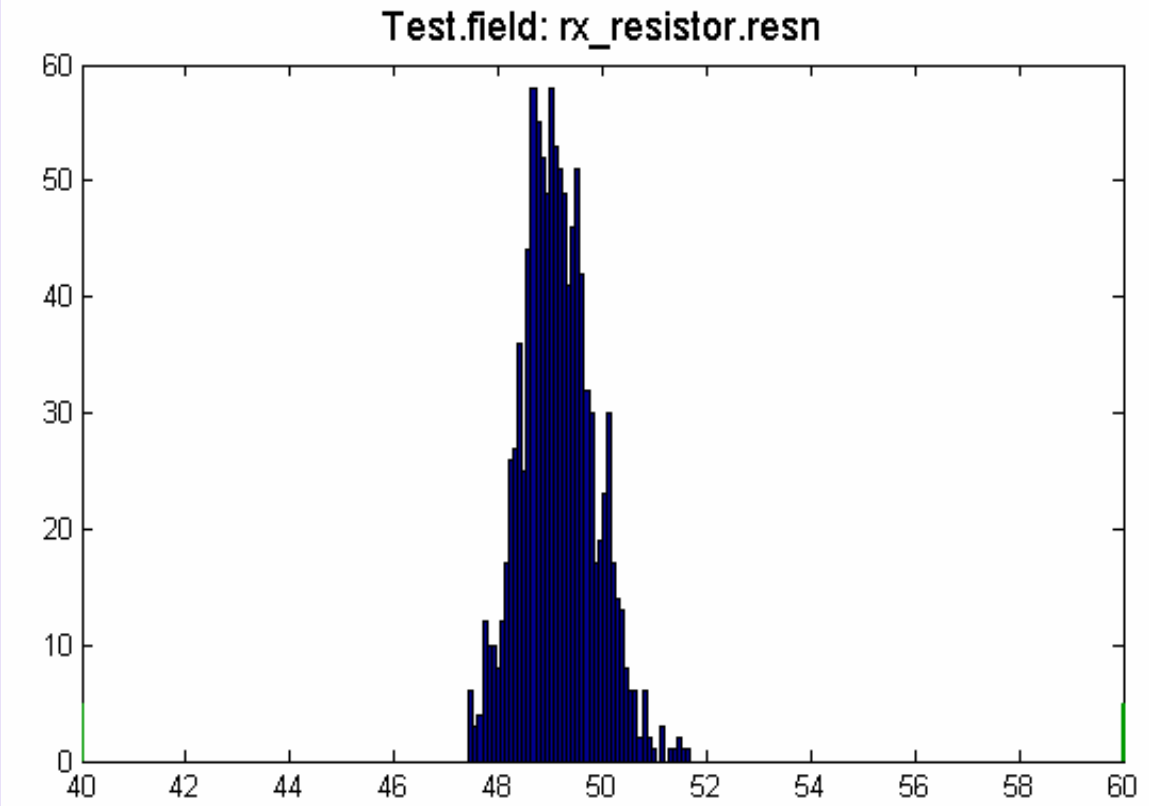
- Access each Rx pin one by one through ATB.
- Force a current into the Rx termination resistance and measure the voltage using the built-in ADC.
- Force the same current into the reference resistor and measure its voltage.
- Calculate the resistance of the Rx.
- Same type of measurement can be used for Tx.



$$R_{RX\{p,m\}j} = R_{RESREF} \frac{V_{RX\{p,m\}j}}{V_{RESREF}}$$

Termination Resistance Data

Histogram of Rx resistance measurements



Rx single-ended resistance (Ω)

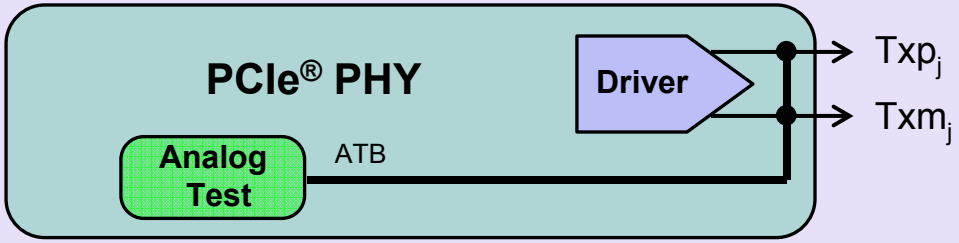
T : -5C to 120C
V_H,V_L: +/- 10%

Transmit Magnitude Spec

- PCIe® Tx output magnitude spec
  - ✓1V +/- 200mV pk-pk differential
  - ✓Minimum is half for mobile mode
- PCIe TX de-emphasis spec
  - ✓ 3.5dB +/- 0.5dB,
  - ✓ No de-emphasis for mobile mode
- How do we measure this without external voltmeters?

Transmit Magnitude Measurement

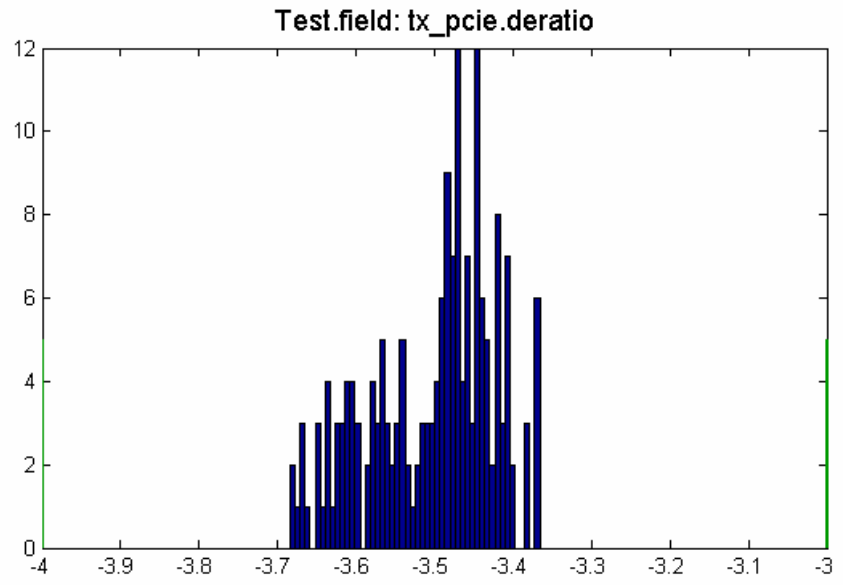
- Access each Tx differential output one by one through ATB.
- Set Tx to output a constant 1 (or 0) with de-emphasis turned off.
- Measure the Tx differential output voltage, calculate output voltage.
- Repeat measurement with equalization turned on; divide by the previous measurement to determine de-emphasis.



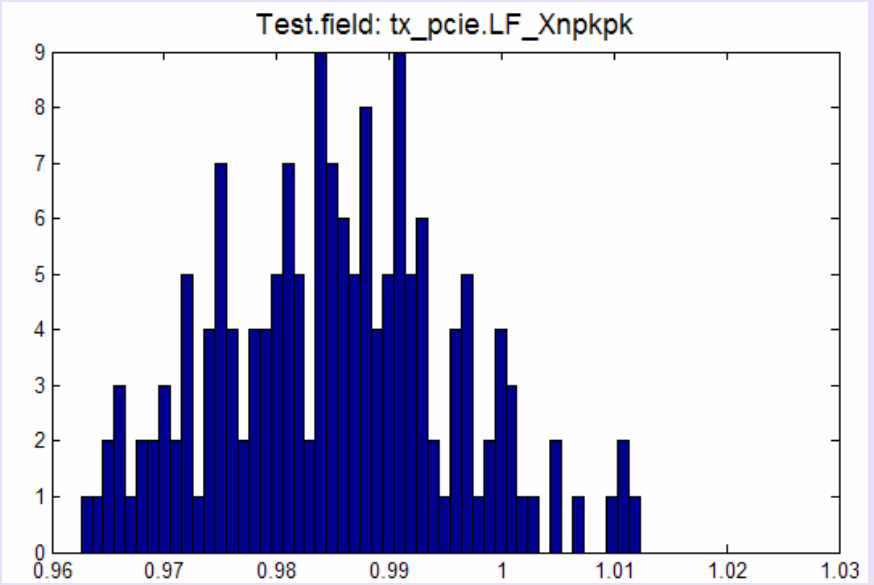
Calculation must adjust for absence of Rx load at DC.

Transmit Magnitude Data

Histogram of Tx magnitude measurements



Tx De-emphasis (dB)



Tx differential pk-pk output (V)

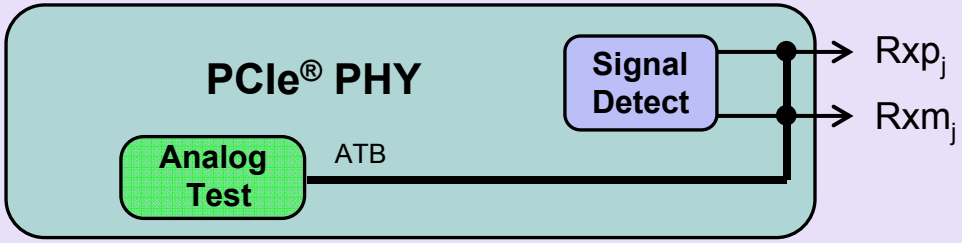
T : -5C to 120C, V_H, V_L: +/- 10%

Electrical Idle Detect Threshold Spec

- PCIe® Rx must detect electrical idle.
  - ✓Must always detect if input signal is above 175mV pk-pk, but always ignore signals below 65mV pk-pk.
  - ✓Therefore, electrical idle detect threshold must be between 65mV and 175mV.
- How do we measure the detect threshold without external voltage/signal sources?

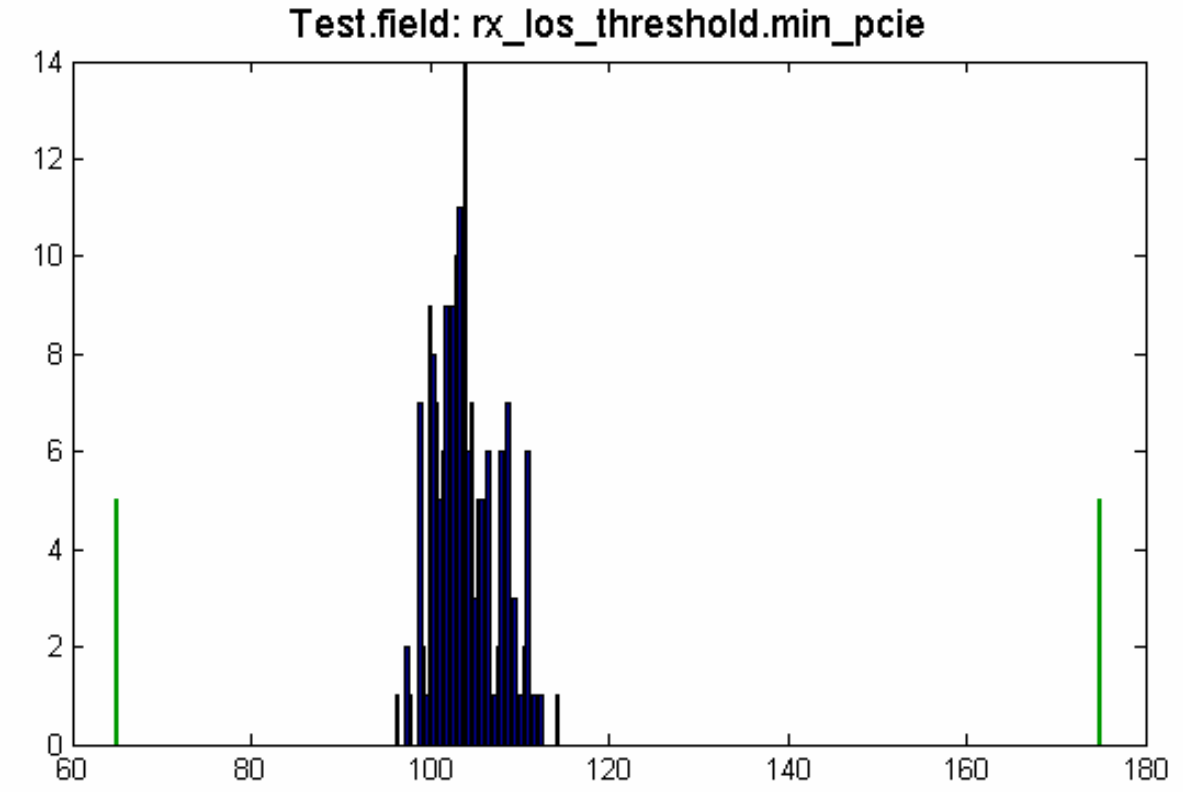
Electrical Idle Detect Threshold Measurement

- Access each Rx differential input one by one through ATB.
- Using DAC in analog test block, impose a small differential input on Rx.
- Ramp this imposed Rx input signal until electrical idle detect is triggered.
- Last value of imposed input is detect threshold.



Electrical Idle Detect Threshold Data

Histogram of electrical idle detect threshold measurements



T : -5C to 120C
V_H,V_L: +/- 10%

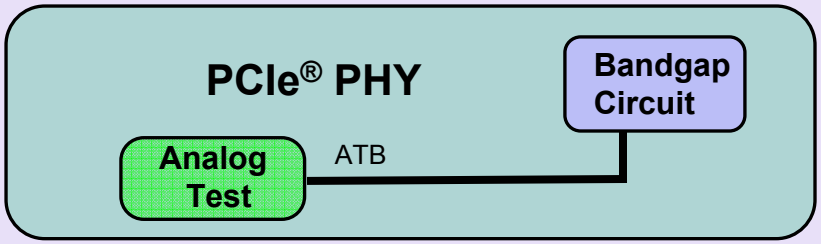
Electrical idle detect threshold, pk-pk differential (mV)

IC Junction Temperature

- PCIe® must operate over a wide temperature range.
  - ✓ Test setup can often control the external package temperature.
  - ✓ But internal IC junction temperature can be higher due to heat dissipation on–chip.
- To correlate performance to device temperature, it would be useful to know the IC junction temperature.
- How do we measure the temperature of the chip itself?

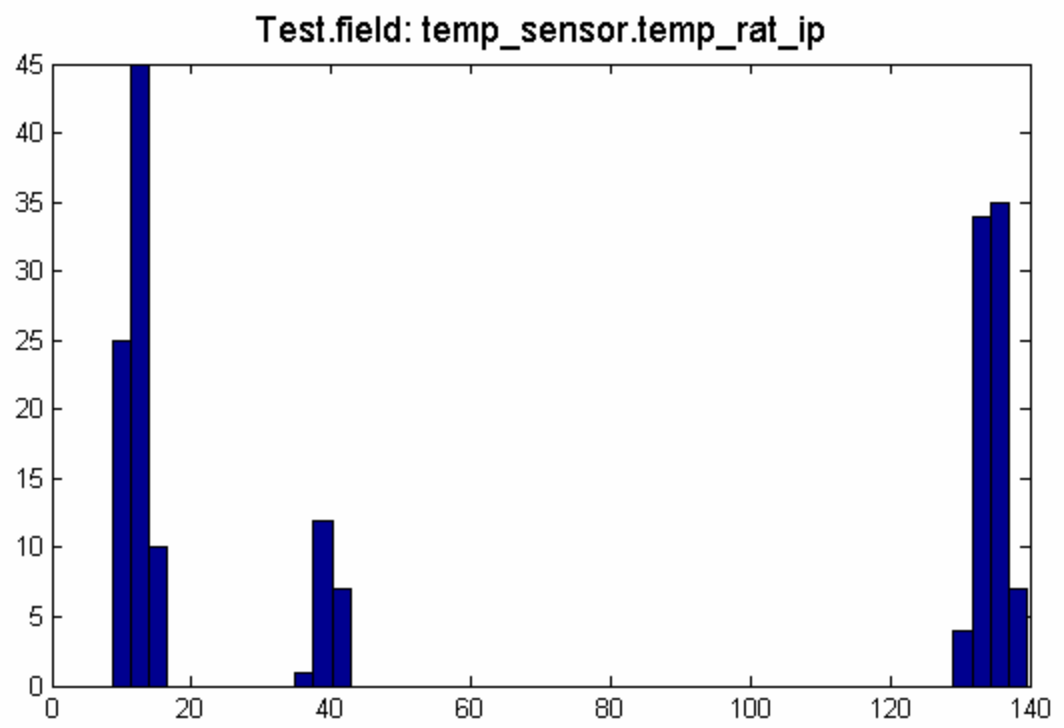
IC Junction Temperature Measurement

- Bandgap circuit in control core contains bipolar NPN transistors, whose current is an exponential function of their temperature and V_{BE}.
- Force several currents through these transistors.
- Using the ATB, access the bandgap circuit.
- Using ADC in analog test block, measure the V_{BE}.
- The temperature T is a linear function of the V_{BE} measurements.
- Almost no additional circuitry needed to implement this function.



IC Junction Temperature Data

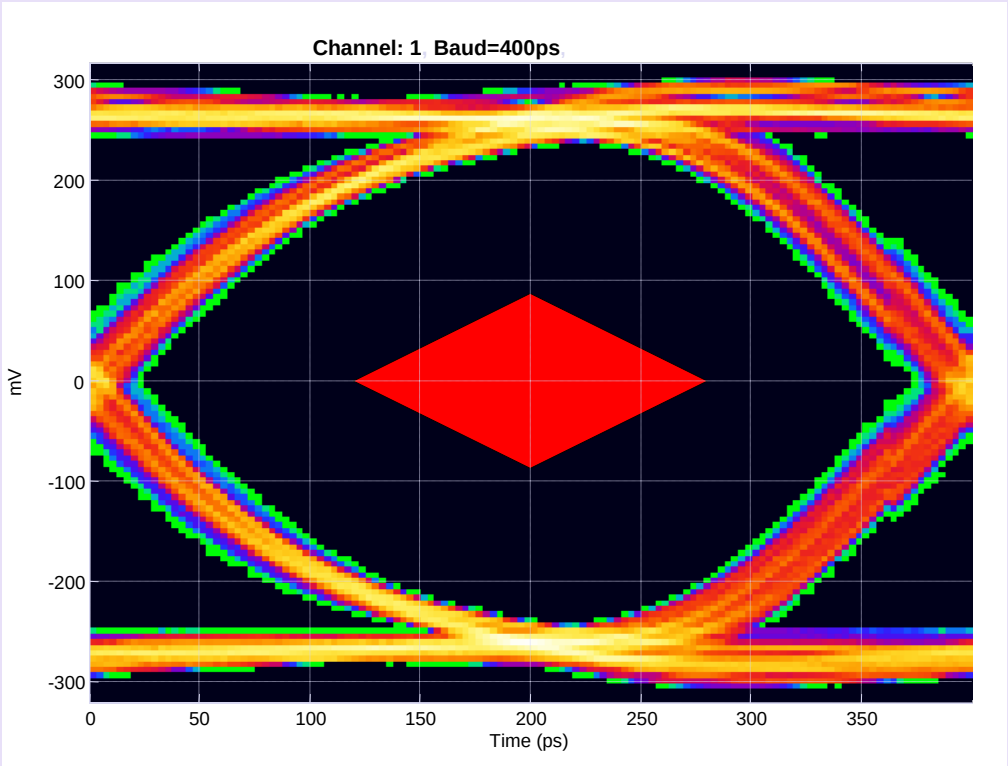
Histogram of temperature measurements



T : -5C, 25C, 120C
V_H,V_L: +/- 10%

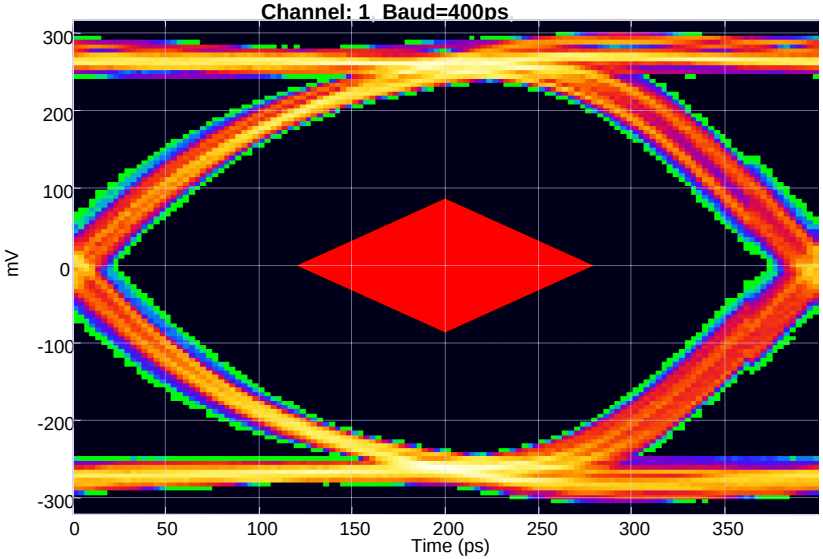
Eye Mask Tests

- PCIe® RX should be able measure an eye that is:
  - ✓ 175mV pk-pk
  - ✓ 0.4UI wide
  - ✓ Eye Mask



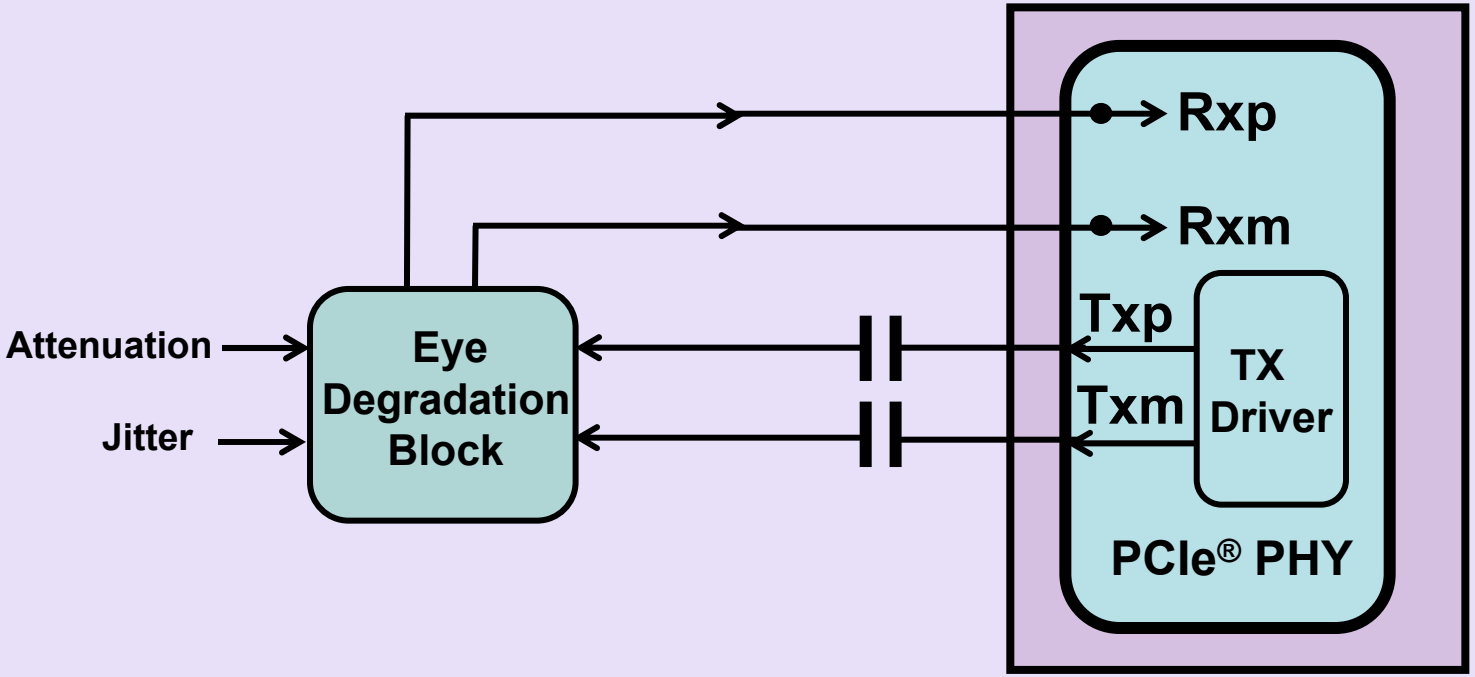
Voltage & Phase Margining

- Two one-dimensional problems
  - ✓ Measuring the height of the eye = Voltage Margining
    - Voltage offset that will cause the PHY to detect errors
  - ✓ Measuring the width of the eye = Phase Margining
    - Phase offset that will cause the PHY to make errors



Voltage Margining – External Test

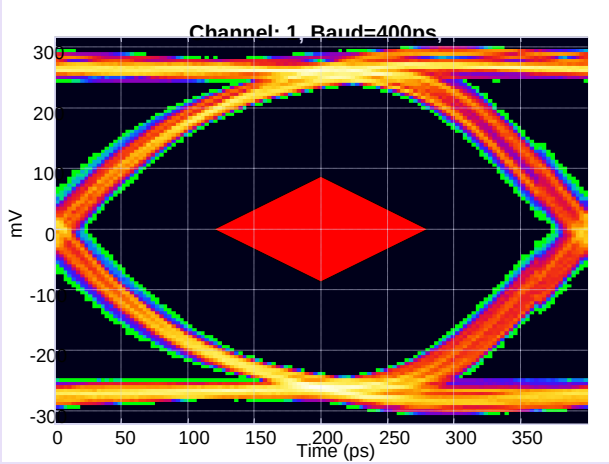
- External Test – eye degradation block



- ✓ TX characteristics affect waveform at RX
- ✓ Designing eye degradation block to only degrade voltage margin can be difficult

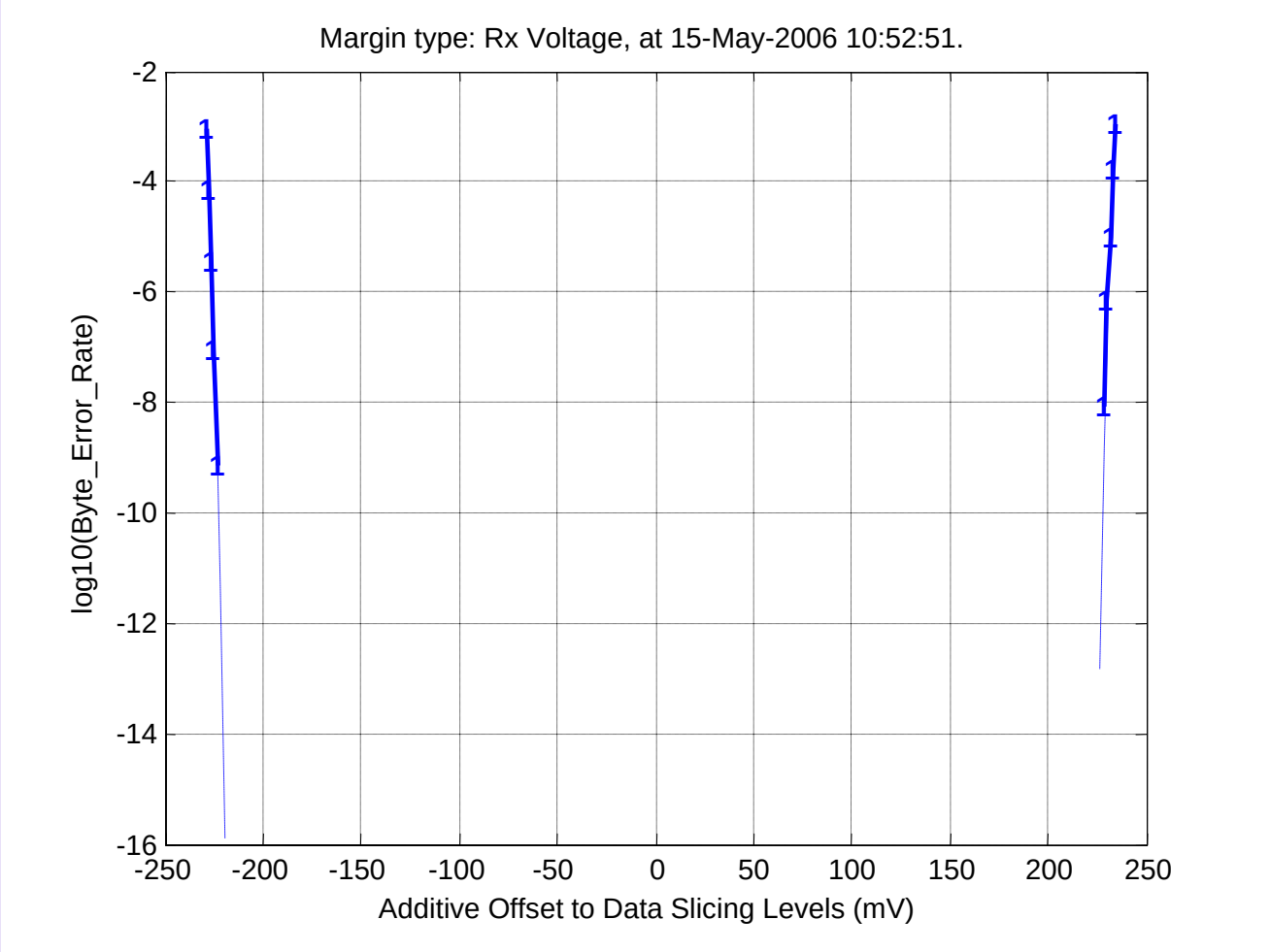
Voltage Margining – Internal Test

- Internal Test – add voltage offset to RX input
  - ✓ If RX operates with no errors at offset of +/-87.5mV, the RX will meet spec



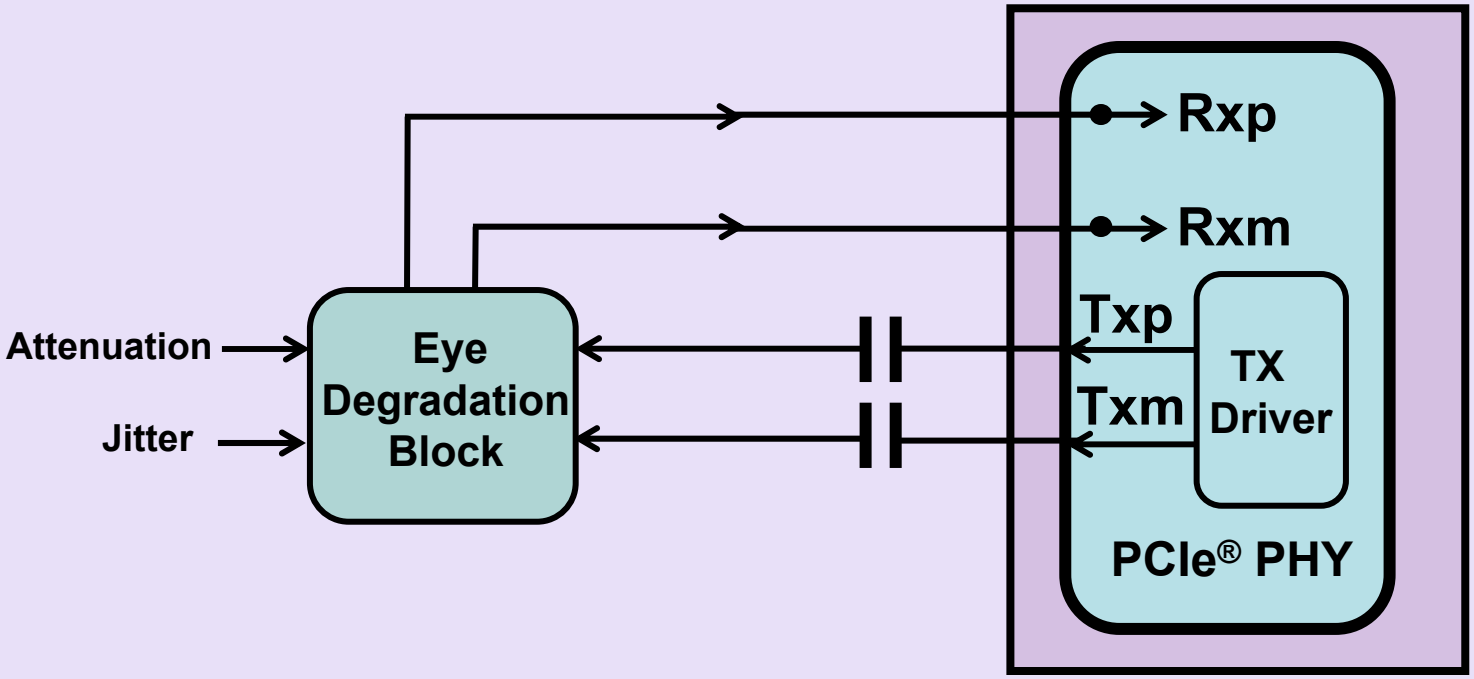
  - ✓ Requires internal test circuitry to be built in
  - ✓ Can keep clock recovery running
  - ✓ Can be measured with an asynchronous clock

Voltage Margining – Bathtub curve



Phase Margining – External Test

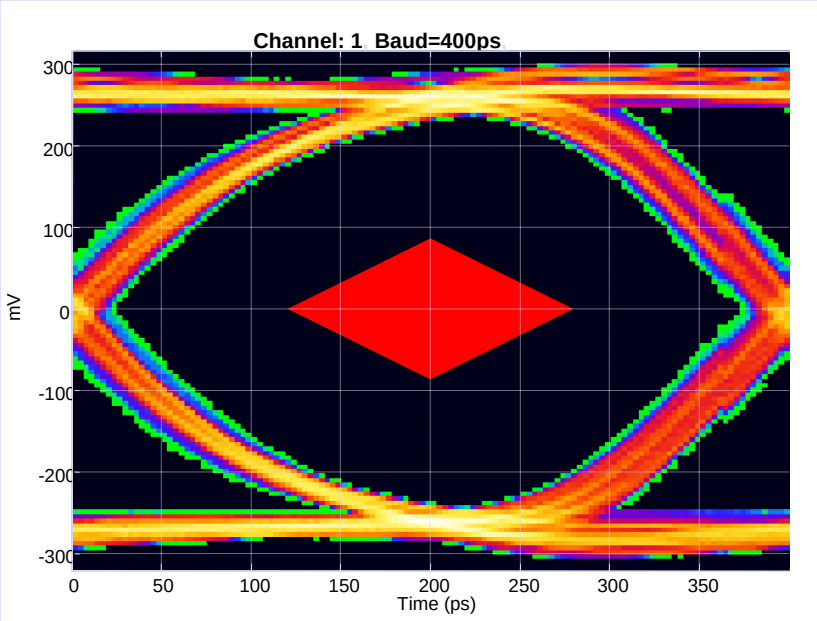
- External Test – Eye Degradation Block



- ✓ No accurate measure of how close part is to failure
- ✓ Difficult to decouple attenuation and jitter effects

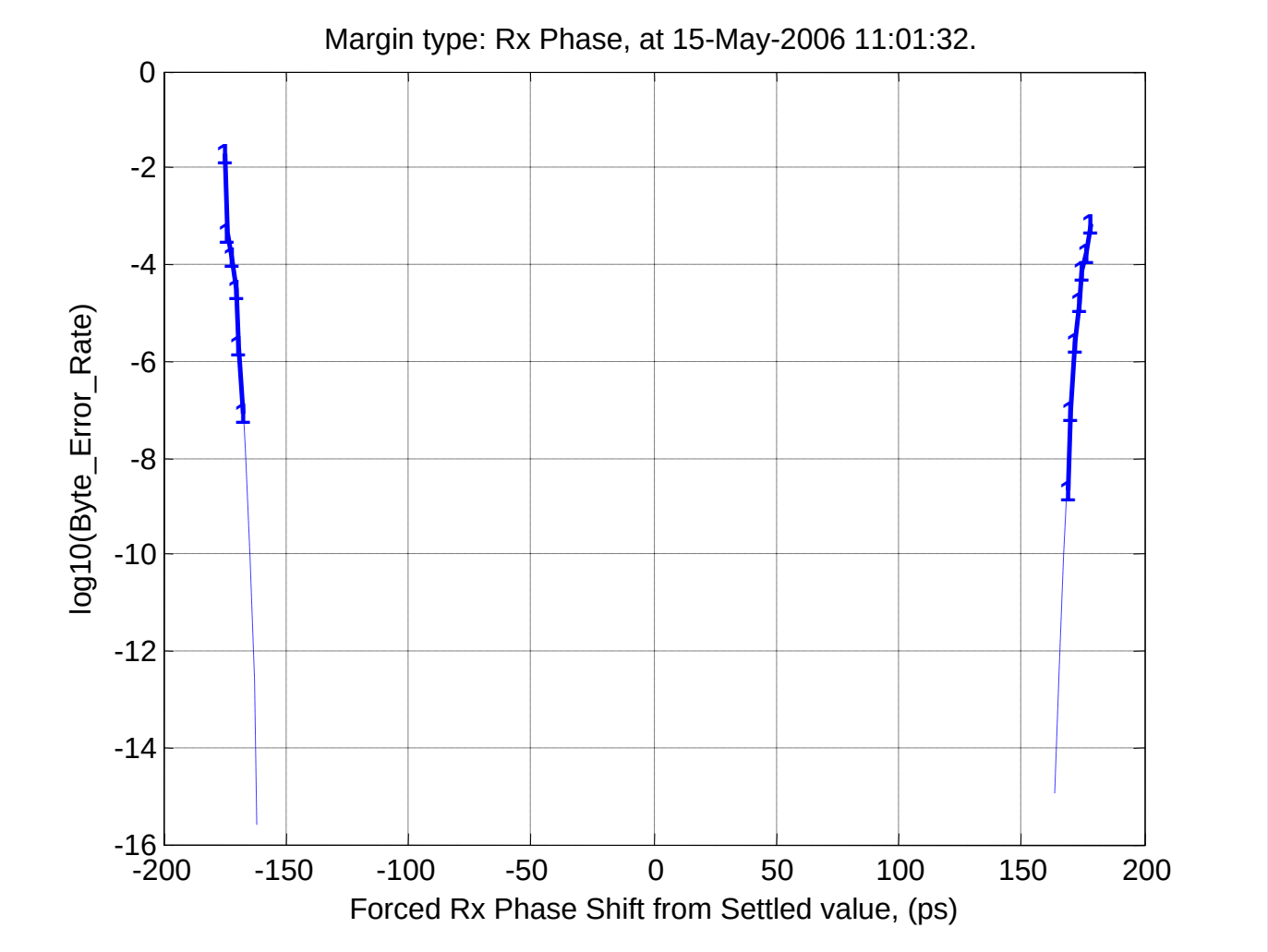
Phase Margining – Internal Test

- Internal Test – add offset to recovered clock phase



✓ Clock recovery is frozen

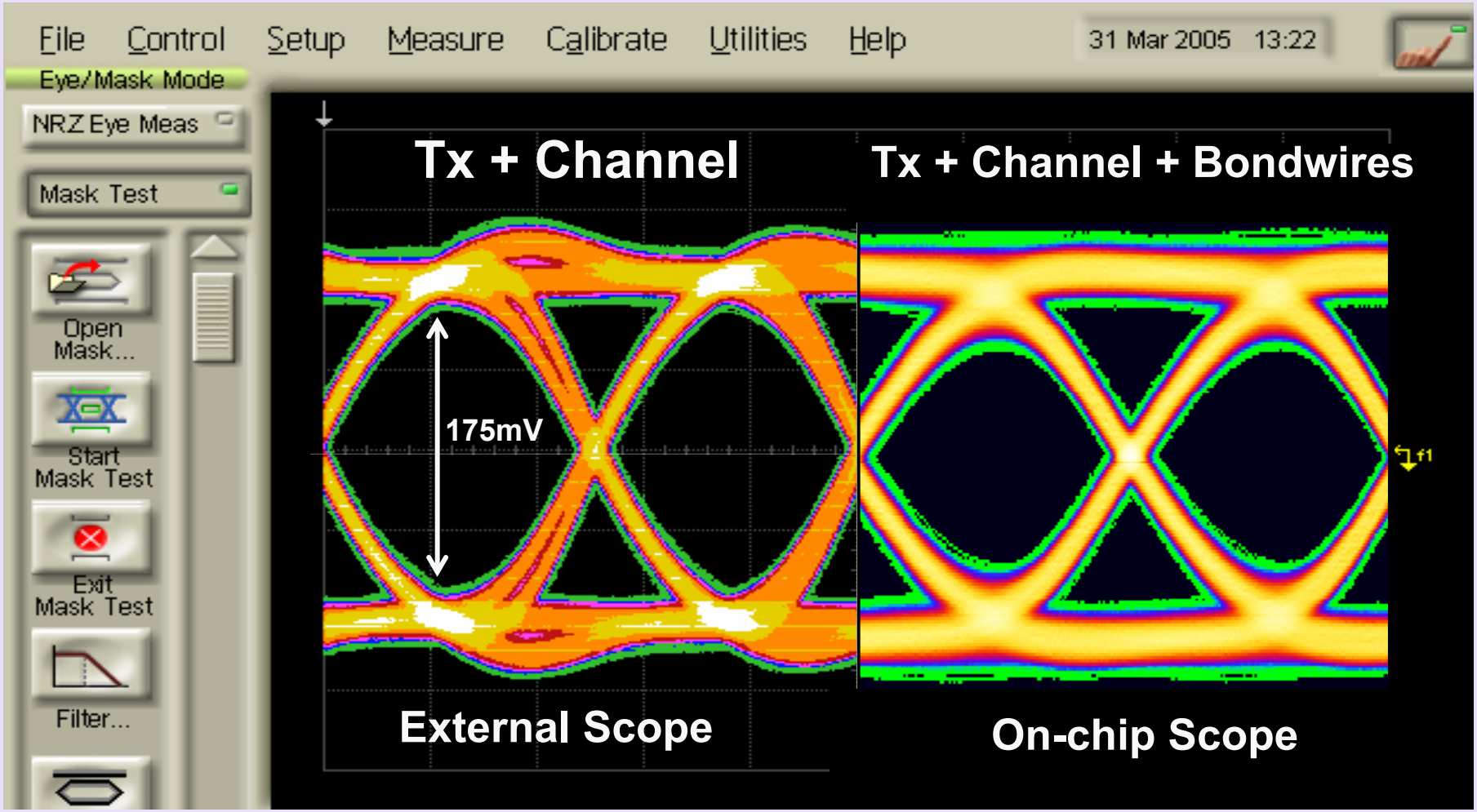
Phase Margining – Bathtub Curve



Signal Integrity: On-chip Scope

- PCIe® minimum Rx eye opening is 175mV at pins – how do we measure it?
  - ✓ Difficult to probe signal right at pins
  - ✓ Effect of package not taken into account.
- On-chip RX scope eliminates these problems
  - ✓ Allows RX eye to be viewed right at Rx comparator inputs
  - ✓ Can view effects of crosstalk, noise
  - ✓ Can help debug problems with signal channel
  - ✓ Invaluable in debugging devices with multiple lanes
- Implemented using existing analog test circuitry

On-chip Scope: Example



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ATE Testing

- Digital Testing Methodology
  - ✓Send digital test vectors in through JTAG interface
  - ✓Do a compare of a digital vector coming out
- Goal different from characterization
  - ✓Time is money
  - ✓Identify failed or marginal parts
  - ✓Sufficient test coverage

ATE Testing of Analog

- Is it possible to test a PCIe® PHY using a digital test methodology ?
- For Synopsys PCIe PHY, all setup functions and results are digital vectors
- All communication with part is through JTAG
  - ✓ Aren't results of all the tests numbers ?
  - ✓ How can they be converted to a form to be of use when the ATE program is stored in vector memory?
- Synopsys PCIe PHY has built-in Compare Functionality
  - ✓ Programmable lower and upper limits
  - ✓ Can check if value of any register lies within these limits

ATE Test Example 1 – Tx Magnitude

- Set up part
- Measure differential output voltage without de-emphasis
  - ✓ Result is ADC output
- Program Compare limits to 0.8V and 1.2V
- Read ADC output to Compare Circuit
- Read output of Compare Circuit via JTAG
  - ✓ Should be 0 (i.e. ADC output >0.8V, <1.2V)

ATE Test Example 2 – Voltage Margining

- Set up part
  - ✓ Part is put in loopback externally
  - ✓ Set up pattern generator and pattern matcher
- Add offset to RX input
  - ✓ Program DAC to provide offset
- Allow device to operate with this offset
- Read the contents of the error counter
  - ✓ Should == 0
- Add a single error
- Set Compare limits to 0 and 2
- Read error counter into Compare Circuit
- Read output of Compare Circuit
  - ✓ Should be 0 (i.e. error counter contents >0, <2)
- A complete test of x16 PHY can be completed in <75ms

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Conclusions: Question

At the beginning, we asked:

"Does it have to be hard to test the high-speed analog part of PCIe® to meet your quality goals? Will test make it hard to adopt PCIe?"

Conclusions: Answer

- The answer is NO, if the PCIe® PHY builds testability into the analog circuitry from the beginning.
  - ✓No additional testing equipment needed.
  - ✓Minimal cost in area.
  - ✓Customer's testing methodology for PHY similar to that used for rest of chip.
- Migrate to PCIe without fear.

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For more information, please contact navraj.nandra@synopsys.com

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Kannan Krishna

R&D Engineer

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