



PCle® Server Validation

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Topics

- Servers
- Areas of Testing
- Approaches
 - ✓ Validation Areas
 - ✓ The Matrix
 - ✓ RAS
- Recommendations

Server

Server?

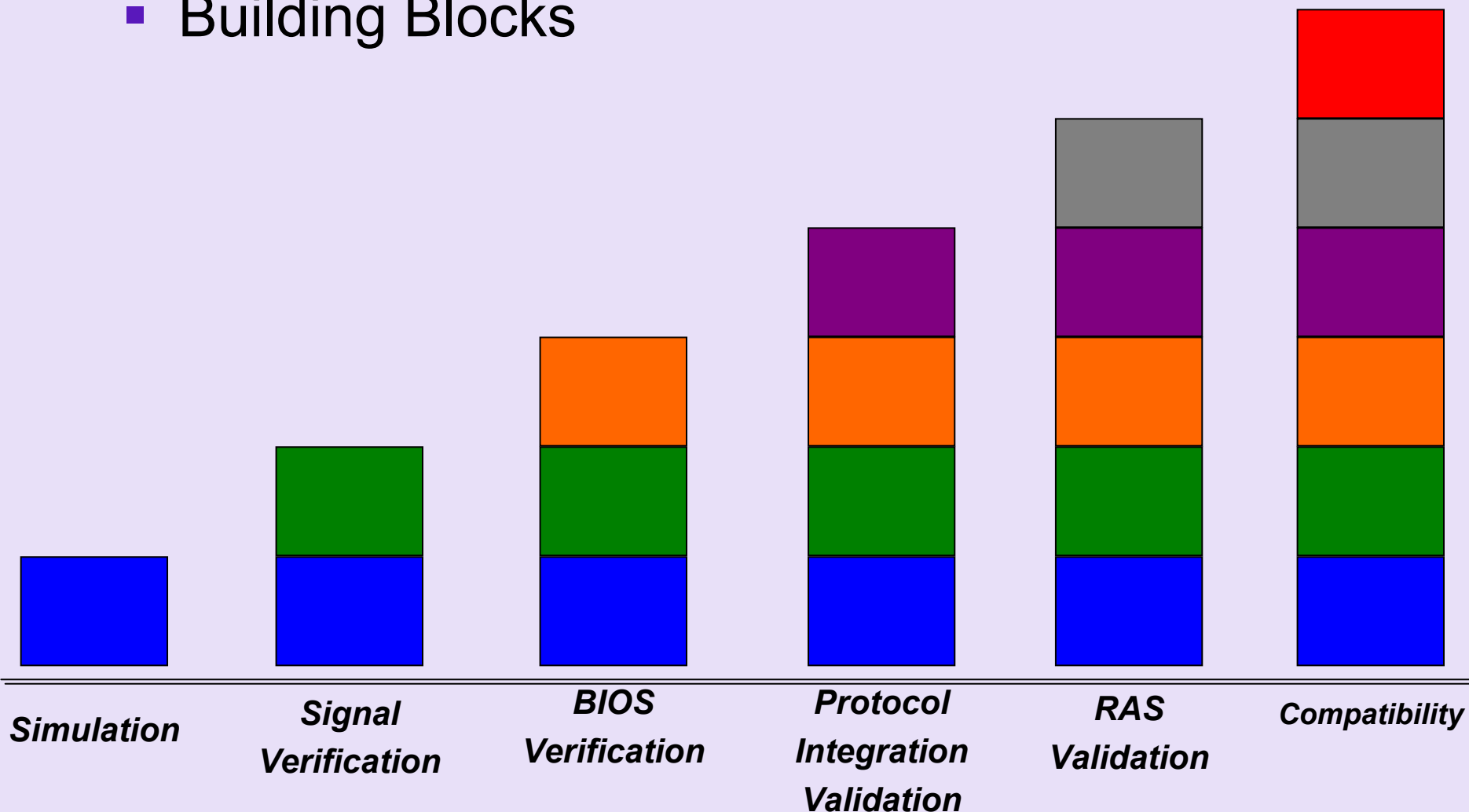
Servers

- A server is a pool of high-end resources (memory, disk, processor, I/O, etc..) for clients / customers
- Servers range from uni-processor to 32-processor Multi-Node NUMA (Non Uniform Memory Addressing) scaleable servers
- Requires High RAS (Reliability, Availability, & Serviceability)
 - ✓ Low tolerance for persistent recoverable and non recoverable events
- All servers need high performance I/O enablement
 - ✓ Compatibility and compliance are key!



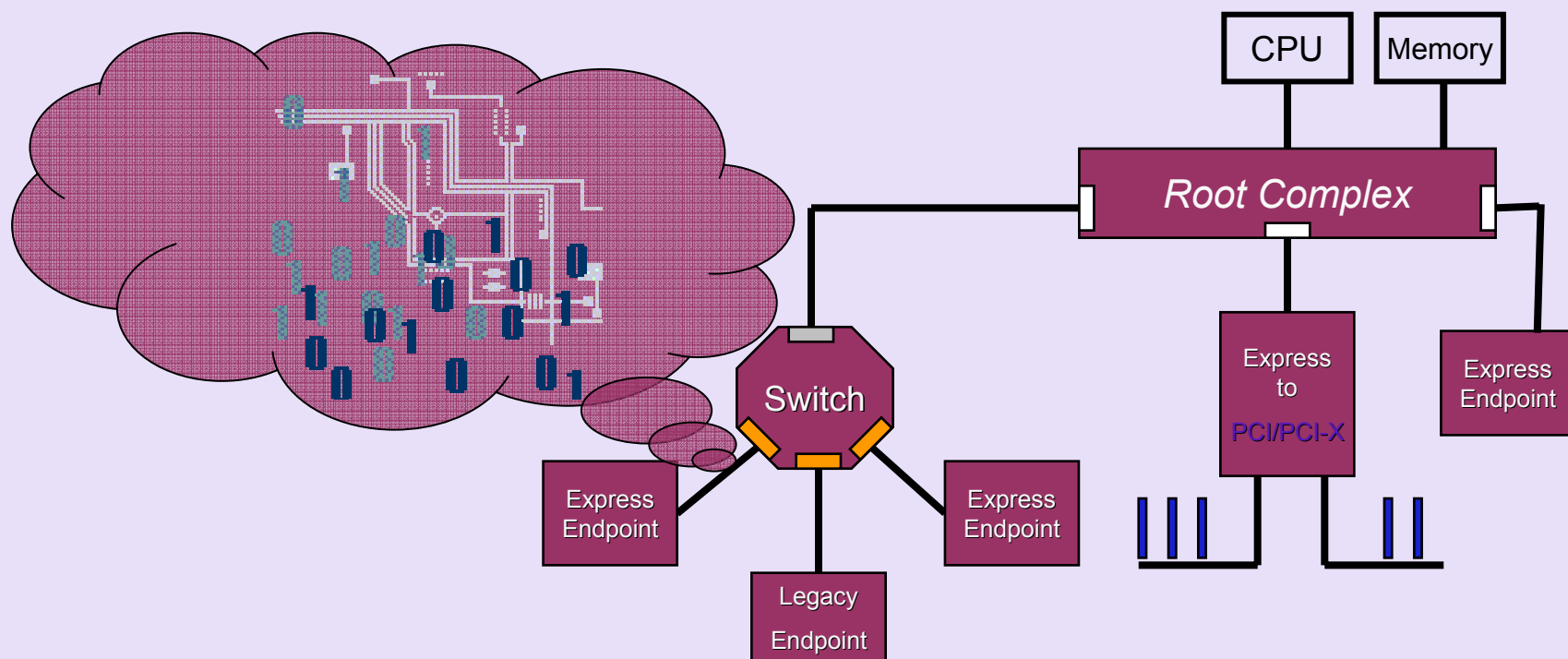
Areas of Testing

- Building Blocks



Areas of Testing

- Simulation
 - ✓ Pre-Hardware / Logic testing
 - ✓ Can be for hardware or Testing Tools



Areas of Testing

Signal Verification

- Physical Bring-up
- Signal integrity measured
 - ✓ Methods
 - PCI-SIG - PCI Express® Electrical Test Fixtures (eye diagrams)
 - Compliance Load Board (CLB)
 - Compliance Base Board (CBB)
 - Custom Analysis Tools
 - Create soft Insertion points for verification
 - Allows check point verifications

Areas of Testing

BIOS

■ System / Device Initialization

✓ Methods

- PCI-SIG - PCI Express Platform BIOS test
 - Uses Protocol Test Card + External Software
 - Simulates various devices
 - Good events
 - Bad events
- Custom Tools
 - Specific BIOS call testing
 - Software
 - Specific BIOS handling
 - Hardware

Areas of Testing

Protocol

■ System / Device Interaction

✓ Methods

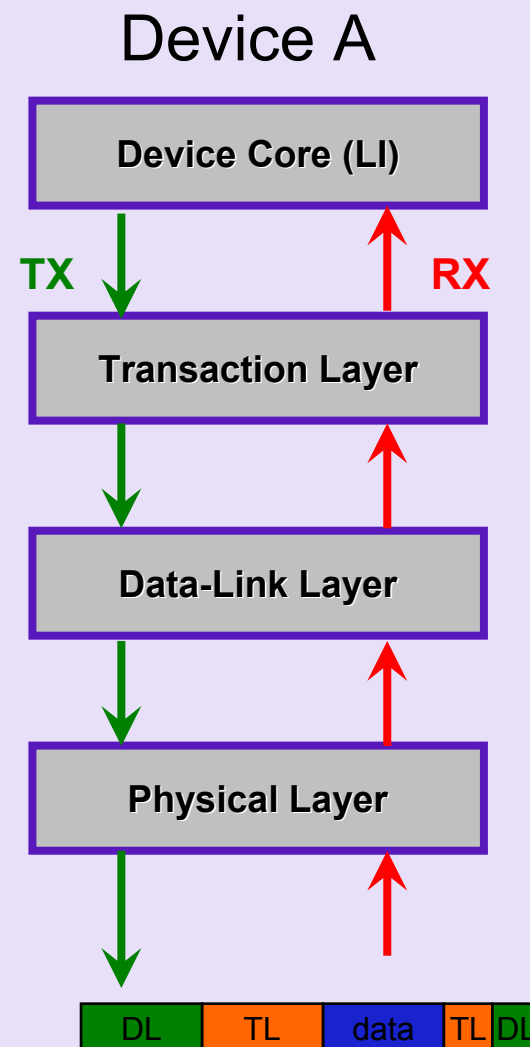
- Custom Tools
 - Software / Hardware
 - Extended verification

✓ Different Levels of the Protocol

- Several layers for validation

✓ Compatibility / Add in-cards

- Several approaches



Areas of Testing

The Matrix Approach

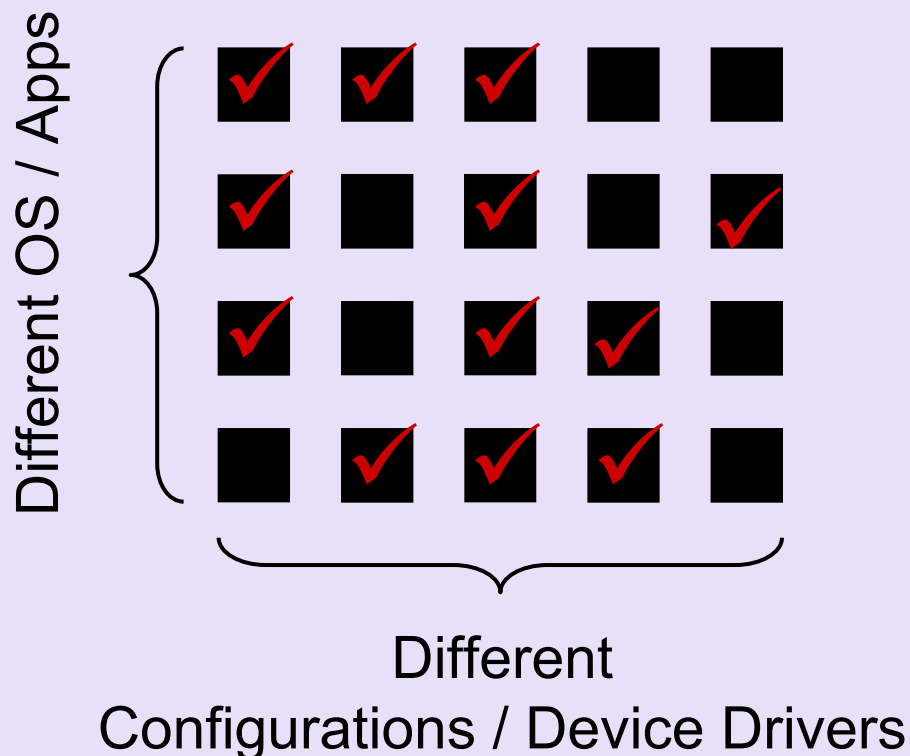
- Use Add-in cards as “configuration validation”
 - ✓ Customize your configuration

- OS(s) used as the hardware enabler
 - ✓ Applications used to drive / load system
 - ✓ Specific to Add-in Card selected

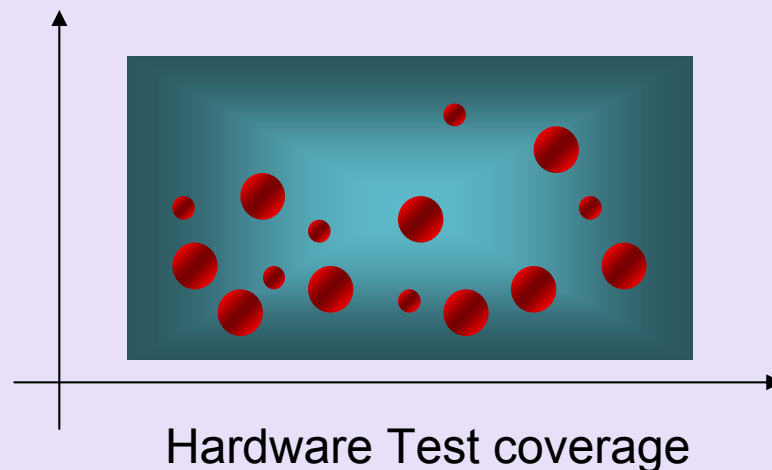
- Time and Coverage NOT directly related
 - ✓ Devices are not designed to do ALL transaction types
 - Size of the devices queue?
 - What are the expected transactions?
 - Does it support....

Areas of Testing

Test Matrix Approach



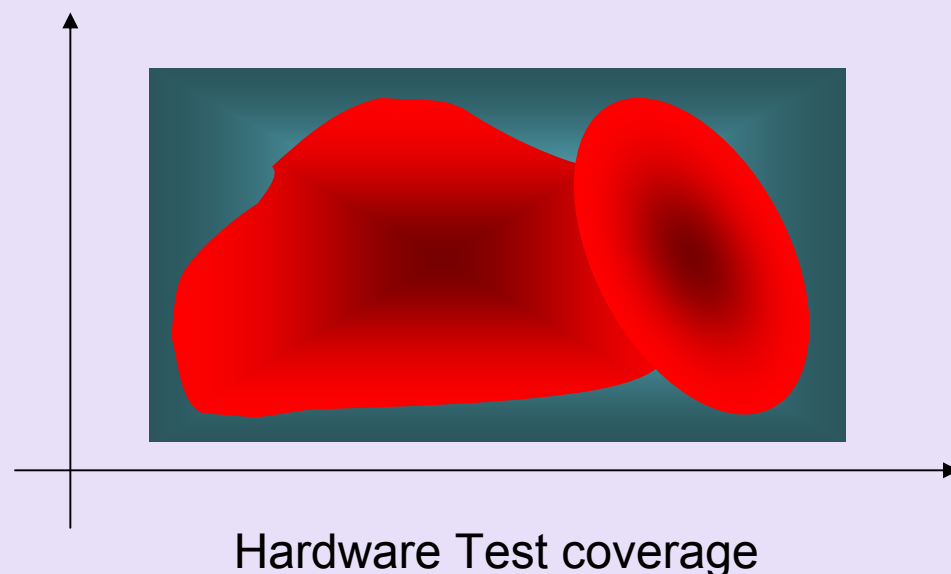
- More hardware coverage using more hardware configurations
- Very time consuming
- Test holes can only be found and verified by knowing the *true* interaction of the device driver with OS.
- OS has direction impact
 - ✓ Access to processors, memory, etc...



Areas of Testing

Hardware direct testing

- Use **“Hardware Test Vehicles”** (HTV)
 - ✓ Protocol Exercisers and Analyzers
- Emulate / Access any system devices directly
- Interact with system components
 - ✓ Memory
 - ✓ CPU
 - ✓ Cache
 - ✓ Other PCI / PCI-X® / PCIe
 - ✓ Interrupts
 - ✓ NUMA (Non Uniform Memory Addressing) Nodes
- Increase integration test coverage
- Focus on subsystem Interactions and coverage
- OS limitation minimized



Areas of Testing

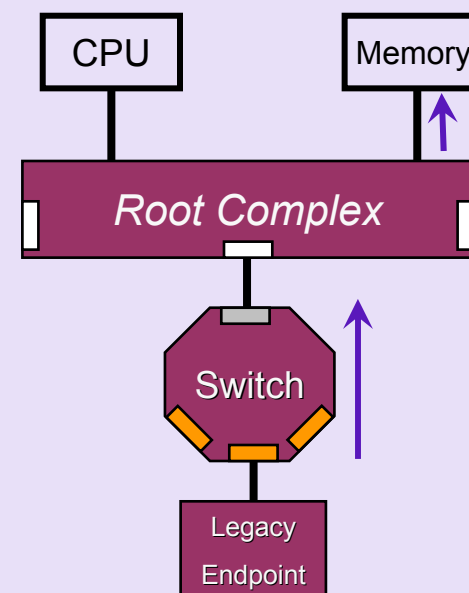
- Many market available for *HTV*
 - ✓ FPGA base and ASIC based
 - Both have advantages and disadvantages
- Allows direct control - Deterministic
 - ✓ To device (Completer)
 - Responses
 - Behavior
 - Timing
 - Etc...
 - ✓ From device (Initiator)
 - System devices targeted
- OS limitations removed
 - ✓ OS Control put in the “back ground”
- Analyzer / Counters
 - ✓ Verify
 - ✓ Debug
- Not a silver bullet
 - ✓ Will not find compatibility issues

Areas of Testing

Method Matters

Memory Target

- ...0000 0001
- ...0000 0010
 - ✓ Stress test
 - Pattern written and Read in burst
 - ✓ Performance test
 - Written once and read back many
 - ✓ Protocol test
 - Pattern written and read back many
 - Changing payload, start at various boundaries, Byte Enables, etc
 - ✓ Positive RAS test
 - Receiver Errors, Bad TLP, Replay Time-out, Replay Number Rollover, etc..
 - ✓ Link retraining

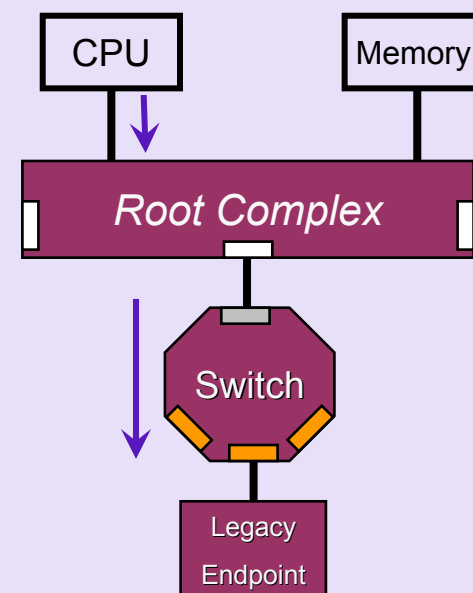


Areas of Testing

Method Matters

Device Target

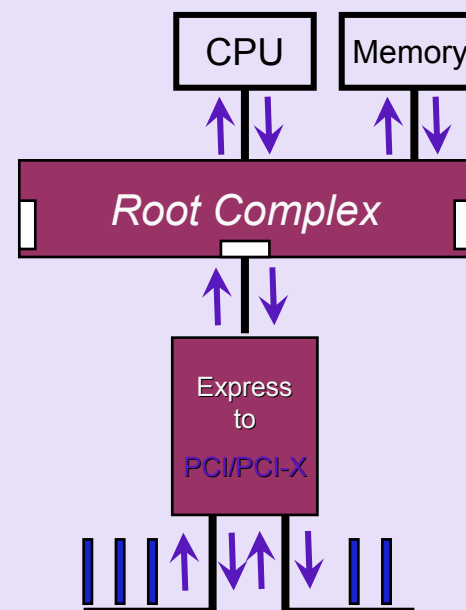
- ...0000 0001
- ...0000 0010
- Behavior and Responses controlled
 - ✓ Stress test
 - Pattern written and Read in burst
 - ✓ Performance test
 - Written once and read back many
 - ✓ Protocol test
 - Pattern written and read back many
 - Changing flow control, Interrupts, Message passing,
 - ✓ Positive RAS test
 - Receiver Errors, Bad TLP, Replay Time-out, Replay Number Rollover, etc..
 - Make part as your standard tests
 - ✓ Link retraining



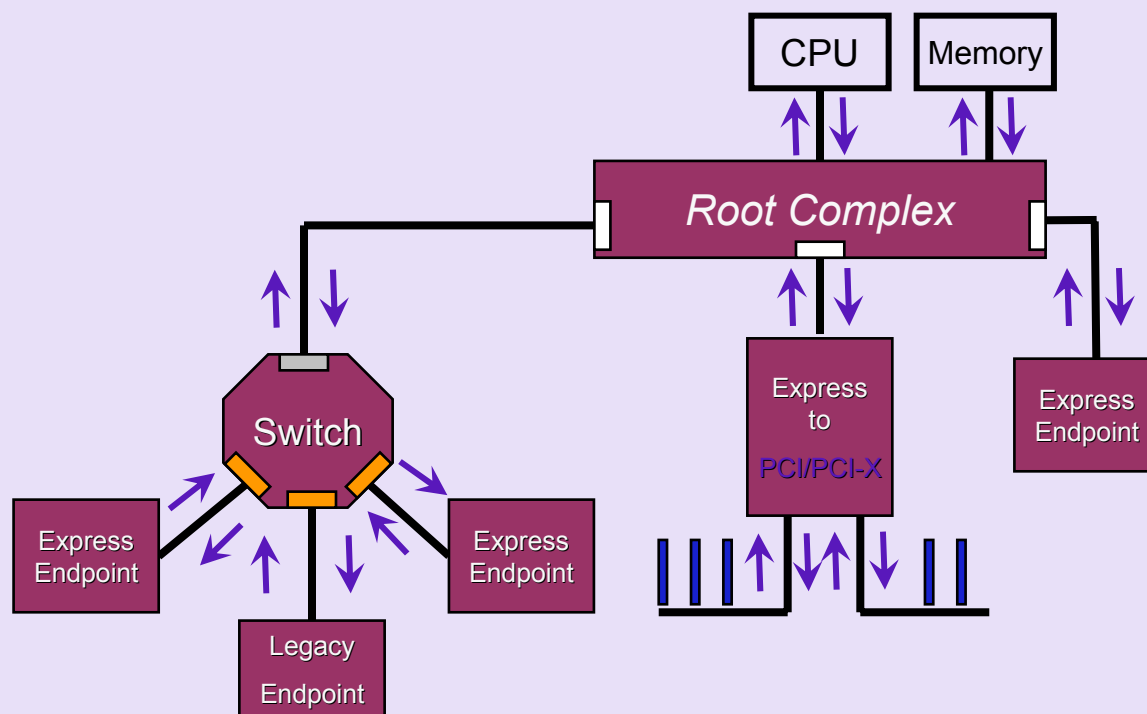
Areas of Testing

- Don't forget about Legacy Buses!
 - ✓ Traffic loading
 - ✓ Compatibility
 - ✓ Starving?

Completed Picture?



Areas of Testing - All



RAS

Reliability, Availability, & Serviceability

RAS - New Challenges

Compare to Legacy

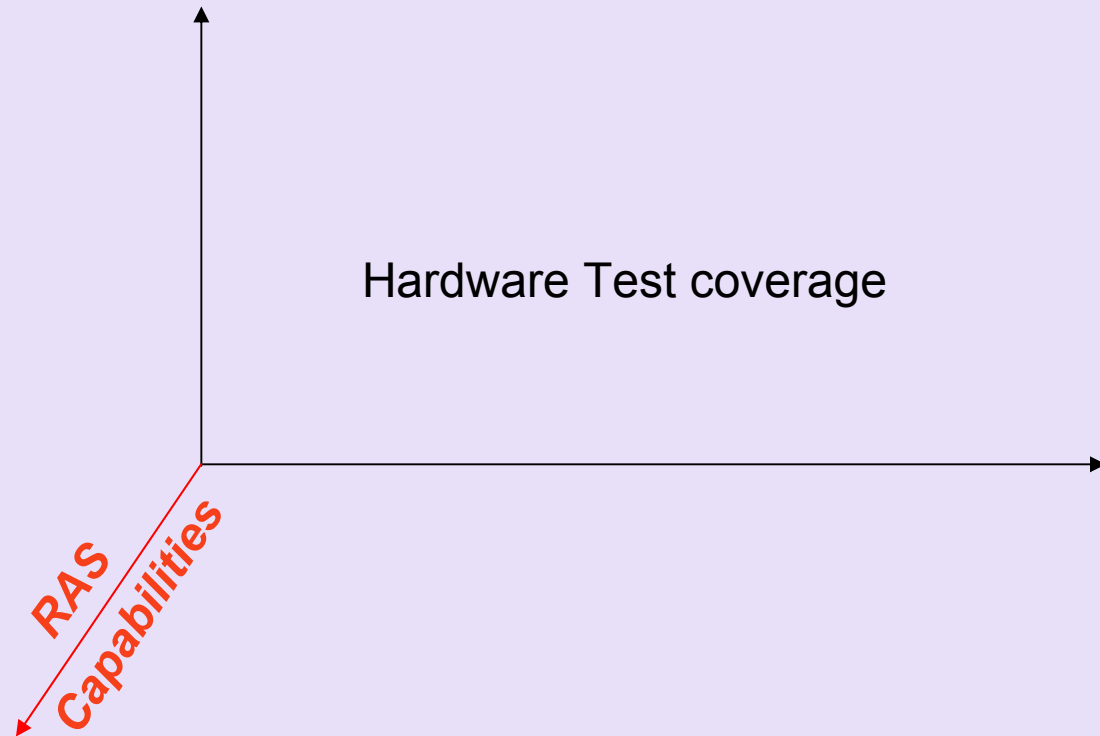
- PCI/PCI-X
 - ✓ Two main types
 - Fatal
 - SERR
 - Parity
 - Master Abort (non config)
 - ...
 - Recoverable
 - Very limited support
 - Requires Device Driver support
 - Retry
 - ...

*** Most errors in Servers are treated as Fatal ***

RAS - New Challenges

RAS Capabilities

- ✓ Error Generation
- ✓ Error Reporting
- ✓ Error Recovery
- ✓ Provisioning
- ✓ Optimization

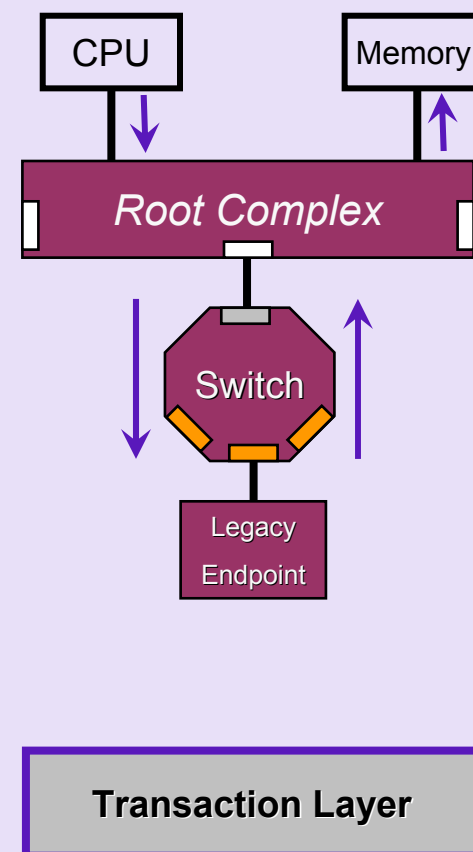


RAS - New Challenges

■ RAS Capabilities

✓ Negative Testing

- Uncorrectable Non-Fatal
 - Unexpected Completion
 - Unsupported Request
 - Completion Abort
 - Completion Time-out
 - Poisoned TLP Received
 - ECRC Failed



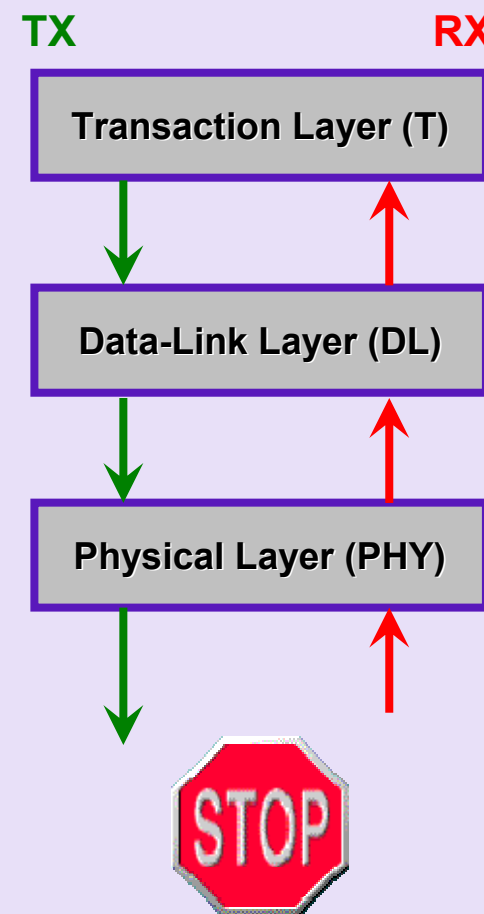
RAS - New Challenges

■ RAS Capabilities

✓ Negative Testing

– Uncorrectable **Fatal**

- Flow Control Protocol Error (T)
- Malformed TLP (T)
- Training Error (PHY)
- DLL Protocol Error (DL)
- Receiver Overflow (T)



RAS - New Challenges

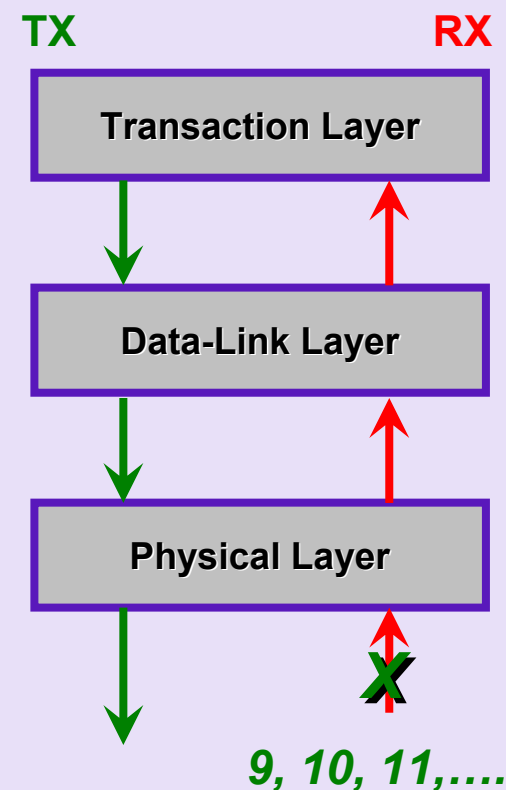
■ RAS Capabilities

✓ Thresholds

- Verify (exceed)
 - Non-Fatal / Correctable
- Action taken
 - i.e. Retraining?
- Reporting
 - Location and information

✓ Systems Responses

- Take the system down
- Recovery



RAS - New Challenges

Must support Legacy and Express

- Insures Software and hardware compatibility
 - ✓ Legacy

- Is advanced error reporting on?
 - ✓ Not a requirement ...

Areas of Testing

Compatibility

Areas of Testing

Device compatibility - Add-in adapters

- Verifying compatibility with
 - ✓ Your System
 - ✓ Your OS
 - ✓ Their Device
 - ✓ Their Device Driver

- Creating a solution
 - ✓ Integrated

Areas of Testing

Device compatibility





















■ System / Device Interaction

✓ Methods

- Insure device is on the Integrator list
 - Limits a number of issues
- OS(s)
 - Signed Drivers
- Lane Width
- Advance Reporting

✓ Reduced Testing Time

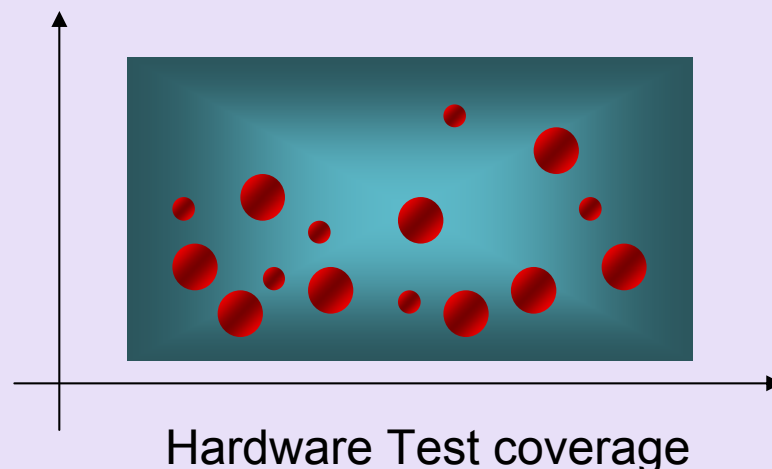
Test Matrix Approach

Different OS					
					
					
					
Device Drivers					

Areas of Testing

Device compatibility as “System Validation”

- Look at cross section of function and capability
 - ✓ Virtual channels?
 - ✓ Number of functions?
 - ✓ RAS?
 - ✓ OS Support
 - Device driver capabilities
 - Equal Support across?
- Lane width and bandwidth
 - ✓ Not an absolute
 - Types of transactions
- Closed System?
 - ✓ Know configuration



Areas of Testing

Device compatibility as “System Validation”

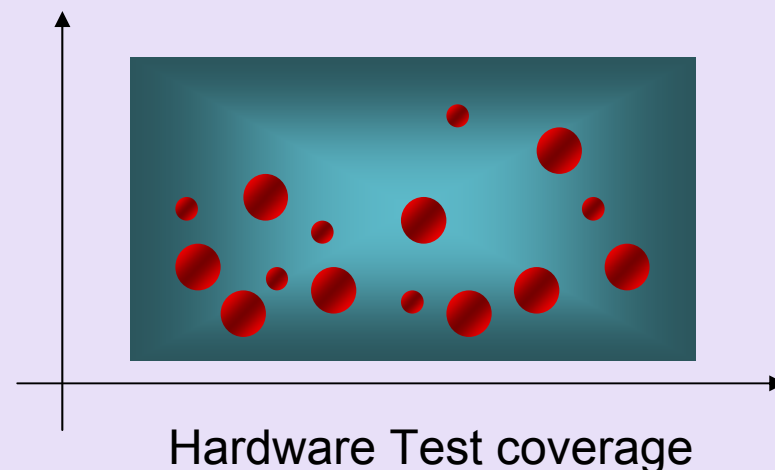
■ Issue arise on

✓ Lane width

- Running in every slot?
 - x4 in a x8 slot?

✓ Combinations of devices themselves

- OS, Driver Version, Other devices
 - Similar, different
- Application to drive the devices



Recommendations

- Recommendations
 - ✓ Signal Verification Feed your testing process
 - Most stressful patterns in different subsystem
 - ✓ Matrix is hard to manage
 - Look at devices testing as compatibility
 - ✓ Touch each layer of the protocol
 - But don't get lost in the combinations
 - ✓ Compatibility is a joint partnership
 - Out of the box testing
 - ✓ RAS is key to success
 - Detection is only one aspect
 - Positive and Negative testing insure overall quality

Recommendations

- Recommendations
 - ✓ No easy straight solution
 - Most solutions are a combination
 - ✓ Compliance allows a common measurement
 - Helps reduce chances of hardware churn
 - Early compatibility testing
 - ✓ Compare Hardware Test Vehicles
 - Many are on the market
 - All have + and –
 - Cost can be a barrier

Thank you for attending the
PCI-SIG Developers Conference 2006.

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