
PCI
SIG®

PCIe™ External Cable Requirements & Definitions

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Session Outline

- PCI Express® External Cabling
  - ✓Why External Cabling?
  - ✓Usage Models
    - Examples
  - ✓Current Definition
    - Sideband Signals
    - PCIe Signaling
      - Loss Budgets Gen1 & Gen2
      - Jitter Budgets Gen1 & Gen2
      - Eye Mask Gen1
    - Additional Considerations
  - ✓Specification Status
  - ✓Call To Action

Why PCI Express Cabling?

- PCI-SIG® members were surveyed in April 2003
  - ✓Responses representing several market segments indicated that cabling was required
    - Extend PCI Express protocol / functionality across arbitrary distances and packaging
- As a result the Cabling Working Group was formed
  - ✓Charter is to create a specification that focuses on
    - Standard cable connectors
    - Copper cabling attributes and electrical characteristics
    - Connector retention
    - Identification/labeling
  - ✓This is **NOT** a replacement for cabling to USB or 1394 peripherals!

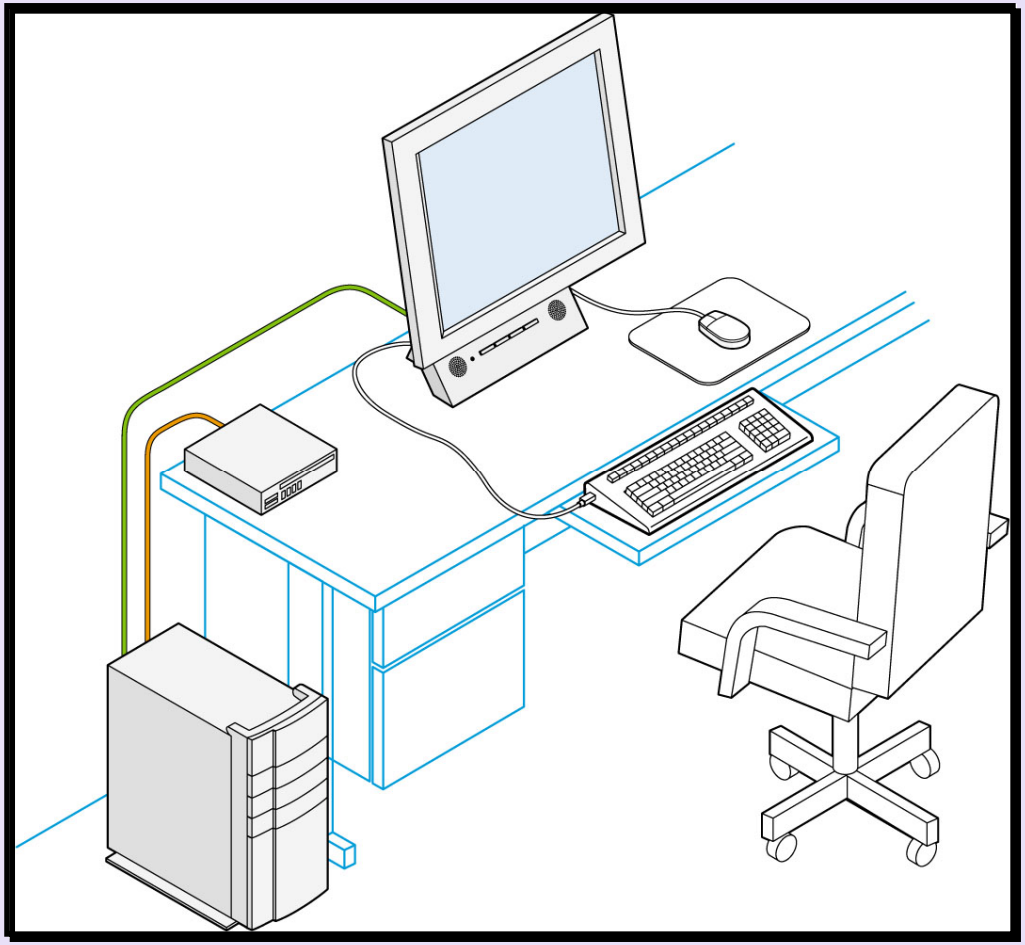
PCI Express External Cabling Usage Models

Cabled PCIe Usage Models

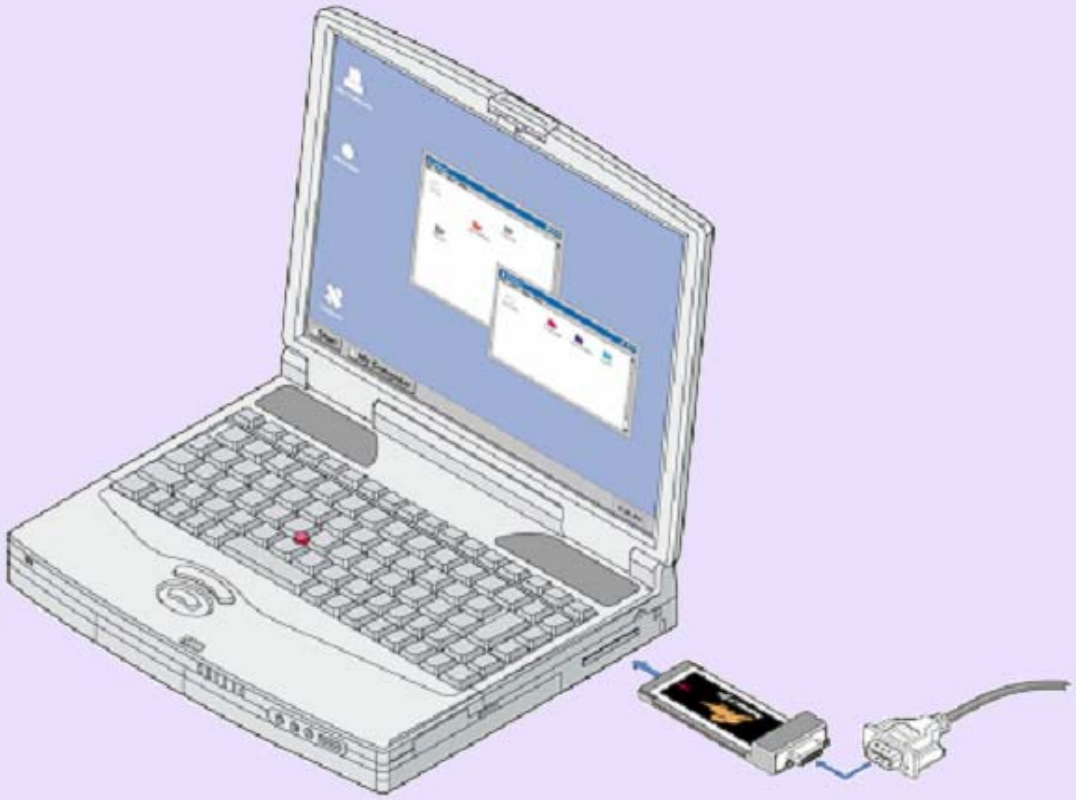
- Expansion I/O
  - ✓ Potential Implementations:
    - Mobile / Desktop / Server platform
    - ExpressModule* module
    - Test & Measurement chassis
    - ExpressCard
- Split-system (disaggregate) desktop
- Tethered docking for mobile platforms
- External graphics controllers
- Communication equipment
- Embedded applications
    - High speed data transfer within large office equipment

*"ExpressCard" is a trademark of PCMCIA.

Split System Application



ExpressCard* Module Implementation



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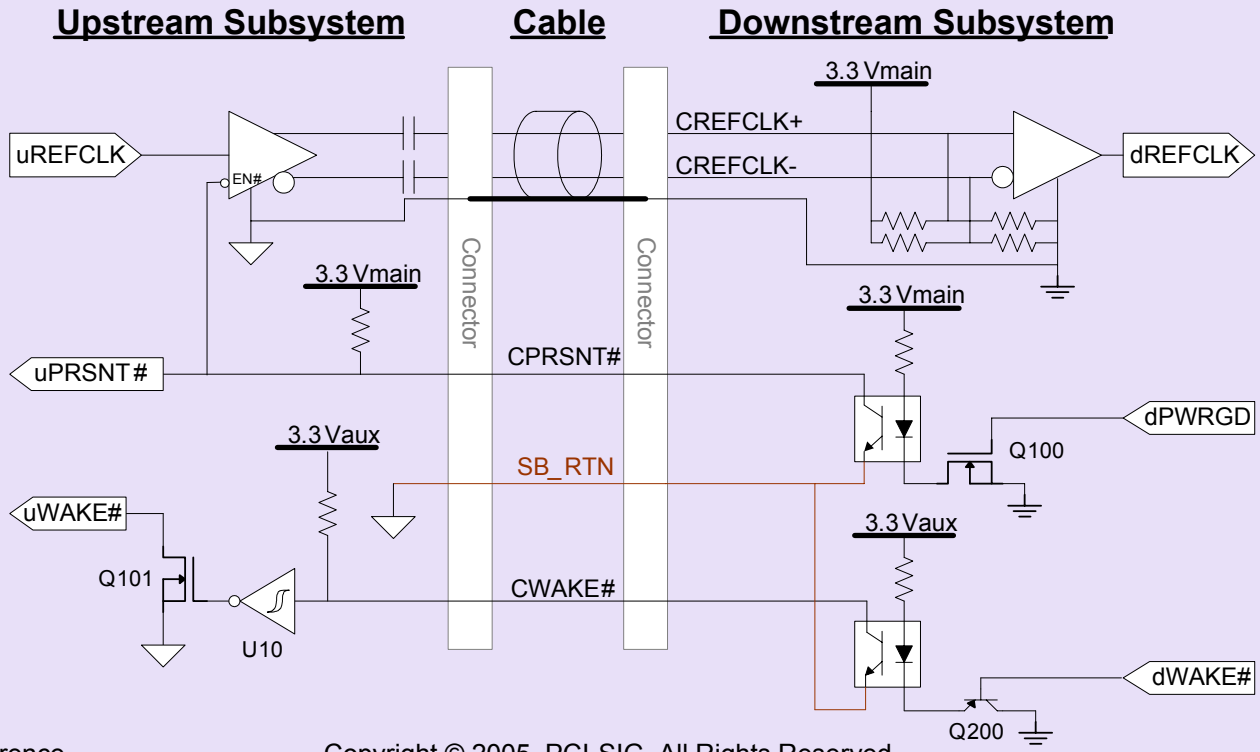
PCI Express External Cabling Preliminary Sideband Definition

Sideband Signal List

- Objective: compatibility with existing silicon and software
- Signals and key reasons for their inclusion:
  - ✓ CREFCLK (Cable Reference Clock, 100MHz)
    - Supports spread spectrum clocking & Phase Jitter considerations
  - ✓ CPRSNT# (Cable Presence Detect)
    - Indicates a downstream subsystem is present
    - Provides a Power Good status of the downstream subsystem
  - ✓ CWAKE# (Cable Wake)
    - Needed for suspend / resume
  - ✓ CPWRON (Cable Power On)
    - Needed if downstream subsystem is essentially a slave to the upstream root complex, for suspend / resume functionality
  - ✓ CPERST# (Cable PCIe platform Reset)
    - Allows for full transparency with remote system expansion

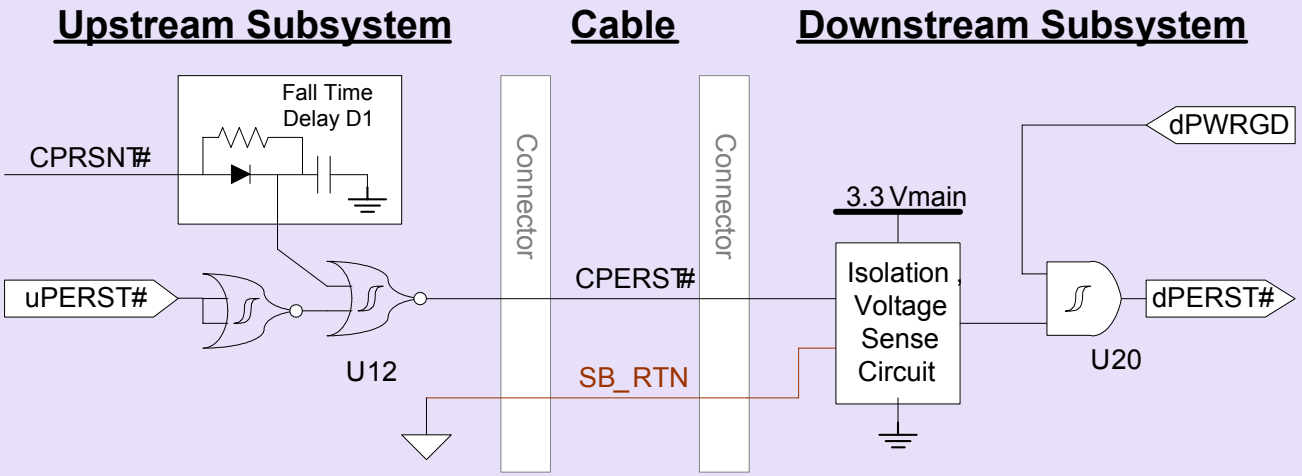
CREFCLK, CPRSNT# & CWAKE#

- CREFCLK is an AC-Coupled differential signal
  - ✓ Source and load termination on RefClk
    - – Block diagram for explanation only, source termination not shown
  - ✓ Requires receiver biasing
  - ✓ Output is enabled with CPRSNT#



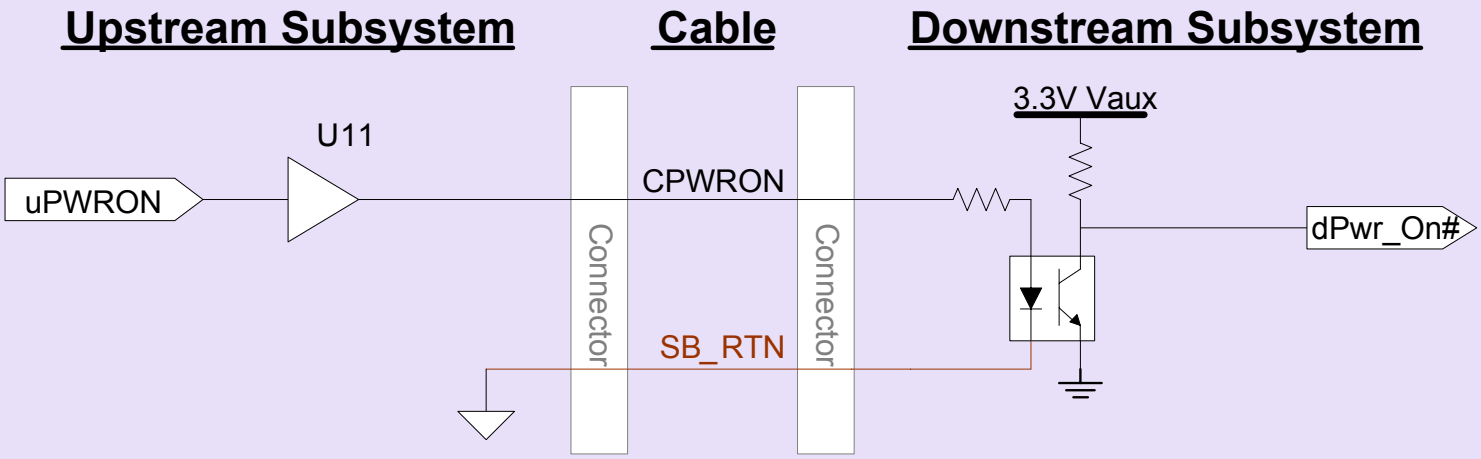
CPERST#

- CPERST# stays asserted until CPRSNT# is asserted and uPERST# is de-asserted
- The isolation / voltage sense circuit for CPERST# within the downstream subsystem might need to account for ground potential differences
- Delay D1 provides minimum CPERST# period following Hot Plug
  - ✓ Block diagram is for explanation purpose only



CPWRON

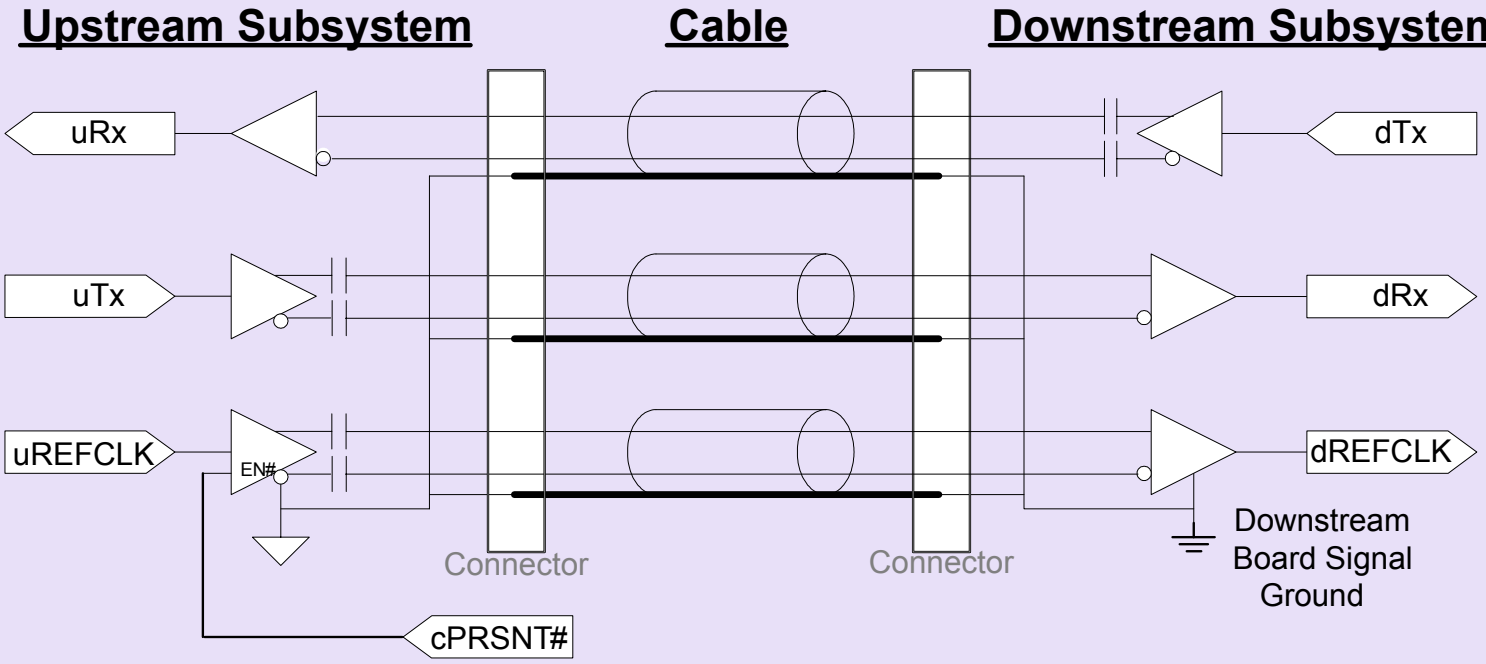
- Following two usage scenarios illustrate some key considerations:
  - ✓ Allows for automatic power sequencing of downstream subsystem (requires fast power-on at downstream device)
  - ✓ Transition main power in downstream subsystem when entering into and exiting from power management states
  - ✓ Block diagram is for explanation purpose only



PCI Express External Cabling Preliminary Insertion Loss & Jitter Budgeting

PCIe Signaling

- Upstream & downstream subsystem and cable loss and jitter budgets provided
  - ✓ Cable budget includes mated connectors at both ends



Inter/Intra Pair Skew

- Inter pair skew is not a critical parameter, 2nsec is currently specified for the channel
- Intra pair skew is not as tightly controlled within copper cabling as might be desired
  - ✓ Intra pair skew negatively impacts loss and jitter while increasing EMI risks
  - ✓ Through establishing a lump sum budget for the cable, inclusive of mated connectors, flexibility has been provided for implementing price / performance tradeoffs while meeting set requirements
  - ✓ A maximum intra pair skew of 0.2UI is recommended for Cabled PCIe applications

PCIe Gen1 Loss Budget

Insertion loss	Symbol	@ 1.25 GHz (dB)	@ 625 MHz (dB)
Total Loss	L_{Total}	< 13.20	< 9.20
Upstream Subsystem	L_{UT} L_{UR}	< 1.75 < 1.50	< 1.00 < 0.80
Cable and Connectors	L_{C}	< 9.95	< 7.4
Downstream Subsystem	L_{DT} L_{DR}	< 1.75 < 1.50	< 1.00 < 0.80

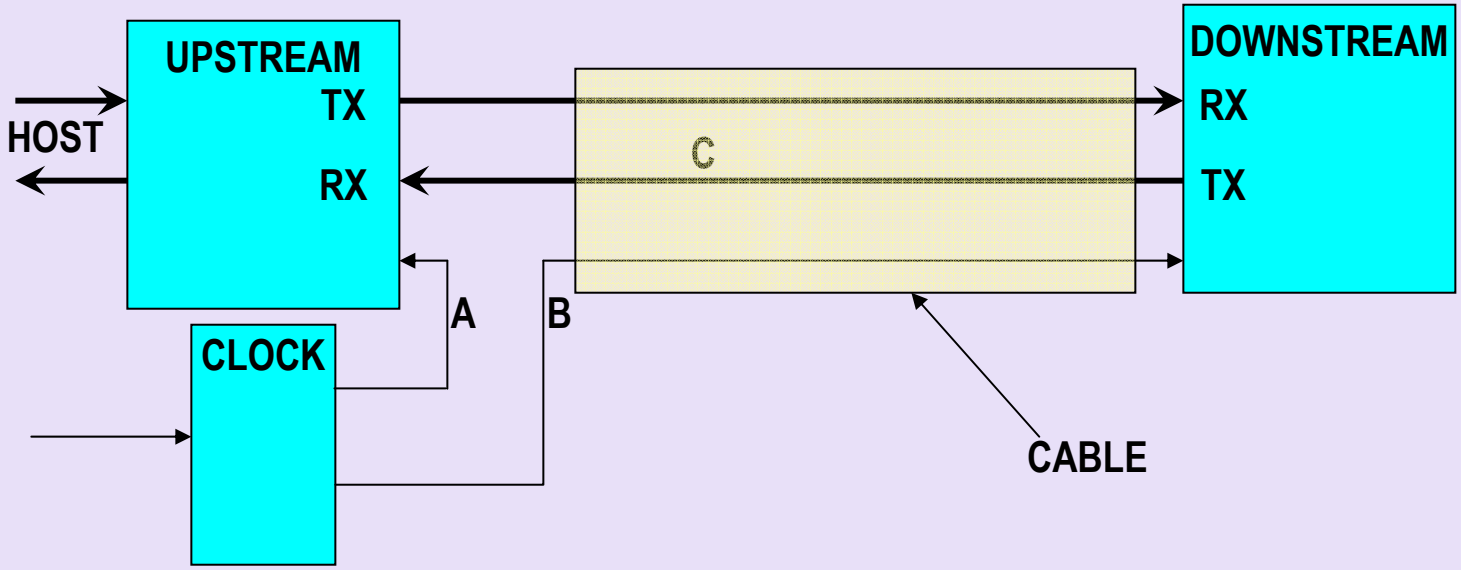
PCIe Gen2 Loss Budget

Insertion loss	Symbol	@ 2.50 GHz (dB)	@ 1.25 GHz (dB)	@ 625 MHz (dB)
Total Loss	L_{Total}	< 16.50	< 10.00	< 6.70
Upstream Subsystem	L_{UT} L_{UR}	< 3.00 < 2.50	< 1.75 < 1.50	< 1.00 < 0.80
Cable and Connectors	L_C	< 11.00	< 6.75	< 4.9
Downstream Subsystem	L_{DT} L_{DR}	< 3.00 < 2.50	< 1.75 < 1.50	< 1.00 < 0.80

Preliminary

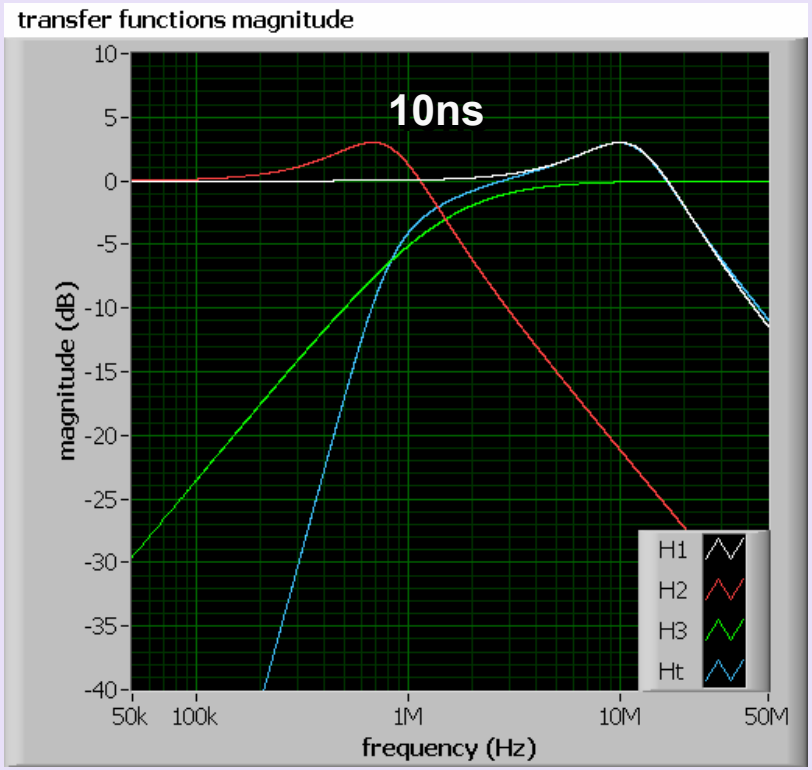
Signal Delay Calculation Evaluating Phase Jitter Impact

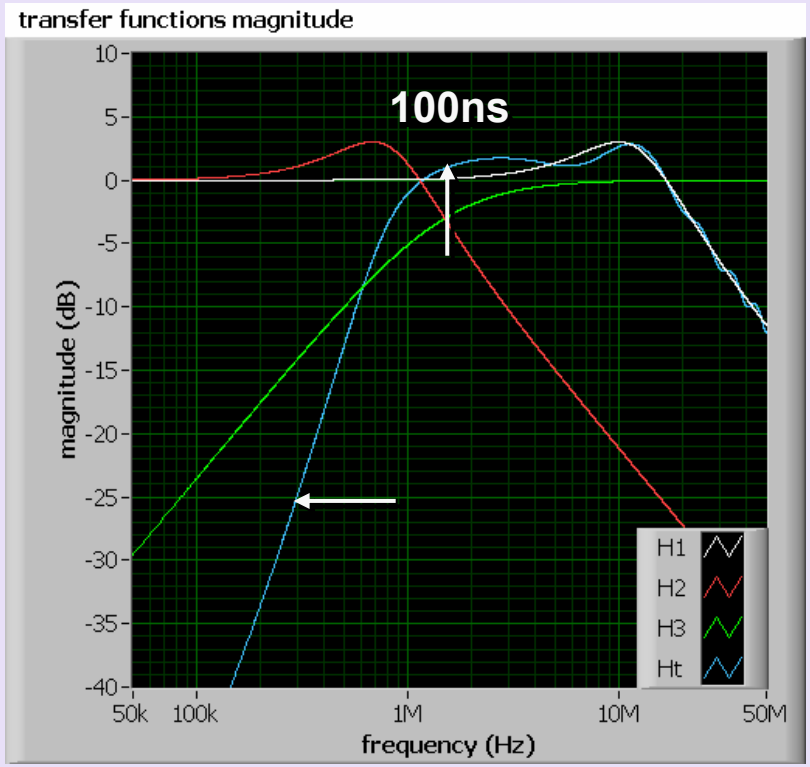
- Phase delay between upstream RX and upstream RefClk
  = (B + C – A) * Tpd = 50nsec for 5 meter cable
- Additional 10nsec budget for component delay differences
- Negative impact on “Eye Closure” transfer function



Phase Jitter Impact from Cable

- Images show impact from 10ns versus 100ns roundtrip delay
- Increase in eye closure from RefClk phase jitter components up to about 6MHz





Gen2 Phase Jitter Calculations

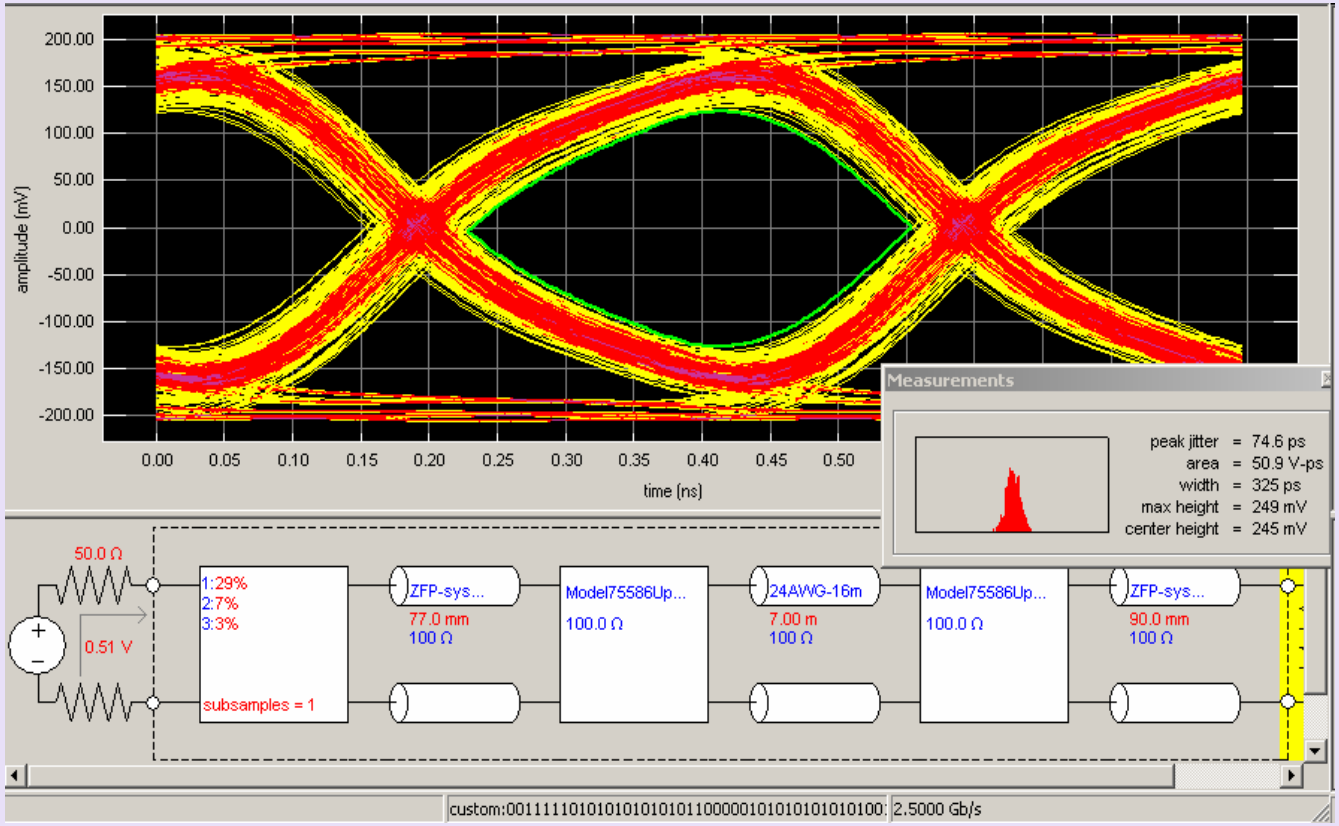
	Dj	Rj (RMS)	Rj @ 10(-12)	
Transmitter	30.0	1.4	20.0	psec
Receiver				psec
Roundtrip delta (est.)			15.0	psec
Reference Clock	0.0	4.2	43.6	psec
Sum Dj	**30.0**			psec
RSS Rj		**4.4**	**61.9**	psec

Tj max @ RX	120	psec
Acceptable Dj	58.1	psec
Channel Dj	**28.1**	**psec**

Preliminary

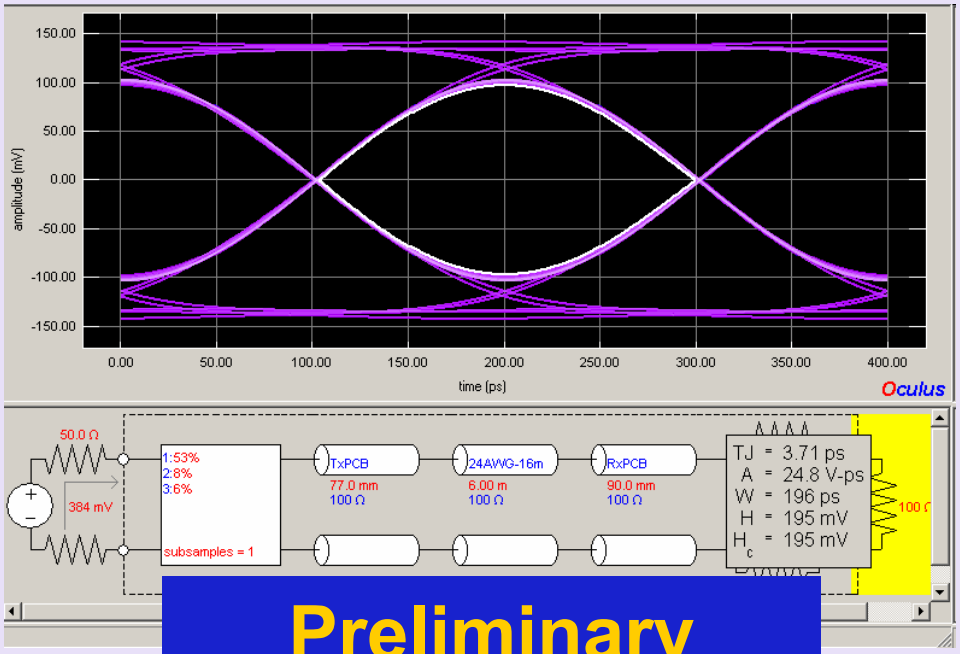
Gen1 Simulation Results

- 2.5Gb/s, 7 meter / 24AWG
  - ✓ 15% random jitter
  - ✓ No crosstalk



Gen2 Simulation Results

- 5.0Gb/s, 6 meter / 24AWG
  - ✓ 0% random jitter, No crosstalk, No connectors
  - ✓ Does not include system level jitter
  - ✓ Includes passive equalization
- Impact from crosstalk could be significant

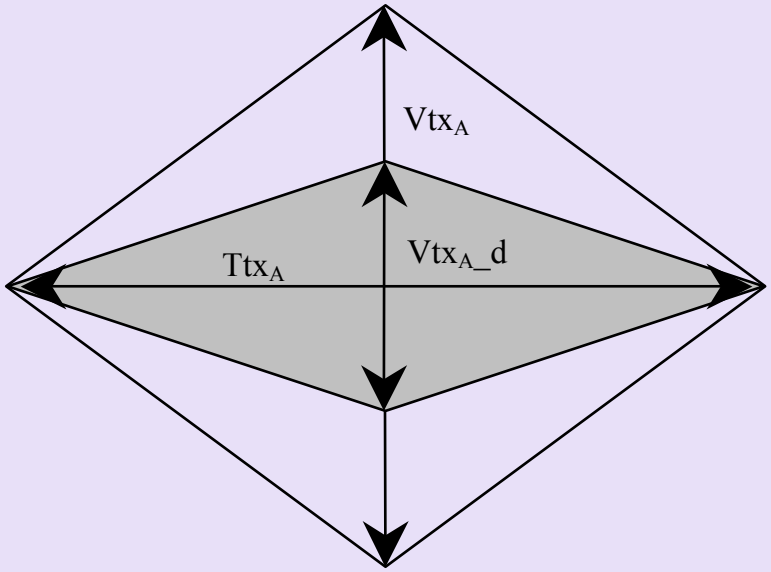


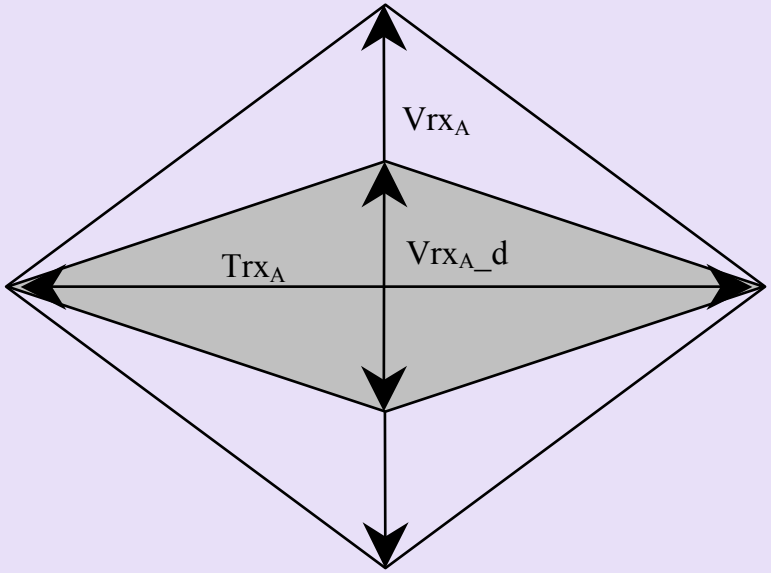
Preliminary

Gen1 Compliance Mask

TX Parameter	Value	Notes
Vtx_A	>= 620mV	1, 2, 4, 5
Vtx_A_d	>= 429mV	1, 2, 4, 5
Ttx_A @ BER 10^{-12}	>= 296ps	1, 3, 4
Ttx_A @ BER 10^{-6}	>= 309ps	1, 3, 4

RX Parameter	Value	Notes
Vrx_A	>= 219mV	1, 2, 4, 5
Vrx_A_d	>= 200mV	1, 2, 4, 5
Trx_A @ BER 10^{-12}	>= 234ps	1, 3, 4
Trx_A @ BER 10^{-6}	>= 247ps	1, 3, 4





PCI Express External Cabling Other Considerations

Long Cable Considerations

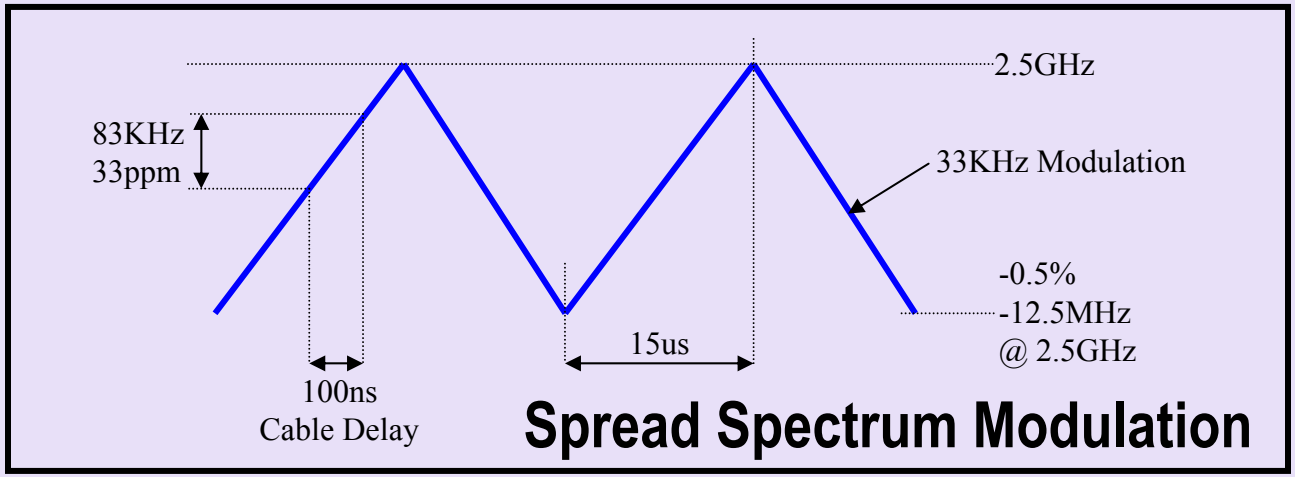
- The PCIe Base specification provides Flow Control Update Latency Guidelines (Table 2-28)
- Silicon provides limited Retry Buffer storage and Credit capability
  - ✓ More of a concern with small packets with increased roundtrip delay due to Ack/Nack latency
- A 100nsec roundtrip delay translates to 400 symbol times for a x16 Link
  - ✓ Add largest packet size supported for calculating Ack/Nack latency
- Can introduce undesired Physical Layer Throttling
  - ✓ Needs to be considered with increased cable length

Long Cable Cons. (cont.)

- The PCIe Base specification provides Replay Timer Guidelines (Table 3-4)
  - ✓ Timer is reset any time an Ack/Nack DLLP is received
  - ✓ Direct impact from roundtrip delay
  - ✓ Potential repeat of TLP that has been received
- Can affect bandwidth due to unnecessary replay
- Can confuse state-machines due to unexpected replay
  - ✓ Needs to be considered with increased cable length

Clock Accuracy & Elastic Buffer Size

- A 100ns roundtrip delay introduces a 33ppm error
  - ✓ Changes polarity at different modulation slopes
  - ✓ Results in 67ppm change at peaks and valleys during 200ns period
  - ✓ Since this is a common clock implementation this is well within the +/- 300ppm PCIe Base Spec requirement
  - ✓ Main concern is the effect from the Periodic Jitter increase
- The Elastic Buffer as defined by the PIPE and PCIe Base specifications is calculated based on this +/-300ppm



PCI Express External Cabling Current Status

Cabled PCIe Spec Status

- Decision has been made to support Gen2 with first release of specification
  - ✓ Circumvent risk of architecture changes for Gen2
- Connector selections are being evaluated for Look & Feel mainstream markets expect
- Ease of Use effort is underway to ensure connectors are user friendly
- Schedule Timeline
  - ✓ Cable spec release anticipated to shortly follow the release of the Gen2 signaling PCIe Base specification

Call To Action

- PCI-SIG members should review the draft specifications when made available and provide your feedback!
- Develop your market requirements for PCI Express cabling and provide input to connector and cable suppliers

Thank you for attending the
PCI-SIG Developers Conference 2005.

For more information please go to
www.pcisig.com

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