Signal Integrity Challenges and Design Practices on Mobile Platforms

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Agenda

- Overview
- Mobile platform focused requirements
- Impedance optimizations
- Rx / Tx Routing optimization
- Layer transition optimization
- Impact of advanced stackup configurations
- Summary

Overview

- As the industry moves to PCI Express® 2.0, boosting data-rates from 2.5GT/s to 5GT/s, we look at some key factors affecting mobile-platform signal integrity and suggest design practices on the silicon package and Printed-Circuit-Board to overcome these challenges.
- Some of these strategies* include:
  - ✓ Adjusting board and package impedances in order to optimize signal integrity and board routing for dense mobile-platform layouts
  - ✓ Assessing the impact of transmitter/receiver interleaved, semi-interleaved, and non-interleaved routing on the board and package
  - ✓ Considering the impact of via stubs, routing layers, and advanced stackup configurations to optimize performance on a mobile platform

*These are recommendations of the authors of this presentation and are not PCI-SIG specifications

Mobile Focused Requirements

- Focus on low-power
  - ✓ Need for low swing drivers
- Implemented on boards with multiple layers
  - ✓ Non-interleaved routing is a good option
  - ✓ Need to optimize layer transitions
  - ✓ Potential for dual-stripline routing
- Compact mobile designs require focus on tight routing
  - ✓ Optimizing the differential impedance target on package and channel
  - ✓ High-density interconnect may be used for small form factor designs

Impedance Optimizations

Impedance Optimizations

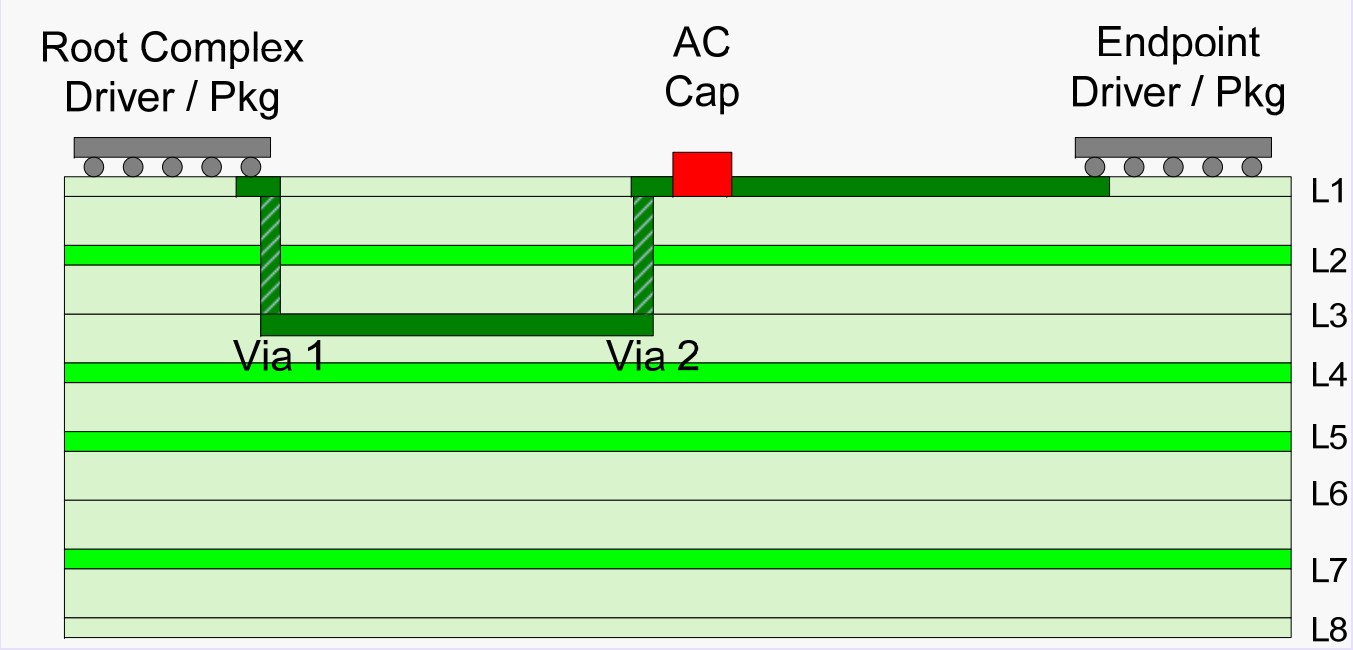
- Analyzed various differential impedance targets on the root complex package, the motherboard, and the endpoint package on the motherboard at 5GT/s

	Root Complex Pkg	Motherboard	Endpoint Pkg
Case 1	85 Ω	85 Ω	85 Ω
Case 2	90 Ω	90 Ω	90 Ω
Case 3	95 Ω	95 Ω	95 Ω

- Need to select the optimal impedance for signal integrity and routability

Case Study Topology

- Considered single routing topology with a combination of stripline and microstrip routing
- Simulated 1 – 10” on the motherboard
- Set the driver and receiver termination values to 100 Ohms differential while changing the package and channel impedance to 85ohms

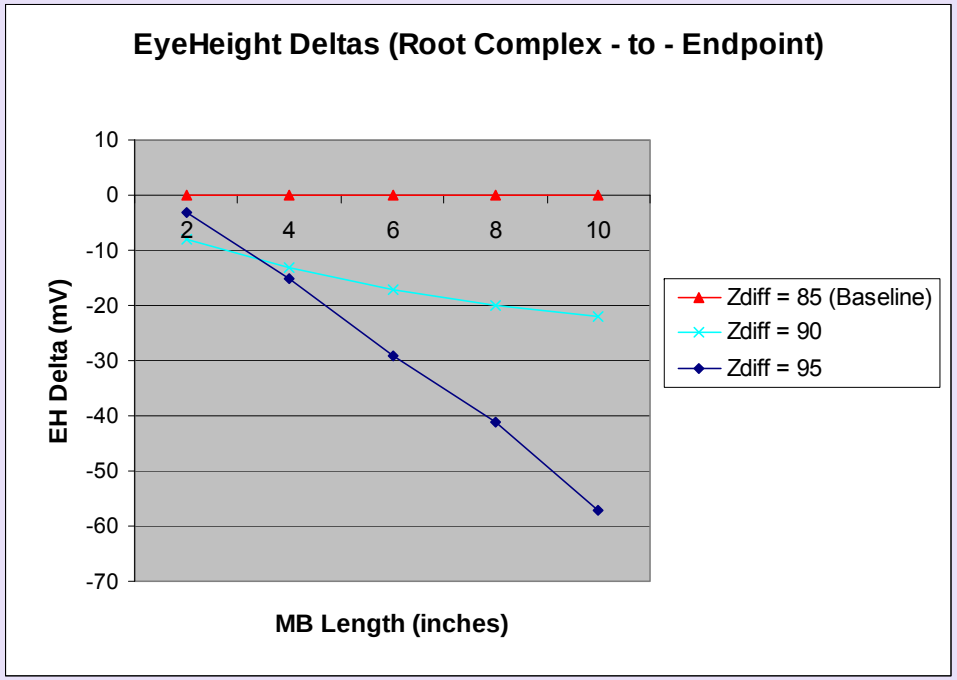


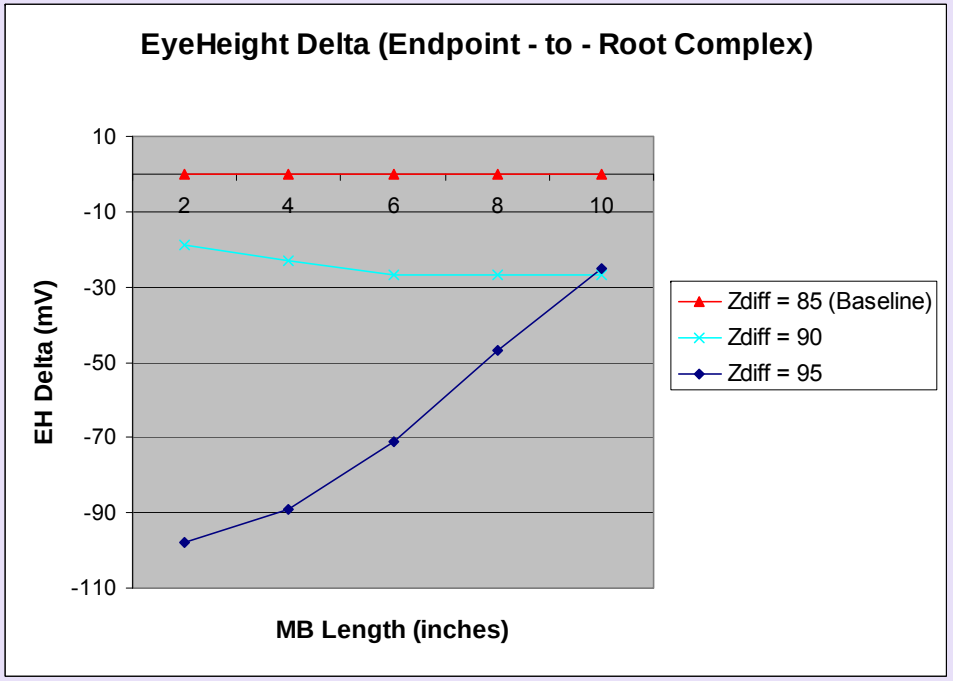
Example Root Complex: CPU/Chipset

Example Endpoint: Discrete GFX device

Impact on Eye Height

- Matching 85Ω differential impedance for the motherboard and packages consistently provides higher eye height margins
- Charts below show the delta in margins with 85Ω as the baseline:





Impact on Eye Width

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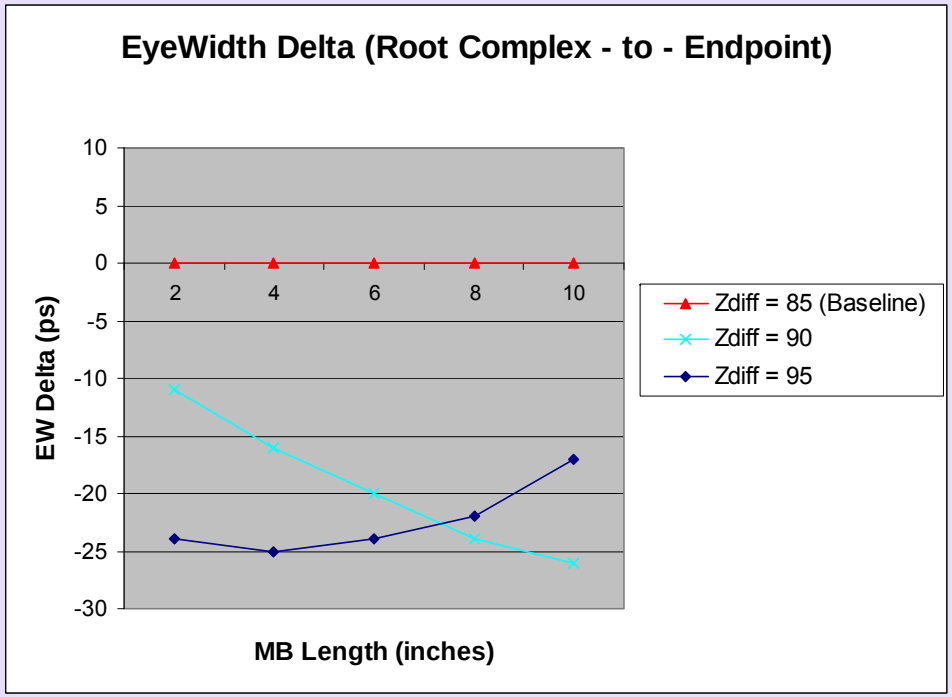
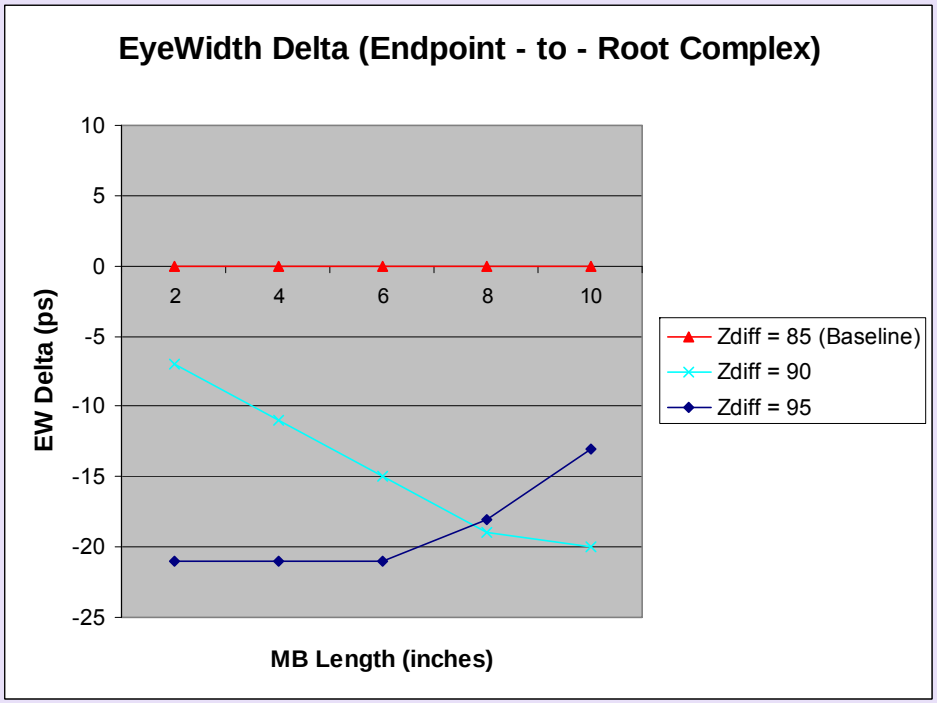
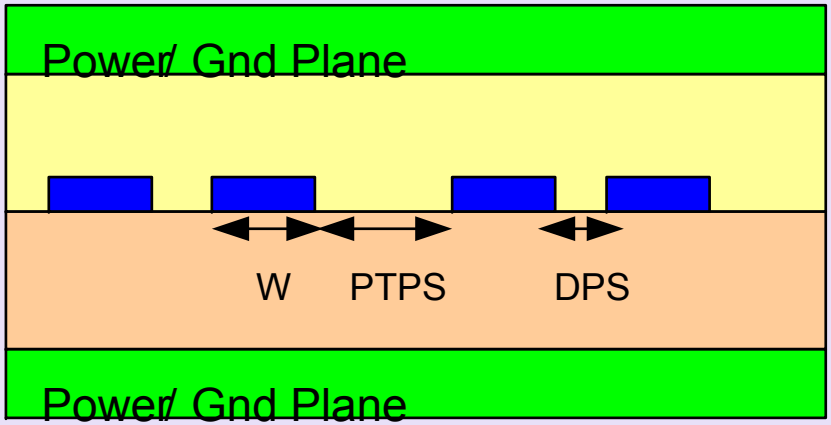




Impact on routability



- W: Trace width
- PTPS: Pair to pair spacing
- DPS: Differential pair spacing

- Lowering the differential impedance on motherboard from 100 Ω to 85 Ω reduces the PTPS by ~25% and DPS by ~45%
  - ✓ Saves real estate on board
  - ✓ Enables smaller form factor designs

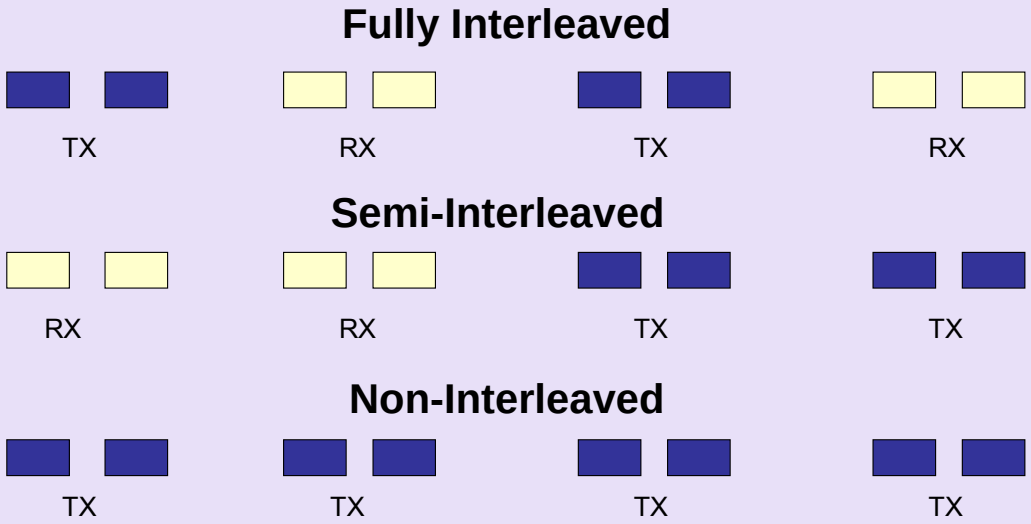
Summary

- 85Ω package + channel differential impedance provides optimal eye width and eye height
- 85 Ω also allows for tighter differential pair spacing which is better for routability on both the package and motherboard
- As power is a concern on mobile platforms, assuming 85 Ω channel with100 Ω terminations helps maintain same power levels as that with a 100 Ω channel
  - ✓ Did not analyze 80 Ω on the motherboard due to difficulty in achieving this low impedance with mobile motherboard assumptions

Rx / Tx Routing Optimization

Rx / Tx Routing Optimization

- Designers should carefully consider their Rx / Tx routing configurations when doing layout



- Crosstalk from interleaved routing has a significant impact on signal integrity
- In a mobile platform, where multiple layers are available, motherboard routing should be non-interleaved
- Crosstalk from the package routing is also significant and its impact should be considered. The following experiments show that impact.

Rx / Tx Routing Optimization

- Analyzed various Rx / Tx routing configurations on the package and compared the impact on eye height / width and cross-talk levels for the channel operating at 5GT/s

	Root Complex Pkg	Motherboard	Endpoint Pkg
Case 1- NNN	Non-interleaved	Non-interleaved	Non-interleaved
Case 2- INI	Interleaved	Non-interleaved	Interleaved
Case 3- SNS	Semi-interleaved	Non-interleaved	Semi-interleaved
Case 4- INS	Interleaved	Non-interleaved	Semi-interleaved
Case 5- NNI	Non-interleaved	Non-interleaved	Interleaved

Case Study Topology

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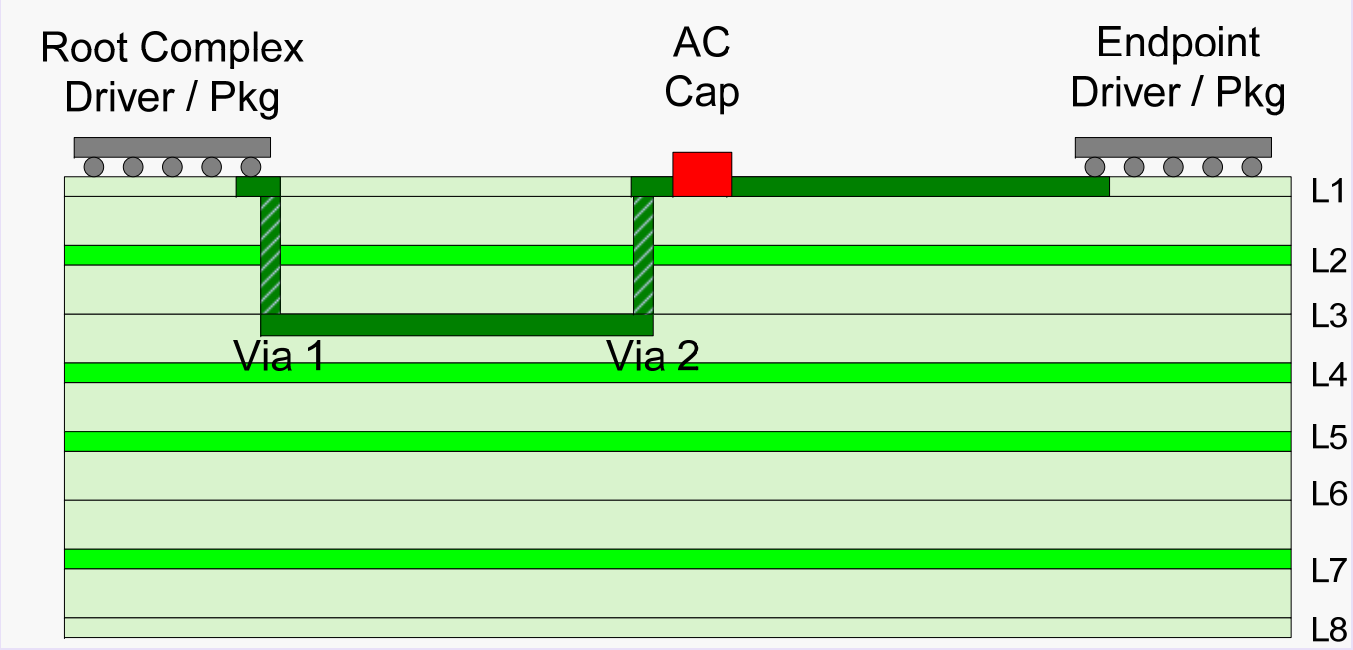
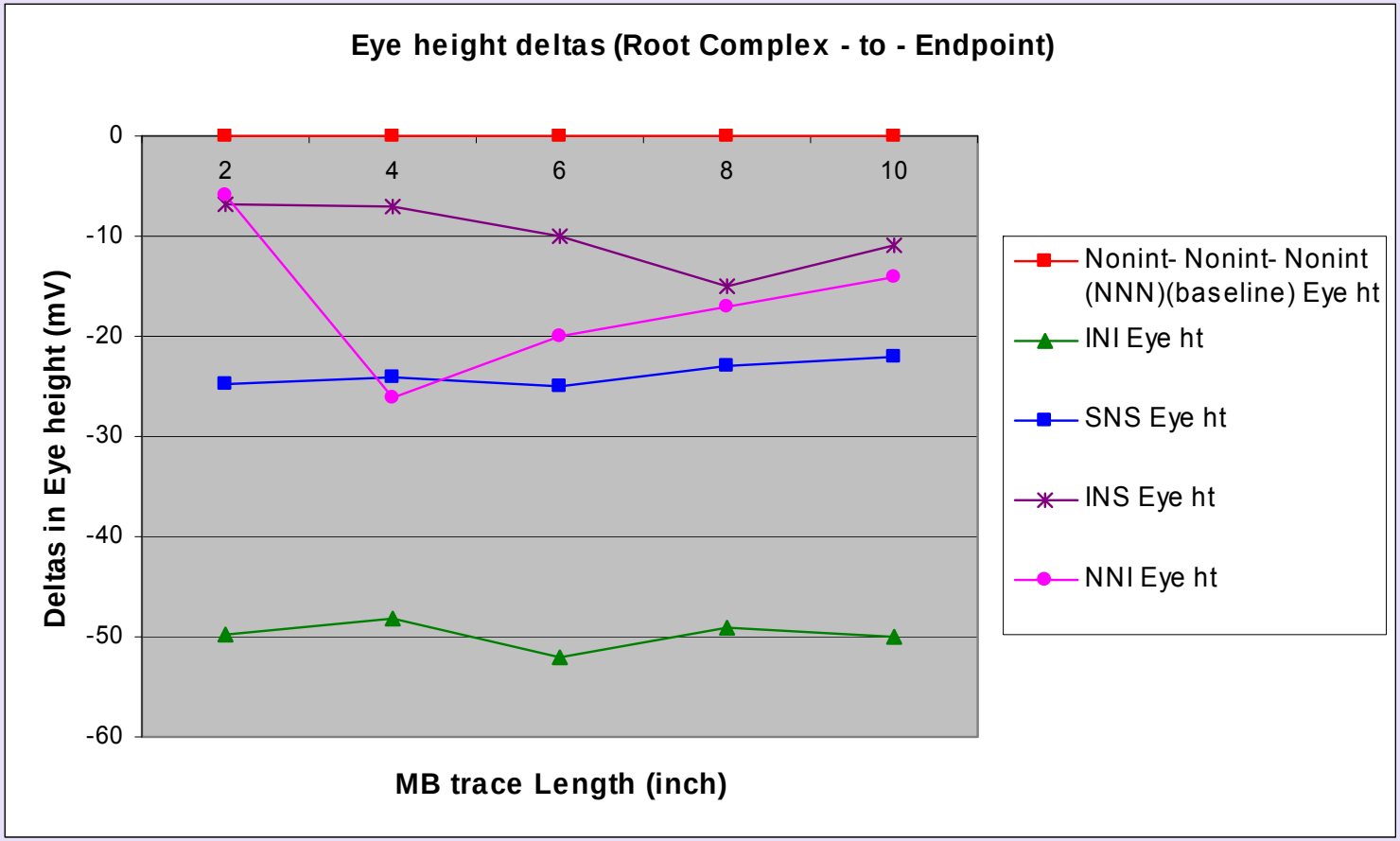


Example Root Complex: CPU/Chipset

Example Endpoint: Discrete GFX device

Impact on Eye Height

- Root Complex driving: Interleave - Non interleave (Motherboard)- Interleave (end point pkg) results in the least eye height
- Non interleave - Non interleave (MB)- Non Interleave (end point pkg) results in the most eye height



Impact on Eye Width

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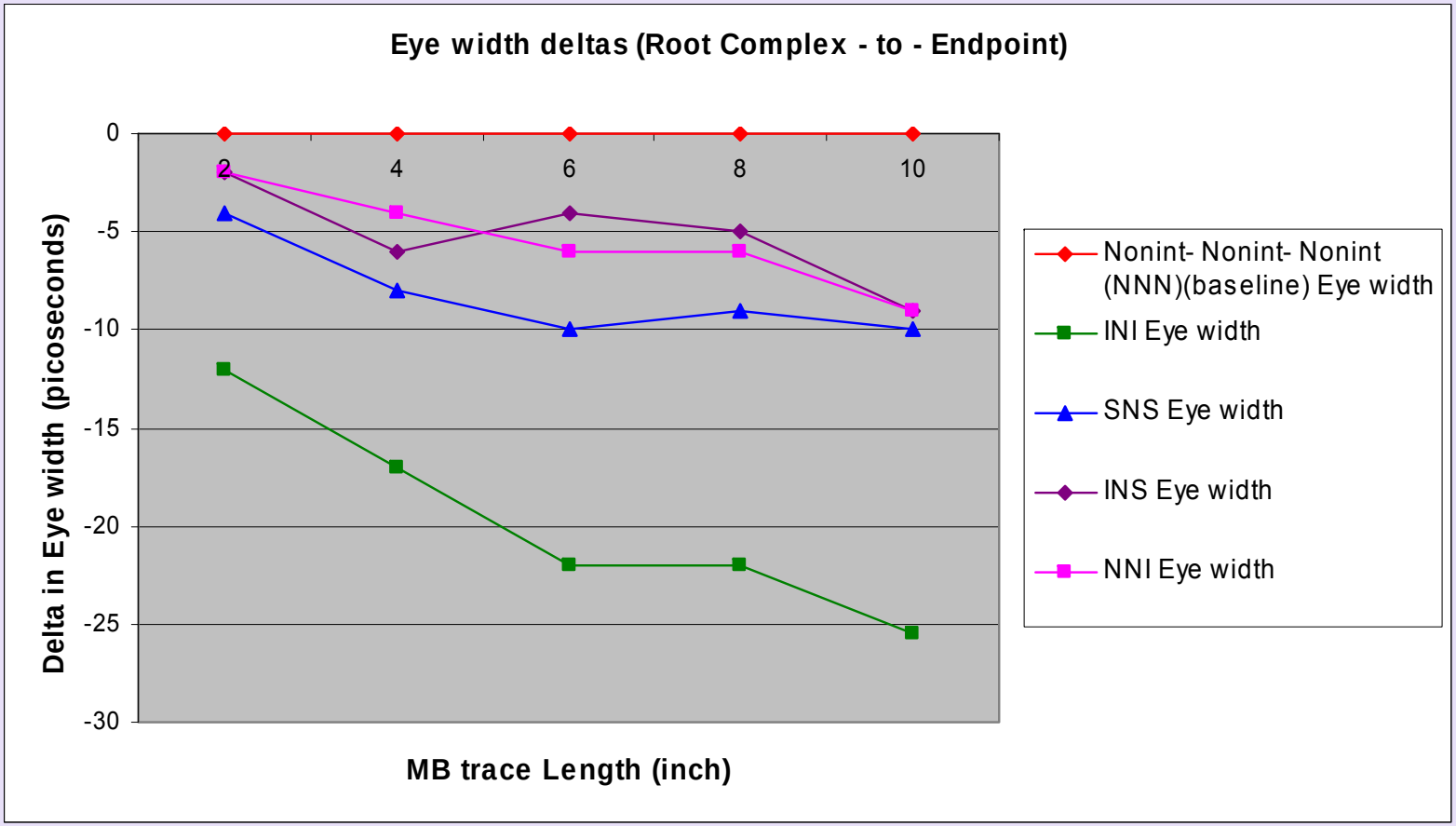
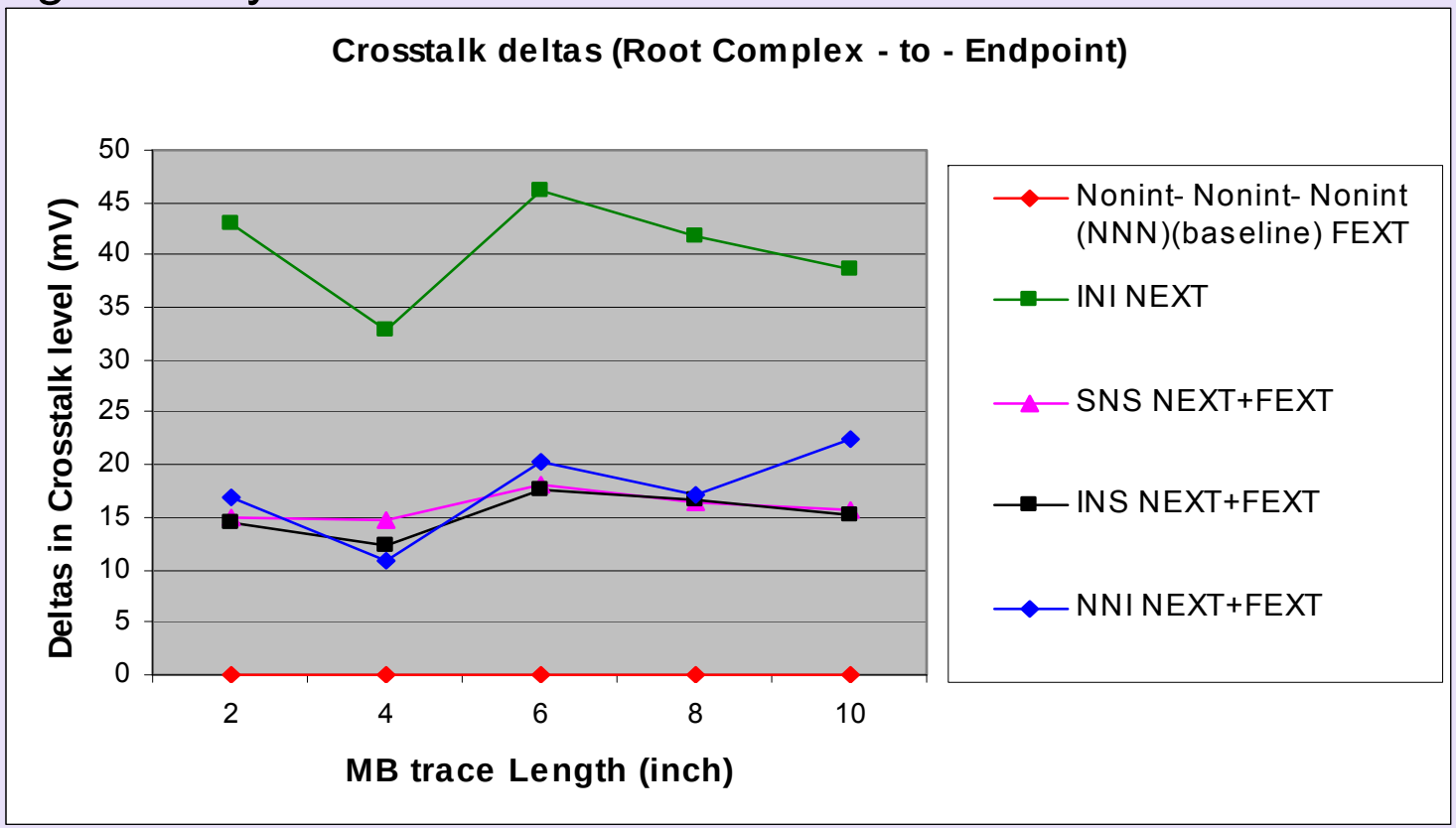
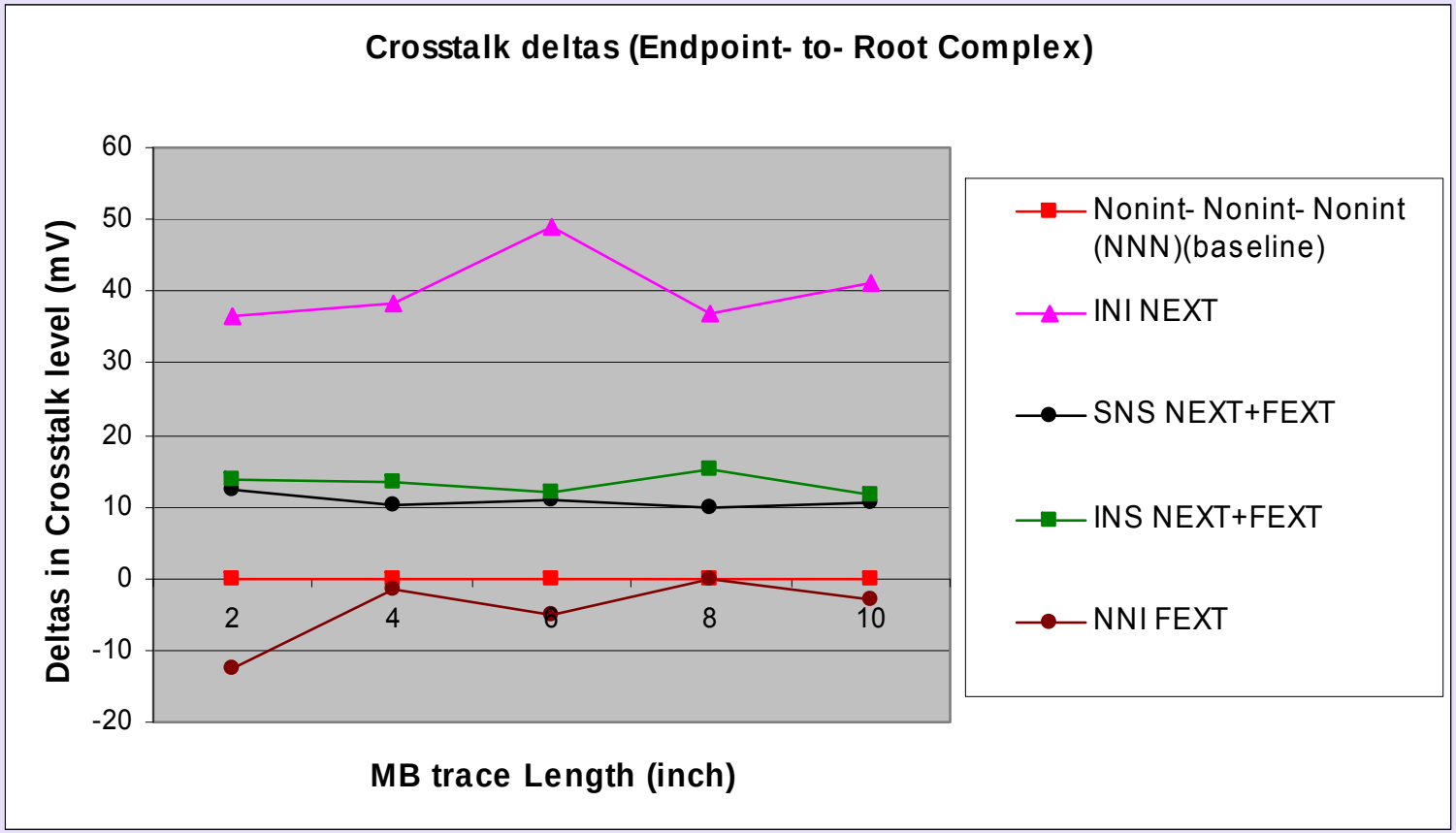


Crosstalk Results – Root Complex driving

- Interleaving on both packages (I-N-I configuration) results in maximum crosstalk- dominated by near end crosstalk (NEXT)
- Implementing all non-interleaved routing can reduce the crosstalk significantly



Crosstalk Results – End Point Driving



- Impact on crosstalk due to interleaving on both packages is quite significant

Summary for package routing combinations

- Non-interleaving on both packages produces the best results
- Interleaving on both packages is not advisable due to increased NEXT
- Interleaving or semi-interleaving on one of the packages (root complex or end point) does not have a large negative impact
- Non-interleaved routing is a good option due to availability of multiple routing layers in mobile layouts

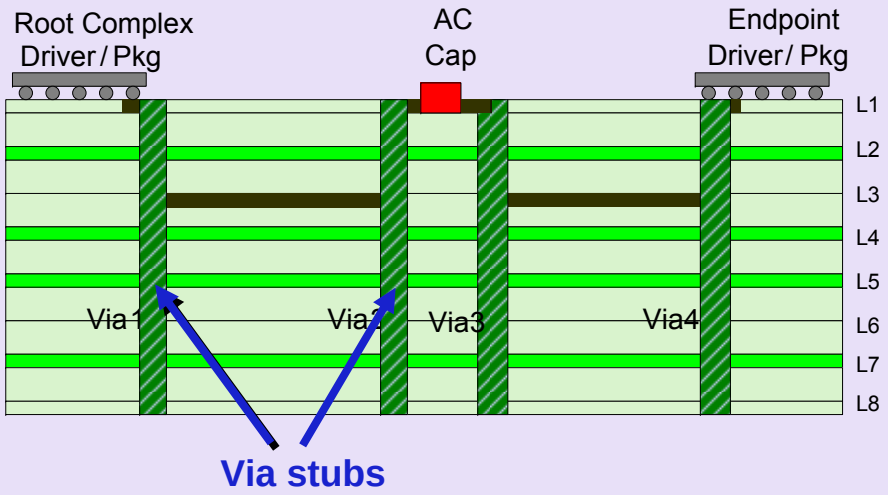
Layer Transition Optimizations

Layer Transition Optimization

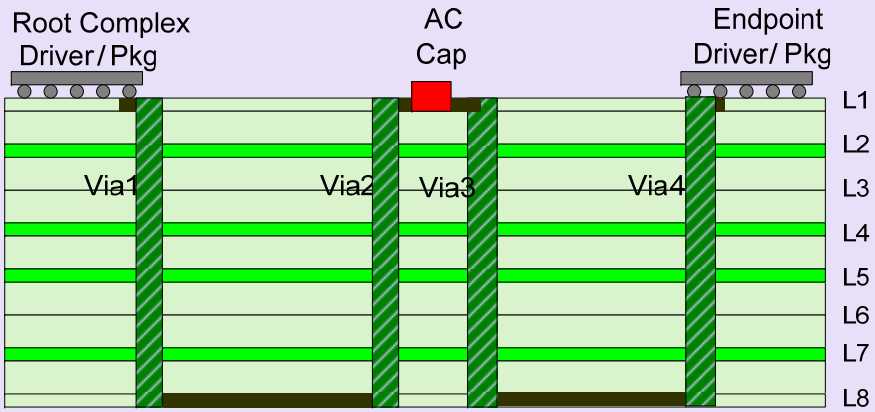
- On a mobile platform, designers should carefully consider the routing layers they select for high speed signals such as PCI Express 2.0
- Via stub affects can have a significant impact on eye height and eye width
- The case study example run at 5GT/s looks at an 8-layer motherboard with all routing on:
  - ✓ Layer 1
  - ✓ Layer 3
  - ✓ Layer 6
  - ✓ Layer 8
- The study looks at 10” motherboard routing
  - ✓ Also looked at 2” motherboard case and saw similar results

Case Study Topology

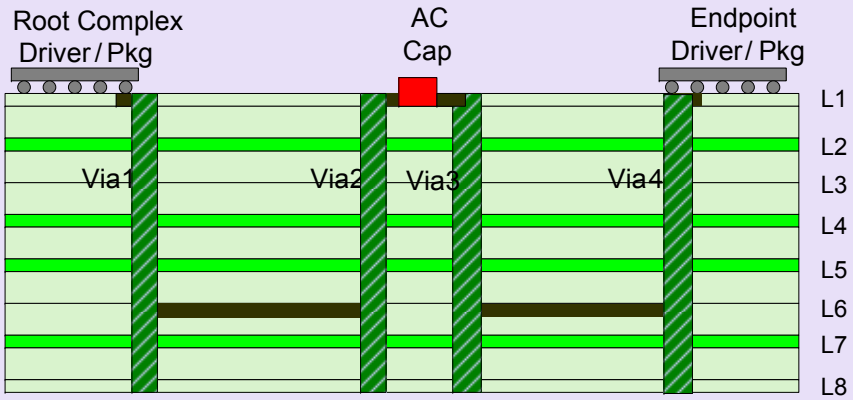
Layer 3 Routing (1to3 Via)



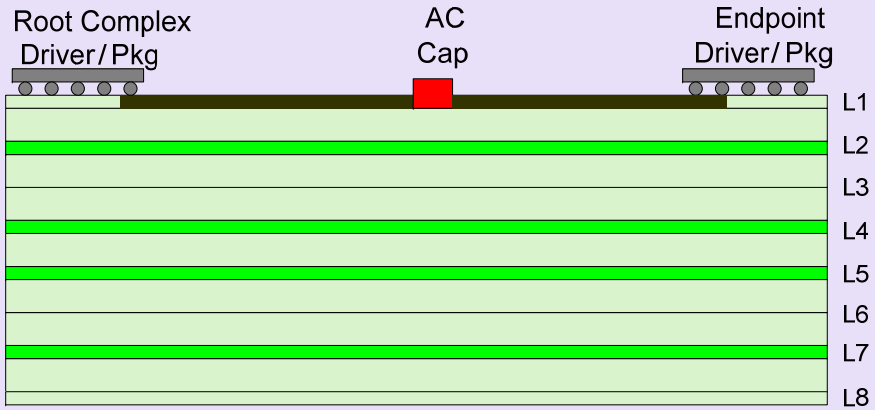
Layer 8 Routing (1to8 Via)



Layer 6 Routing (1to6 Via)



Layer 1 Routing (No Vias)



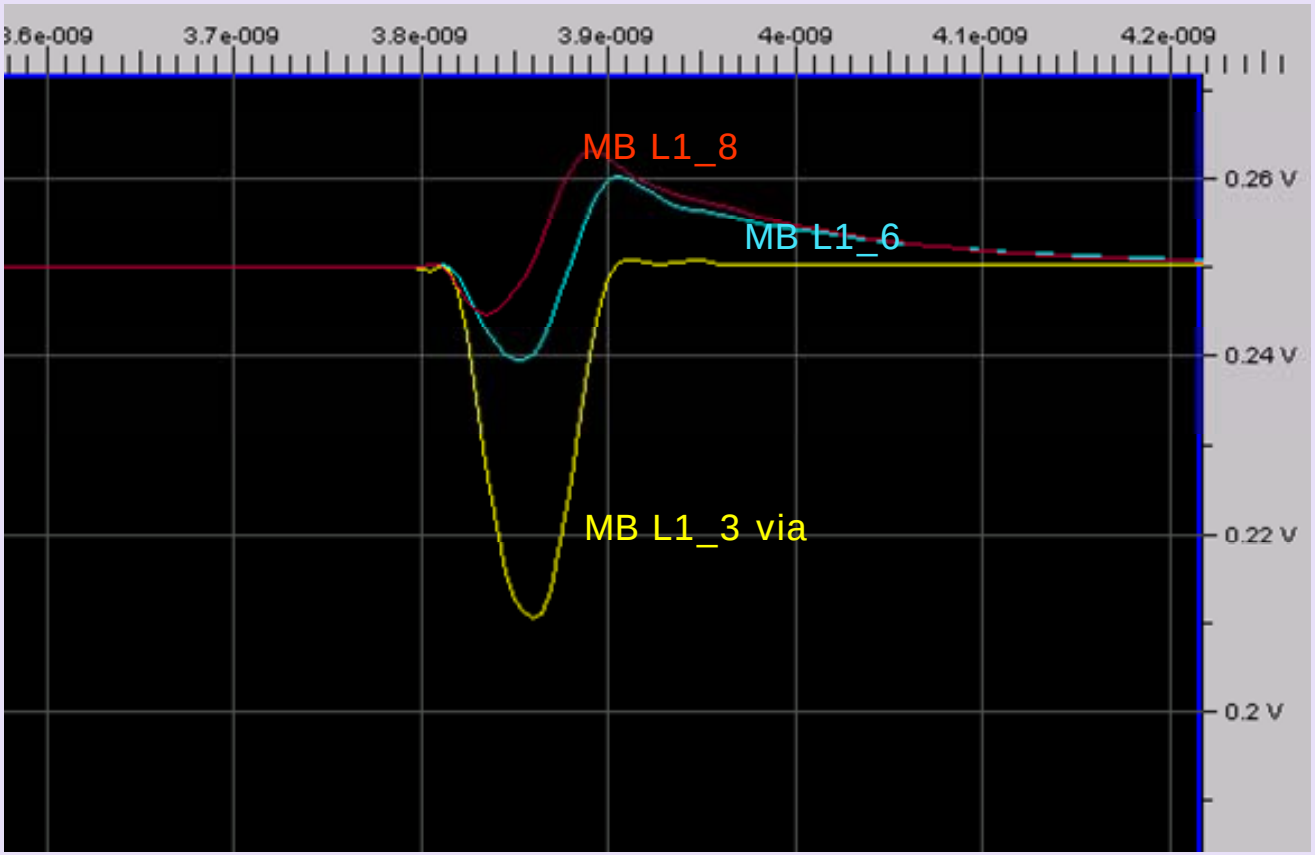
Impact on Eye Height and Width

- Transitioning from layer1 to layer3 results in worst case eye height
- For this case, the via stub has little impact on eye width margins
- If doing stripline routing, designers should consider using the far routing layer (Layer 6 in example). This reduces the resonance effects of the via stub
- Removing all vias improves eye height and eye width margins
  - ✓ However, microstrip routing can have other negative design impacts, such as EMI and limited routing space due to dense component placement on PCB top/bottom layers.

	All SL routing; 1to3 Vias	All SL routing; 1to6 Vias	All MS routing; 1to8 Vias	All MS routing; No vias
Eye Height (mV)	Baseline	+ 3	+ 17	+ 32
Eye Width (ps)	Baseline	+ 1	- 3	+ 6

Capacitive effect of 1to3 Via

- Looking at via model in the time domain into a test load, the capacitive affects of the Layer1-to-Layer3 via can be seen



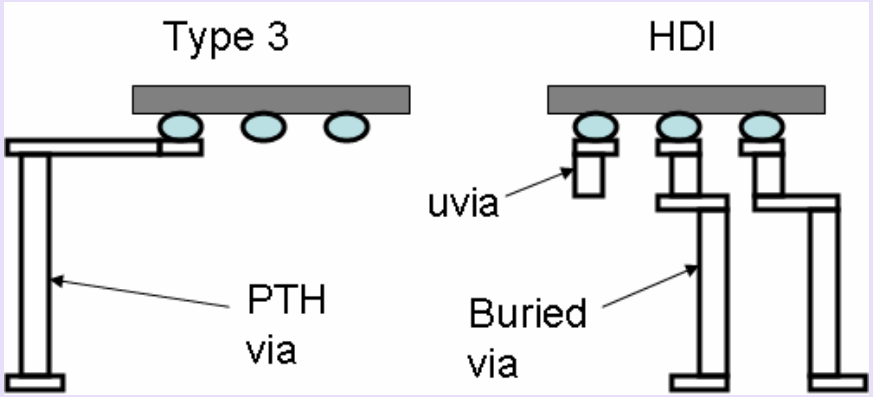
Impact of advanced stackup configurations implemented on mobile platforms

Mobile stackup implementations

- The ability to use multi-layer motherboards and the desire to implement small form factor designs drive mobile designs to use advanced stackup configurations, such as dual-stripline routing and high-density interconnect
- Both configurations assist in accomplishing tighter routing density but can also have a impact on signal quality, especially at high frequencies such at 5GT/s

Impact of High-density Interconnect

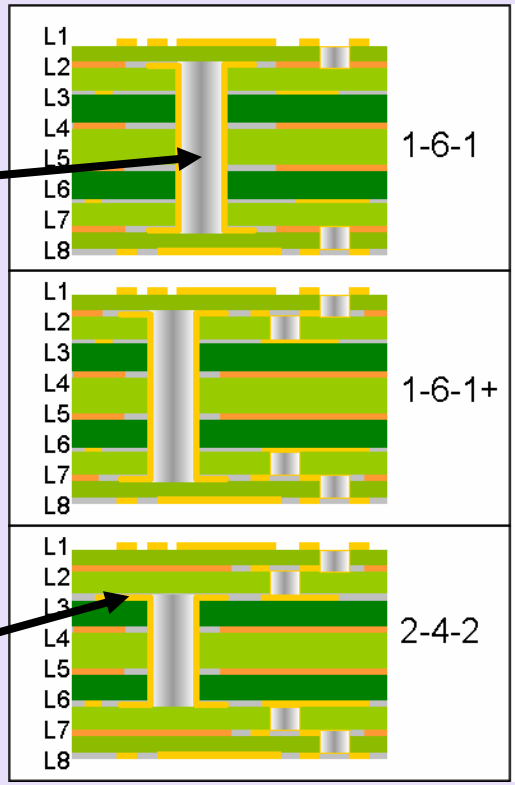
- Mainstream motherboards are defined as Type 3 PCB and are multilayer designs with no microvias or buried vias
- High-density interconnect (HDI) is a multilayer board manufactured with one or more build up layers that allow for the creation of microvias and buried vias



Impact of High-density Interconnect

- This study looked at 3 types of HDI configurations: 1-x-1, 1-x-1+, and 2-x-2, where “x” represents a variable number of core layers

Buried vias in 1-x-1 designs have via stubs similar to PTH vias



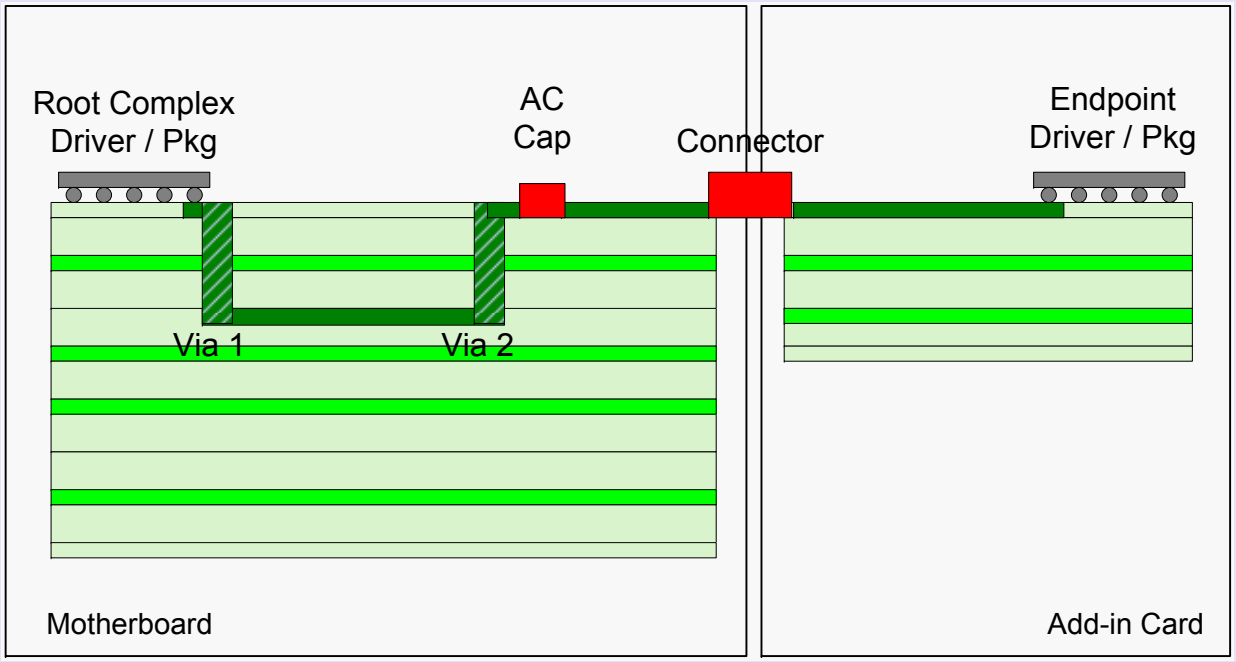
In 2-x-2 designs, L3 is a plated layer which causes larger xtalk but better differential coupling

Metal Layer	Type 3 (mils)	1-6-1 / 1-6-1+ (mils)	2-4-2 (mils)
	0.65	0.65	0.65
L1	1.9	1.9	1.9
	2.7	2.5	2.5
L2	1.2	1.9	1.9
	4	3	3
L3	0.6	0.6	1.2
	5	5	7
L4	1.2	1.2	1.2
	4	3	3
L5	1.2	1.2	1.2
	5	5	7
L6	0.6	0.6	1.2
	4	3	3
L7	1.2	1.9	1.9
	2.7	2.5	2.5
L8	1.9	1.9	1.9
	0.65	0.65	0.65

*** An 8-layer example was used in this study**

Case Study Topology

- Considered single routing topology with a combination of internal and external routing
- Simulated 1 – 6” on the motherboard and 2” on the add-in card
- Set the driver and receiver termination values to 100 Ohms differential while changing the package and channel impedance to 85ohms

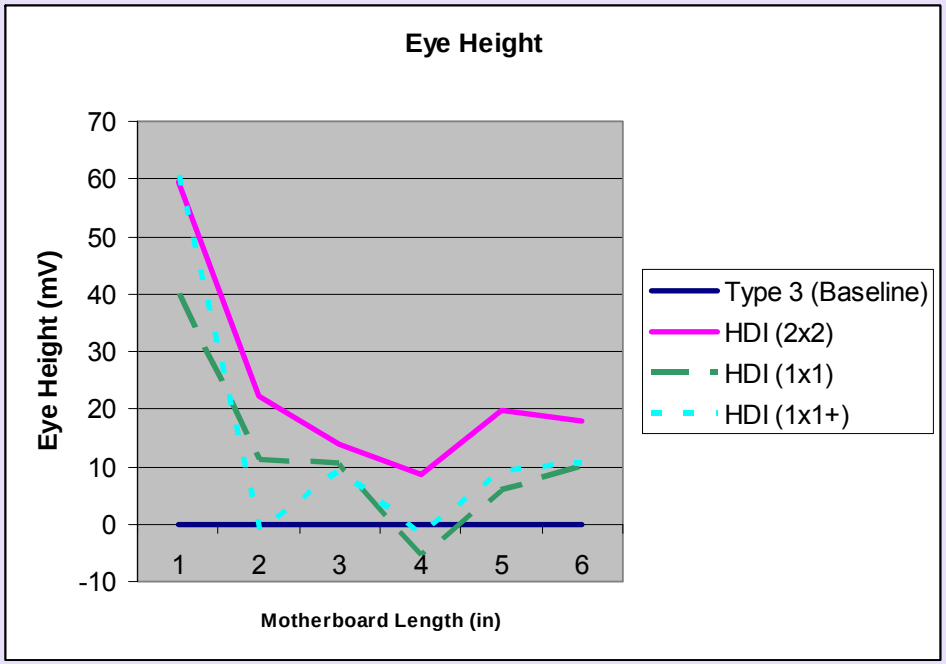


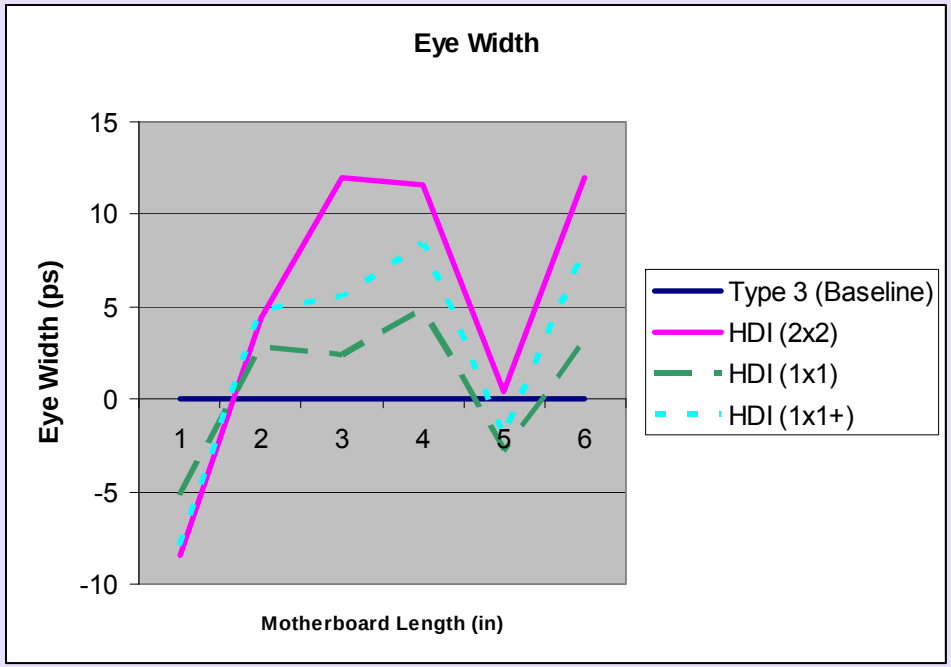
Example Root Complex: CPU/Chipset

Example Endpoint: Discrete GFX device

Impact of High-density Interconnect

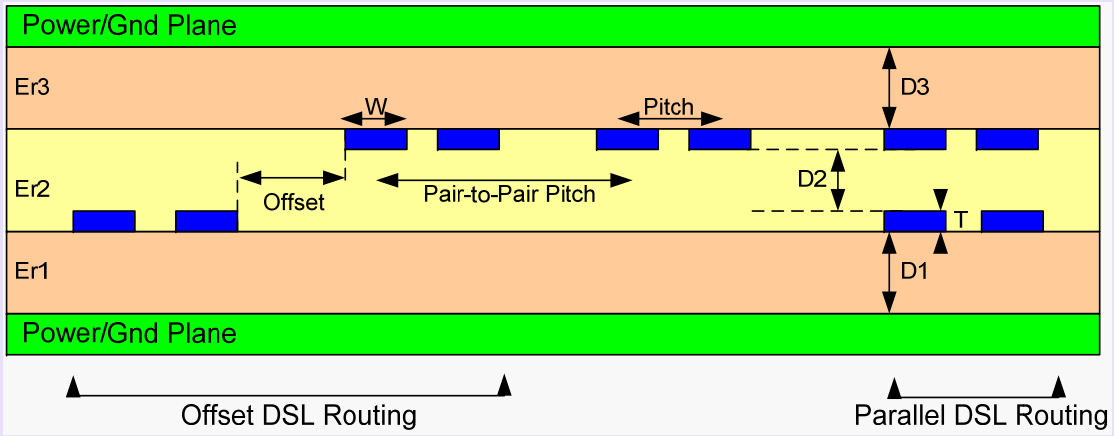
- For most routing lengths, HDI routing provides better eye height and eye width, largely due to smaller / no via stubs





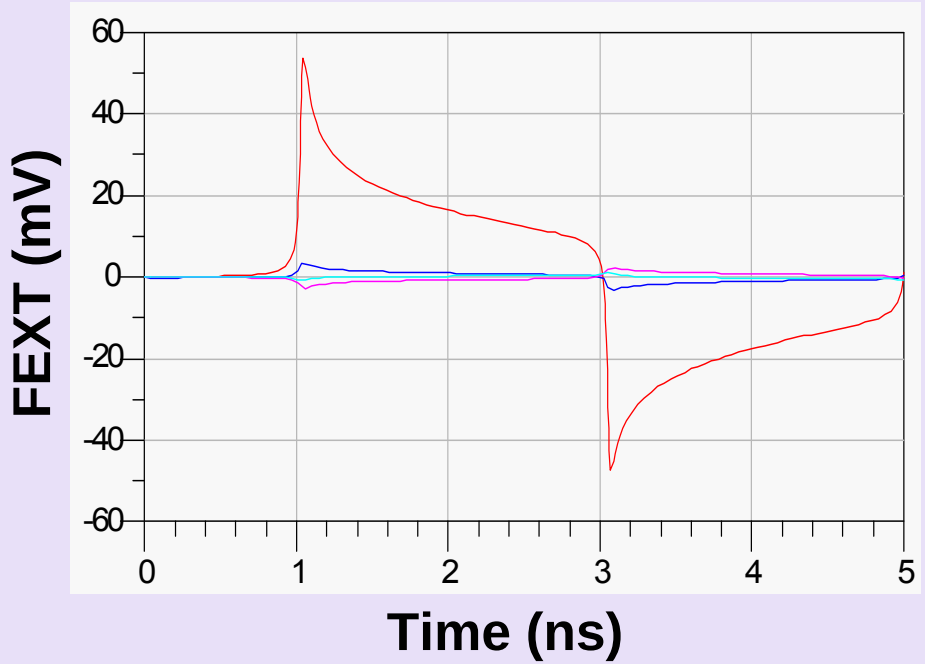
Dual-stripline Impact

- Dual-stripline (DSL) routing, where two signal layers are placed between between two plane layers, is used in mobile designs to reduce routing space and lower layer count
- There are several routing strategies for DSL configurations:
  - ✓ Parallel, Offset, and orthogonal routing
  - ✓ Large “D2” dielectric thickness vs small “D2” dielectric thickness



Impact of parallel DSL routing

- When the “D2” value in the DSL configuration is small, the crosstalk seen between the two signal layers is larger than the crosstalk between two differential pairs on the same layer
  - ✓ Experiment assumes 25ps rising and falling edges, 10inches of routing, and a 15mil pair-to-pair space



D2=5mils, Same layer neighbor

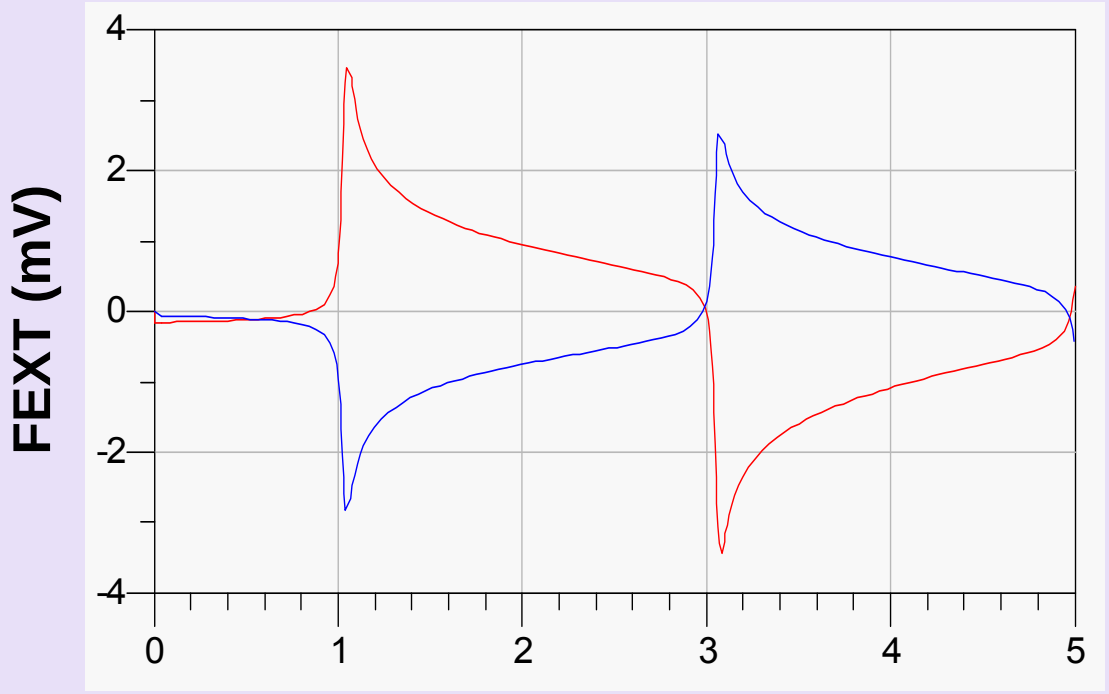
D2=15mils, Same layer neighbor

D2=15mils, Parallel on DSL layer

D2=5mils, Parallel on DSL layer

Impact of parallel DSL routing

- "D2" is 15mils and the pair-to-pair spacing is 15mils
- FEXT between DSL layers > FEXT between signals on same layer
- Due to broadside coupling

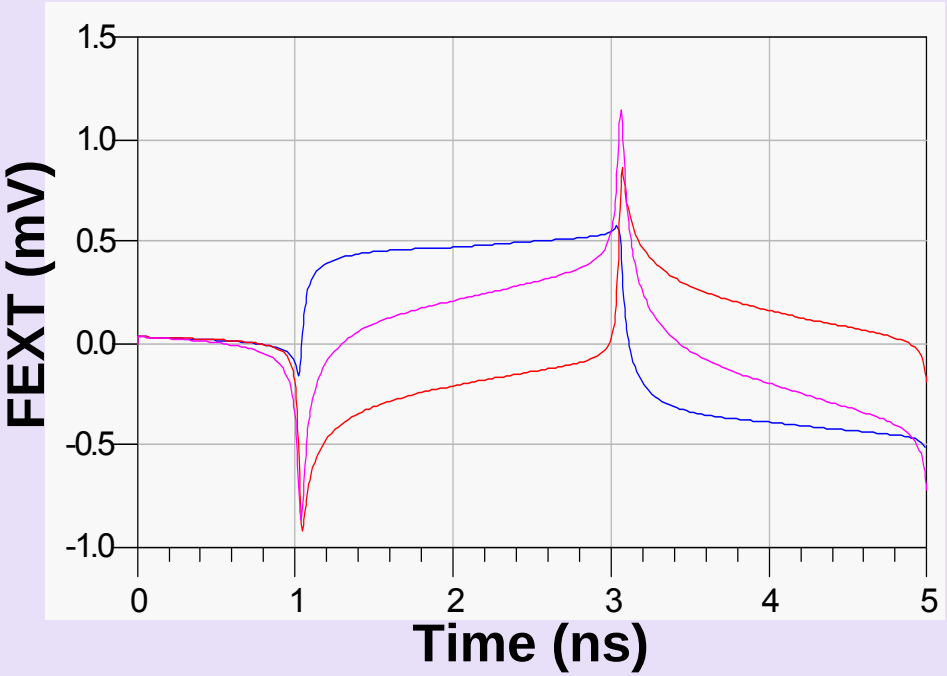


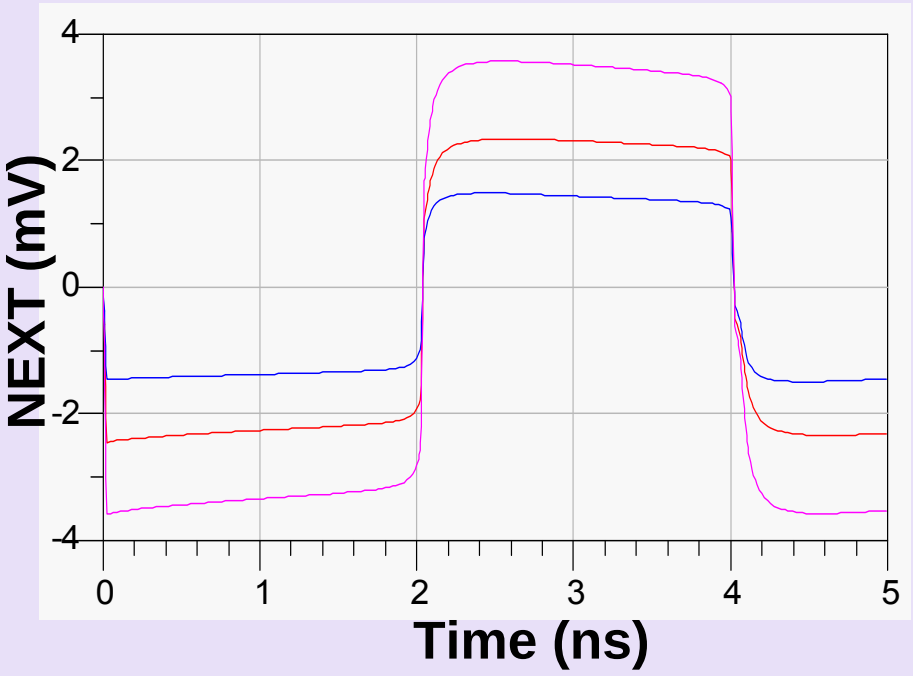
Pair-to-pair spacing =15 mils, Same layer FEXT

D2=15mils, DSL layer FEXT

Impact of offset DSL routing

- An offset = 15mils minimizes NEXT and FEXT seen on DSL layer





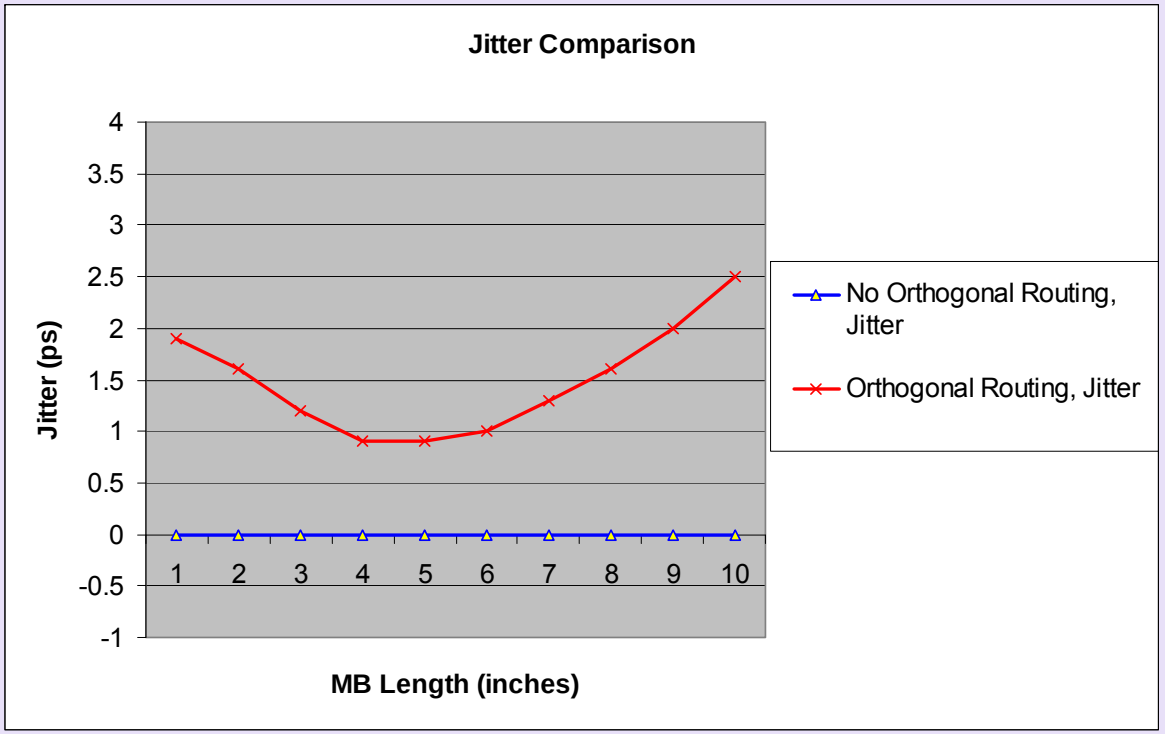
D2=15mils, Offset=15mils, DSL layer Xtalk

D2=5mils, Same layer neighbor Xtalk

D2=5mils, Offset=15mils, DSL layer Xtalk

Impact of orthogonal DSL routing

- Case study looked at topology shown on Slide 7
  - ✓ Added 14 single-ended DDR-like signals routed on a DSL layer above it
  - ✓ “D2”=5mils
- Little impact is seen to eye height or jitter



Overall Summary

- On a mobile platform, there are many optimizations that can be made to improve signal integrity and routability for PCI Express 2.0
  - ✓ Lower differential impedance on the package and motherboard to 85 Ohms
  - ✓ Use all non-interleaved routing
  - ✓ Consider reducing layer transitions; Using optimal layers for routing
  - ✓ Implement optimized or low-impact dual-stripline or HDI stackup configurations
- At higher data rates (5GT/s), these optimizations can no longer be considered insignificant and should be implemented where possible

Backup

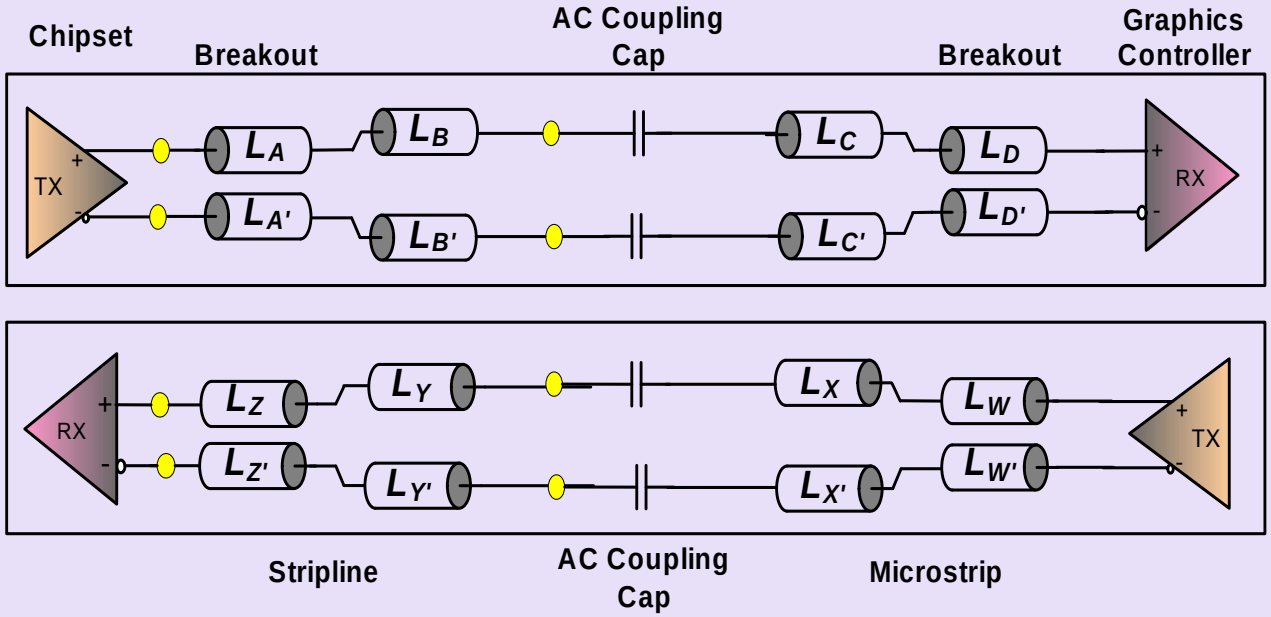
Simulation assumptions

- PCI Express 2.0 simulations were run with a nominal 85 ohm differential impedance for the root complex package, endpoint package, motherboard, and add-in card (AIC)
- Impedance variation: 85 +/- 15%
- Simulation tool: Hspice
- Simulation setup: 6line (or 3 differential pair) setup.
- Post-processing/analysis tool: Intel-internal tool that is based on Peak-distortion analysis (PDA) that reports eye height, eye width and crosstalk values. It determines the worst case bit-pattern for each topology
- Input to the topology: Pulse pattern
- Rise time of the pulse: ~50ps
- Trace geometries on PCB and add-in-card: (in mils) in below table

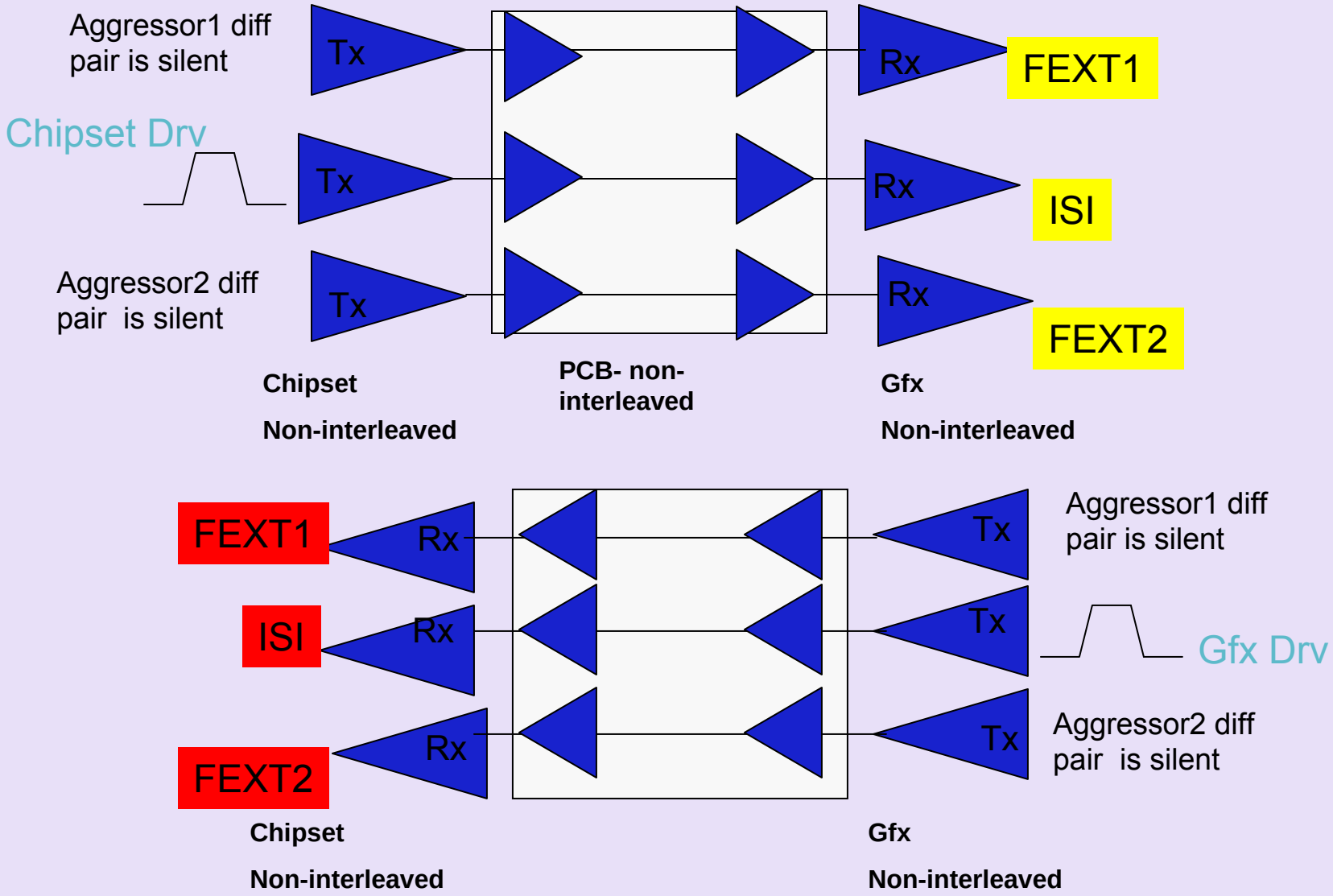
	Trace Width	Differential Pair Spacing	Zdiff	Pair-to-Pair Spacing	
Stripline	3.5	4	N/A	6	Breakout
	4	4	85	15	Main route
Microstrip	3.5	4	N/A	6	Breakout
	4	4	85	15	Main route

- AIC: Only Microstrip routing is assumed. Max length assumed on AIC: 2”
- Max length assumption on PCB: 10” for device down and 6” for AIC topology

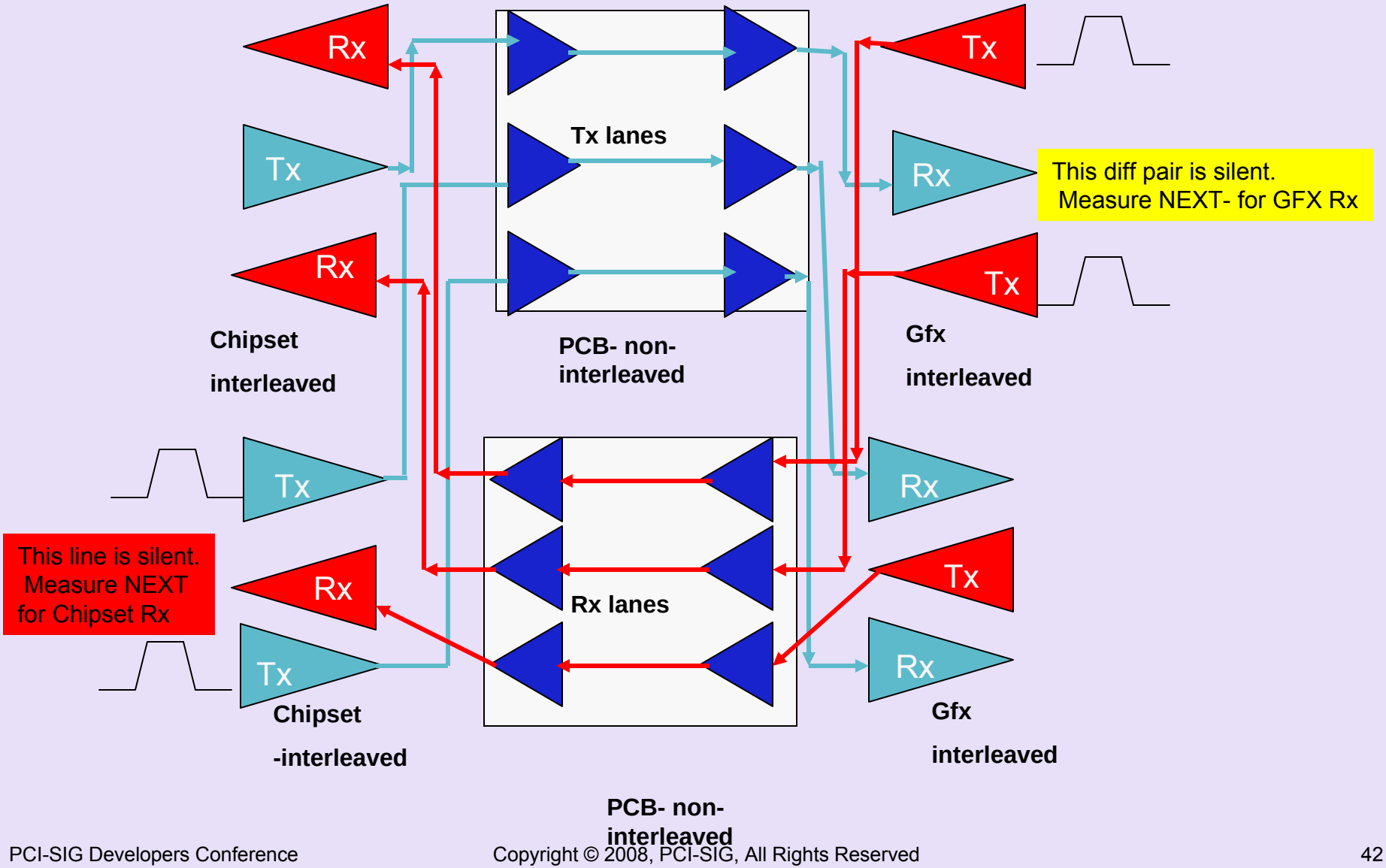
Topology simulated - device down



NNN configuration: (Non-interleaved on driver pkg- non-interleaved on motherboard and non-interleaved on gfx pkg)
Far End Cross Talk (FEXT) is measured
3 differential pair setup for chipset drv and 3 diff pair setup for GFX drv



INI configuration: (interleaved on driver pkg- non-interleaved on motherboard and interleaved on gfx pkg) Near End Cross Talk (NEXT) is measured



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