PCIe® 3.0 Physical Updates

Bent Hessen-Schmidt

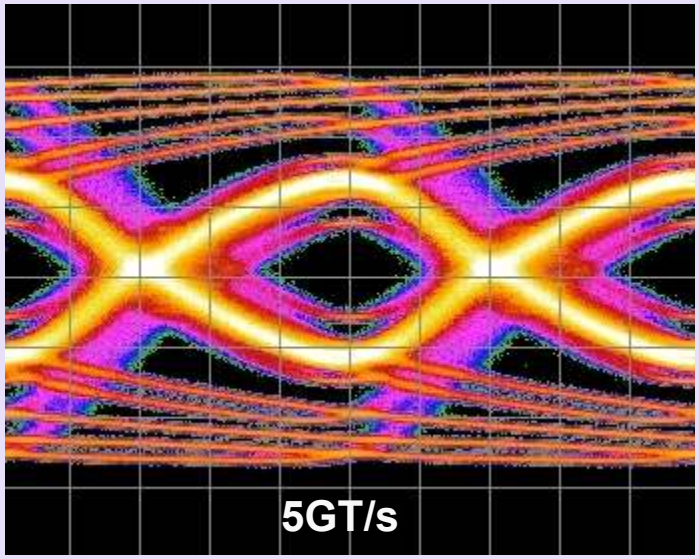
PCI Express EWG member

SyntheSys Research, Inc.

Disclaimer

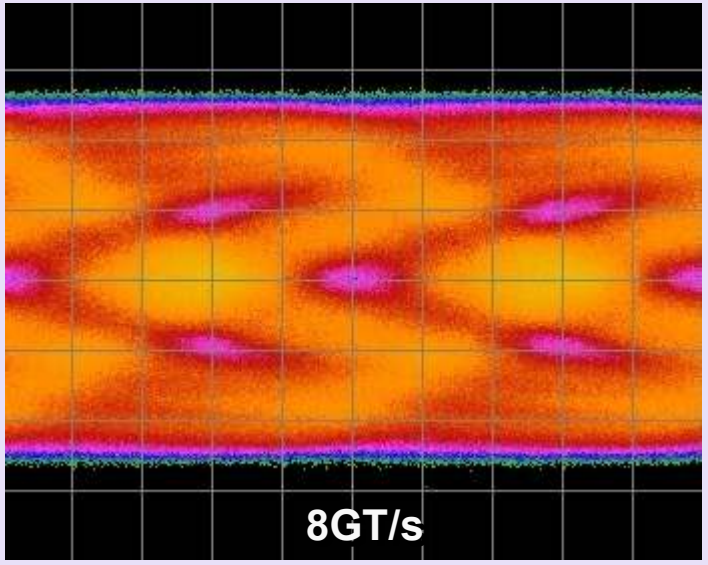
- NOTE: The information in this presentation refers to a specification still in the development process. This presentation reflects the current thinking of the workgroup, but all material is subject to change before the specification is released.

Challenge



200.0 ps

Reference Clock Jitter	44.2ps
-2500 ppm Offset	0.5ps
Residual of Spread Spectrum Clock	75.0ps
Total to share between Tx, Channel and Rx	80.3ps



125.0 ps

Reference Clock Jitter	14.2ps
-2500 ppm Offset	0.5ps
Residual of Spread Spectrum Clock	75.0ps
Total to share between Tx, Channel and Rx	35.3ps

Agenda

- Some key findings and enablers for 8 GT/s
  - ✓ PCIe® 3.0 Requirements
  - ✓ CDR analysis
  - ✓ Tx and Rx PLL bandwidths
  - ✓ Reference Clock filtering
  - ✓ Transmitter measurement de-embedding
  - ✓ Baseline wander from PRBS scrambling of data
  - ✓ Inter lane PRBS offsets
  - ✓ Channel Validation
  - ✓ Receiver jitter tolerance testing

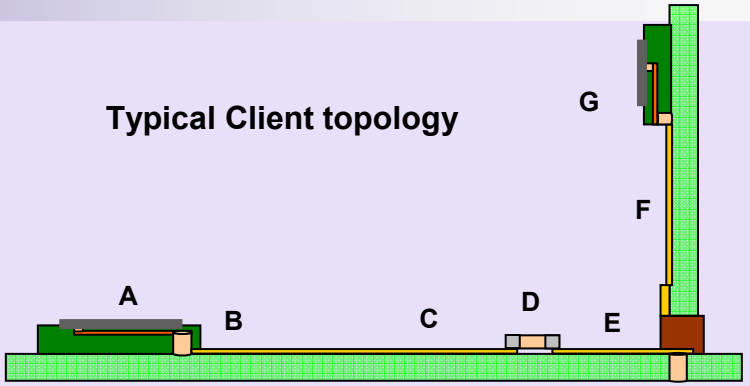
PCIe 3.0 Requirements

- 2x the data payload bandwidth of PCIe 2.0
- Full backwards interoperability with PCIe 1.x, PCIe 2.0
- Same cost structure for high volume platforms
- Same or better mW/GB/s power budget as PCIe 2.0
- Same channel reach as for PCIe 2.0
  - ✓ Mobile: 8 inches, one connector
  - ✓ Client: 14 inches, one connector
  - ✓ Server: 20 inches, two connectors
- Re-use of Reference Clock components
  - ✓ Jitter performance need not be improved

Channel

- Client
  - ✓ Motherboard and adapter
  - ✓ One PCIe connector
  - ✓ No vias other than connector
  - ✓ Routed as microstrip
  - ✓ Two channels analyzed: 14” and 7”
- Server
  - ✓ Motherboard, riser card, and adapter
  - ✓ Two connectors
  - ✓ Several vias on motherboard
  - ✓ Routed primarily as stripline
  - ✓ Max channel length ~ 20”
- Channels analyzed to include corner cases
- Various statistical tools used by different PCI-SIG members to generate results
  - ✓ STATEYE, SIGSIM, others
  - ✓ All results corroborated

Typical Client topology

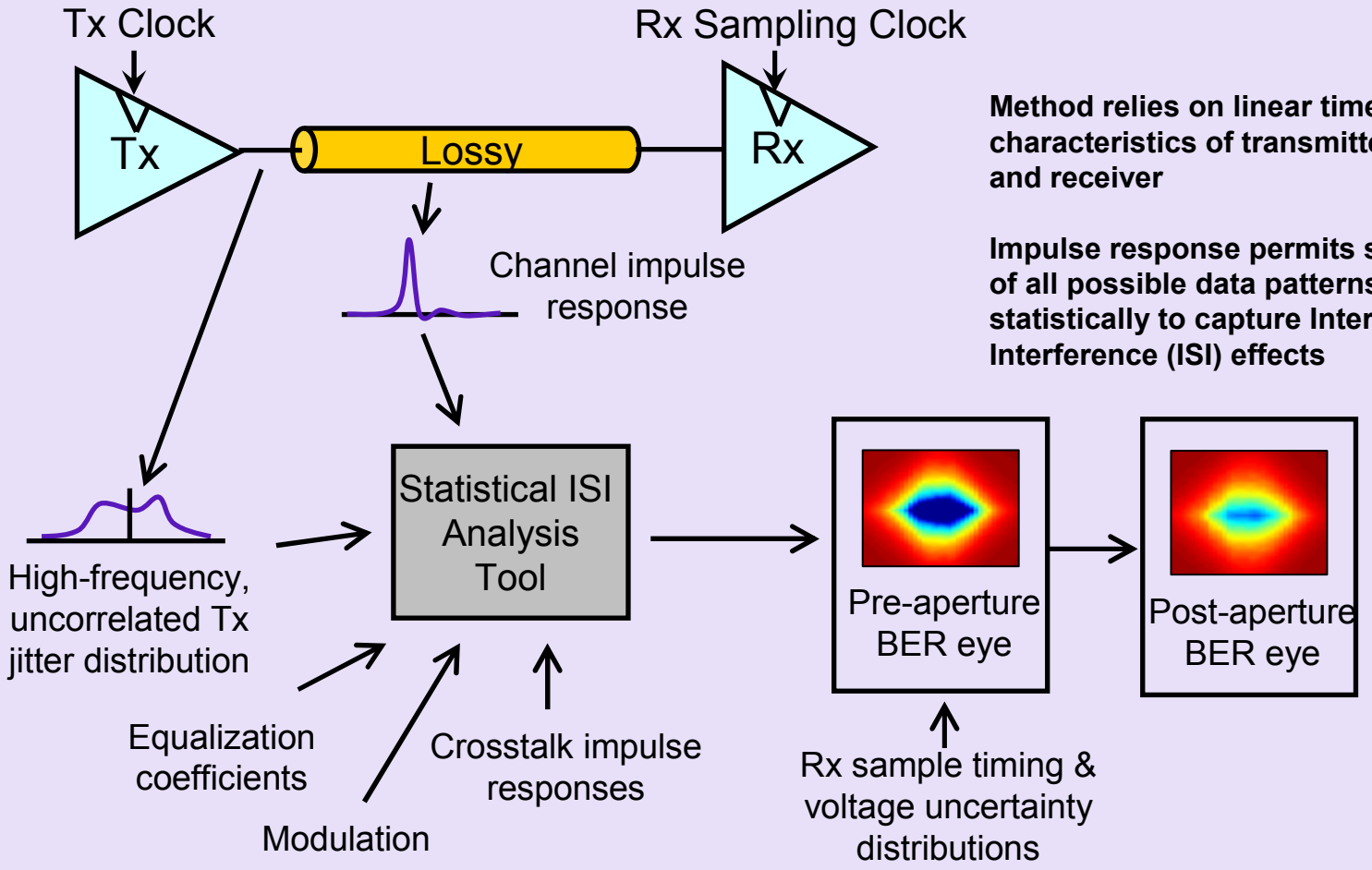


Seg	Description
A	Host package (transmitter)
B	Break Out
C	Mother board 7” transmission line
D	Mother board post capacitor
E	Add in card 3” transmission line
F	Add in card package break out
G	Add in card package (receiver)

Enabling Factors for 8 GT/s

- Transmitter (Tx) de-emphasis
  - ✓ Several presets to accommodate different classes of channels
  - ✓ One post cursor tap and (possibly) one pre cursor tap
- Receiver (Rx) equalization
  - ✓ 1st order linear equalizer is assumed as minimum receiver equalization
  - ✓ Specification does not stipulate what type of receiver equalization may be implemented
- Optimizations for Tx, Rx Phase Locked Loops (PLL) and Clock Data Recovery (CDR)
  - ✓ PLL bandwidth reduced, CDR jitter tracking increased
- Employ statistical methods in identifying solution space
  - ✓ Properly account for all Tx, Rx jitter components
  - ✓ Model interaction between scrambled data and channel

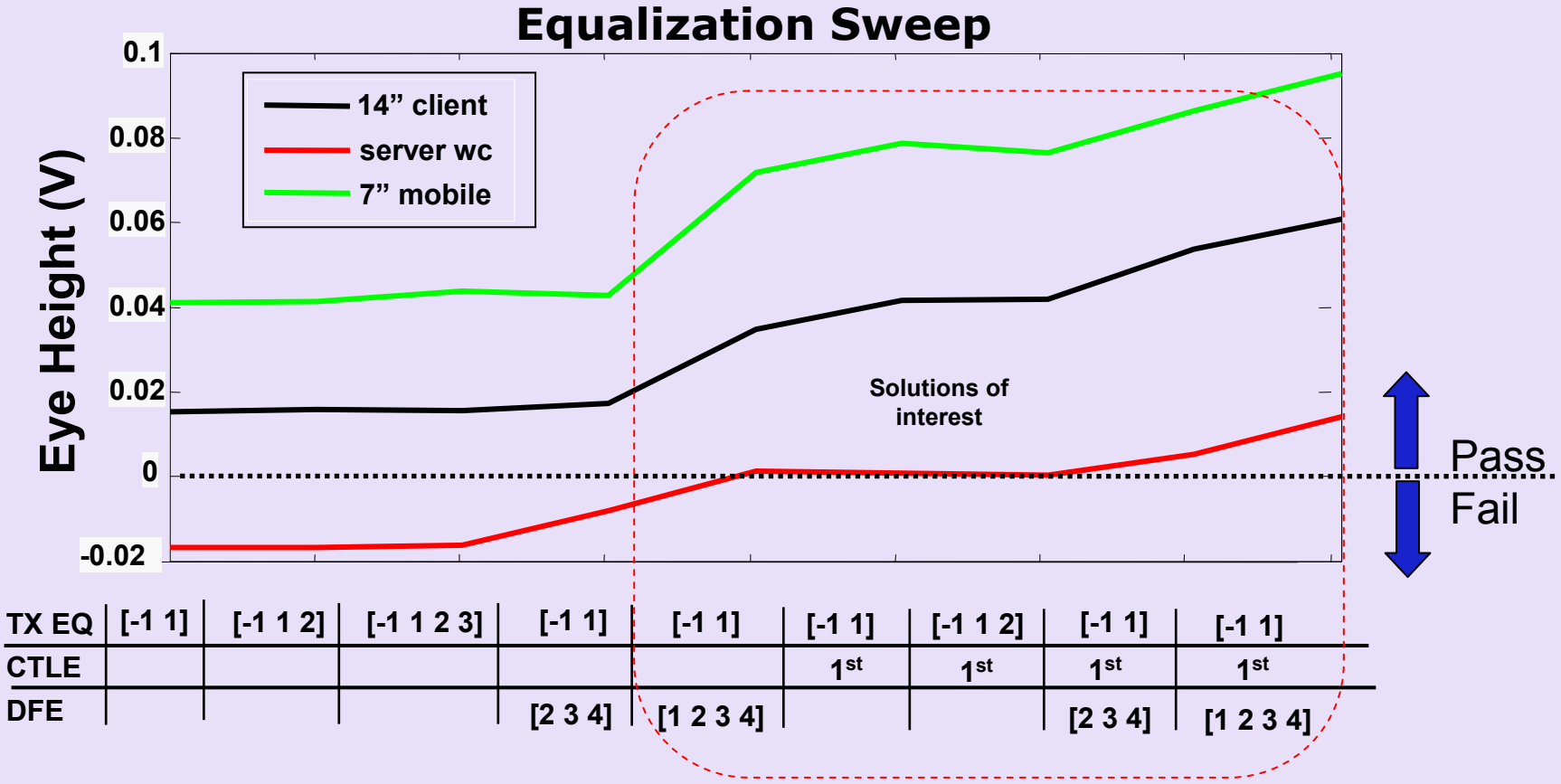
Statistical Signaling Methodology



Method relies on linear time invariant characteristics of transmitter, channel and receiver

Impulse response permits superposition of all possible data patterns weighted statistically to capture Inter Symbol Interference (ISI) effects

Margins versus Equalization Type



With the exception of a few worst case maximum length server channels, a combination of Tx de-emphasis and Rx linear equalization yields positive margins. Voltage/jitter margins may be increased by use of more complex Rx equalization techniques.

8 GT/s Timing budget

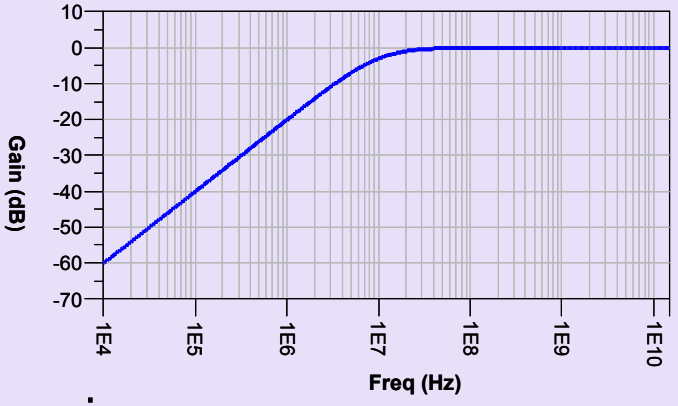
- A major goal is to make 8 GT/s evolutionary
  - ✓ Support existing usage models
  - ✓ Preserve Common Reference Clock and Data Clocked modes
  - ✓ Re-use of silicon PHY architectures
  - ✓ Re-use of 5 GT/s reference clock generators
- Common Reference Clock most challenging
  - ✓ At 5 GT/s Reference Clock jitter consumes significant portion of the timing budget (3.1ps RMS)
  - ✓ Tx and Rx Phase Locked Loop (PLL) bandwidth matching
  - ✓ Transport delay
- Low frequency transmitter jitter tolerance
  - ✓ Want to avoid requiring LC based PLLs

Clock Data Recovery (CDR) Bandwidth

- Key to solving these problems is to place burden on the Rx CDR
  - ✓ 2.5 GT/s and 5 GT/s have no specific CDR phase tracking requirements
  - ✓ 8 GT/s higher data rate allows CDR bandwidth to be increased
  - ✓ Despite non-linear behavior, CDR is conservatively approximated by a first order high pass filter (higher order CDRs are allowed and suggested)
- 8 GT/s Rx tolerance testing validates CDR tracking performance
  - ✓ Rx must tolerate 0.35 UI of additional sinusoidal eye closure at 1 MHz compared to minimum eye opening
- Expectation is that existing Rx CDR's can be modified to meet these requirements for 8 GT/s

Tx and Rx Multiplying PLL

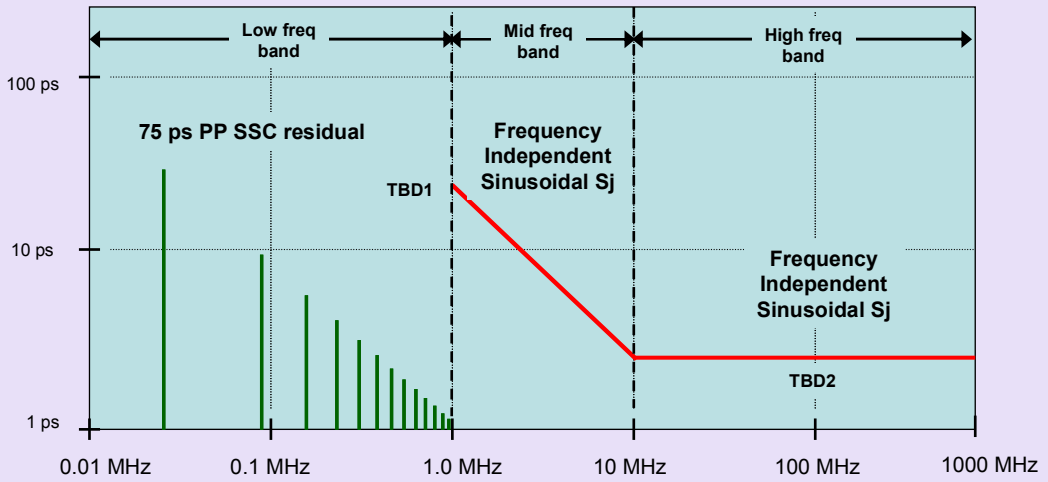
- Propose for 8 GT/s using a 5 MHz to 10 MHz Tx PLL bandwidth with 1dB peaking and 10 MHz Rx CDR (0.3 draft was 2 MHz to 4 MHz)
  - ✓ Provides overlap with 5 GT/s requirements
  - ✓ Increased bandwidth relaxes phase noise requirements on PLL VCO
  - ✓ Receiver tolerance testing ensures CDR will reject low frequency phase noise



- High bandwidth CDR makes up for reduced attenuation of LF jitter from higher PLL bandwidths
- Allows backward compatibility with 2.5 GT/s and 5 GT/s
  - ✓ Common PLL architecture can be used for 2.5 GT/s – 8 GT/s
  - ✓ Multiple PLLs only needed for devices that support splitting links

Receiver tolerance testing

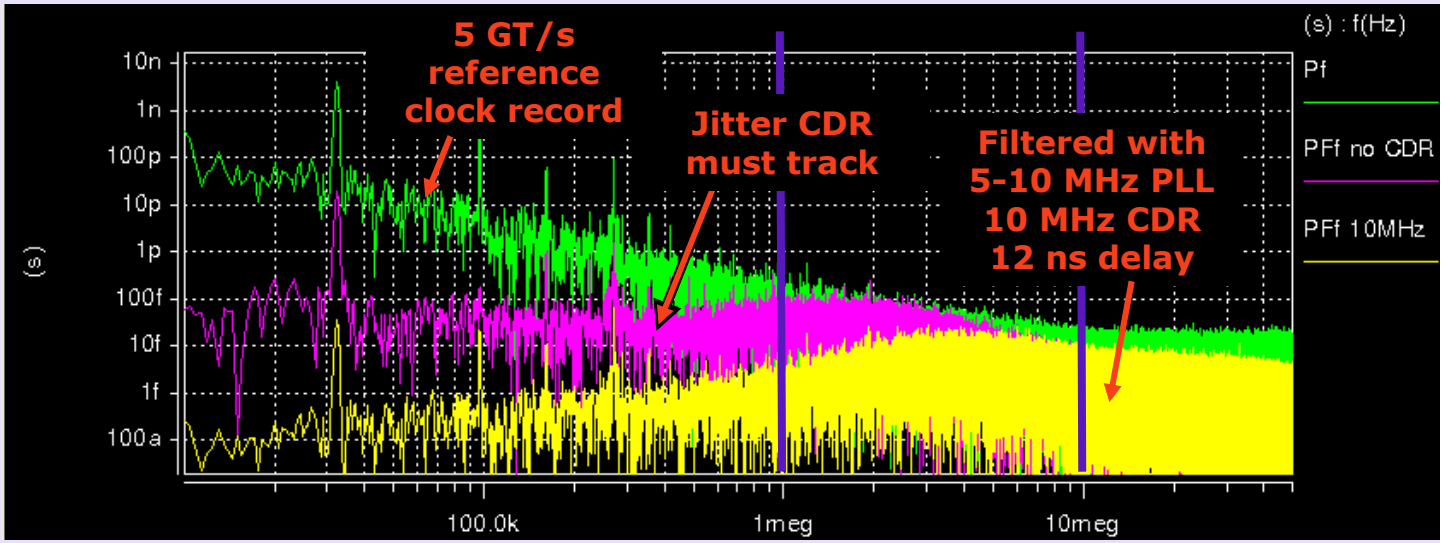
- To be able to rely on the receiver to follow a first or higher order high pass we need to test its response
- We can add a jitter tolerance test that phase modulates the data source and sweeps the frequency
  - ✓ Voltage waveform generated like PCIe 2.0 with a calibration channel to generate ISI
- At high frequency (>10 MHz) two sinusoids are calibrated to create a limit stressed eye as in PCIe 2.0
  - ✓ Use a variable and fixed frequency
  - ✓ 10 MHz ~0.04 UI pk-pk (5 ps) + 200 MHz ~0.2 UI
- Variable frequency sinusoid is then swept to a lower frequency increasing its amplitude from 10 MHz to 1 MHz at 20 dB per decade
  - ✓ 1 MHz ~0.4 UI pk-pk (50 ps) + 200 MHz ~0.2 UI

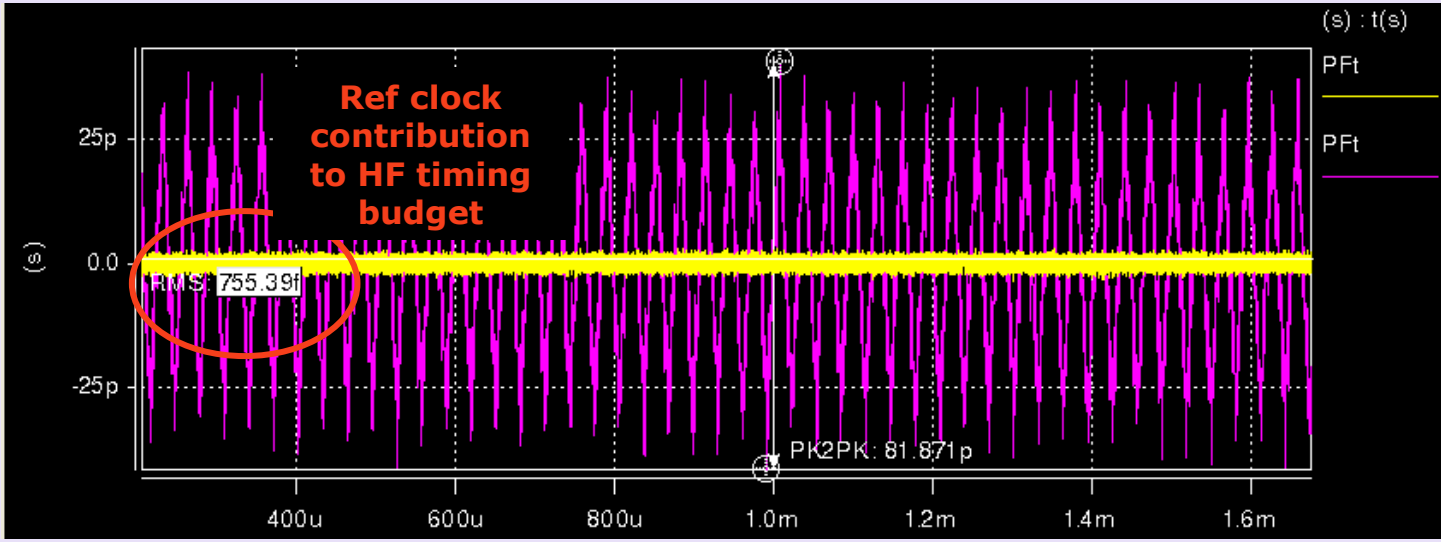


N.B. Only one Medium frequency spur applied at a time

Reference clock filtering

- Typical 100 MHz 5 GT/s reference clock
- Filtered with PLL difference function defined for 2.5 GT/s with:
  - ✓ 5-10 MHz PLL BW 1 dB peaking
  - ✓ 10 MHz high pass for CDR
  - ✓ 12 ns transport delay
- Will require an additional measurement of reference clock
  - ✓ Expect existing 5 GT/s ref clocks will pass



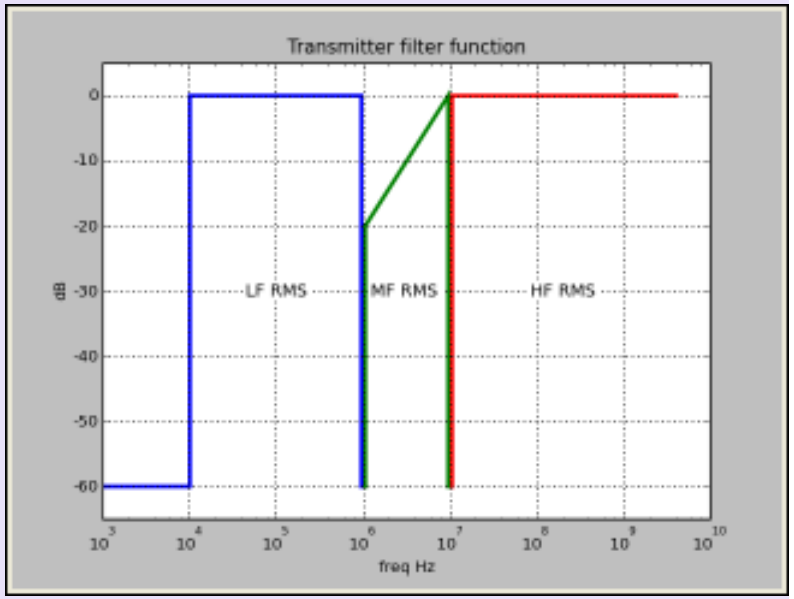


Transmitter measurement

- For 2.5 GT/s and 5 GT/s, the Tx was specified using the pin as the reference plane
  - ✓ Most convenient manufacturing boundary
  - ✓ Frequency domain return loss specification used to bound package interaction with channel
- At 8 GT/s, package/die-pad and package/channel interactions need to be comprehended
  - ✓ Return loss is much more significant
    - Interacts with channel discontinuities
    - Need a representative package model for channel compliance
  - ✓ Package high frequency loss makes Tx voltage and jitter measurements inaccurate
    - DUT 'pin' is physically the SMT pad of device and so not accessible
- Requires a methodology that separates package effects from silicon effects
  - ✓ Implies de-embedding to die-pad or fitting to a Tx-model

Transmitter phase jitter filtering

- Split into 3 bands
  - ✓ Low Frequency RMS (10 kHz to 1 MHz) similar 5 GT/s
  - ✓ Medium Frequency RMS (1 MHz to 10 MHz) filtered with 20 dB/dec high pass
  - ✓ High Frequency RMS (>10 MHz) similar to 5 GT/s
- Medium Frequency band takes advantage of Rx CDR rejection
  - ✓ Allows significantly more Tx eye closure at 1 MHz
  - ✓ Provides relief for non-LC based PLL's
- Low Frequency and High Frequency bands combined into the budget as per 5 GT/s
- Medium Frequency band Root-Sum-Squared (RSS'd) with reference clock Medium Frequency jitter sources

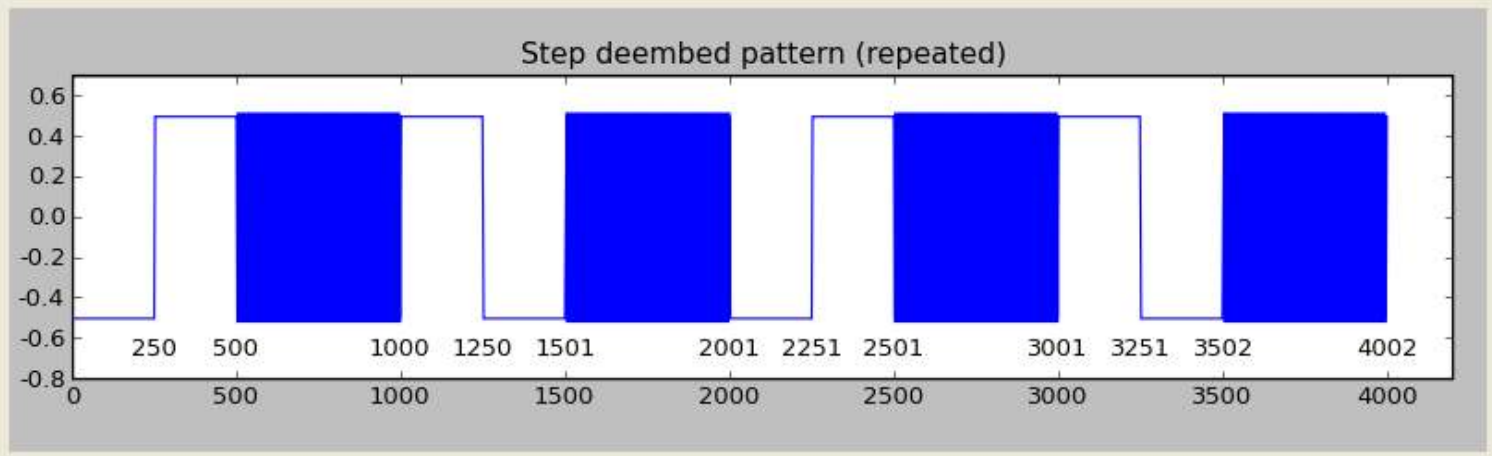


Extracting package S-parameters

- Two main approaches on a compliance board to de-embed from measurement plane to the die pad
  - ✓ Forward bias ESD diodes to measure transmitter Gamma at three different load impedances
    - Solve for SDD22, SDD12 and SDD11
  - ✓ Measure step response of the transmitter at two different output drive strengths, one tuned to 50 ohm, de-embed to ideal driver
    - Solve for SDD22, SDD12 and measure SDD11
- Once full channel S-parameters have been extracted package S-parameters can be deconstructed using the replica channel S-parameters
  - ✓ Final package S-parameters are susceptible to errors from replica channel
- Although both of these approaches are feasible they are complex procedures that have numerous error sources that have to be minimized to get reasonable results

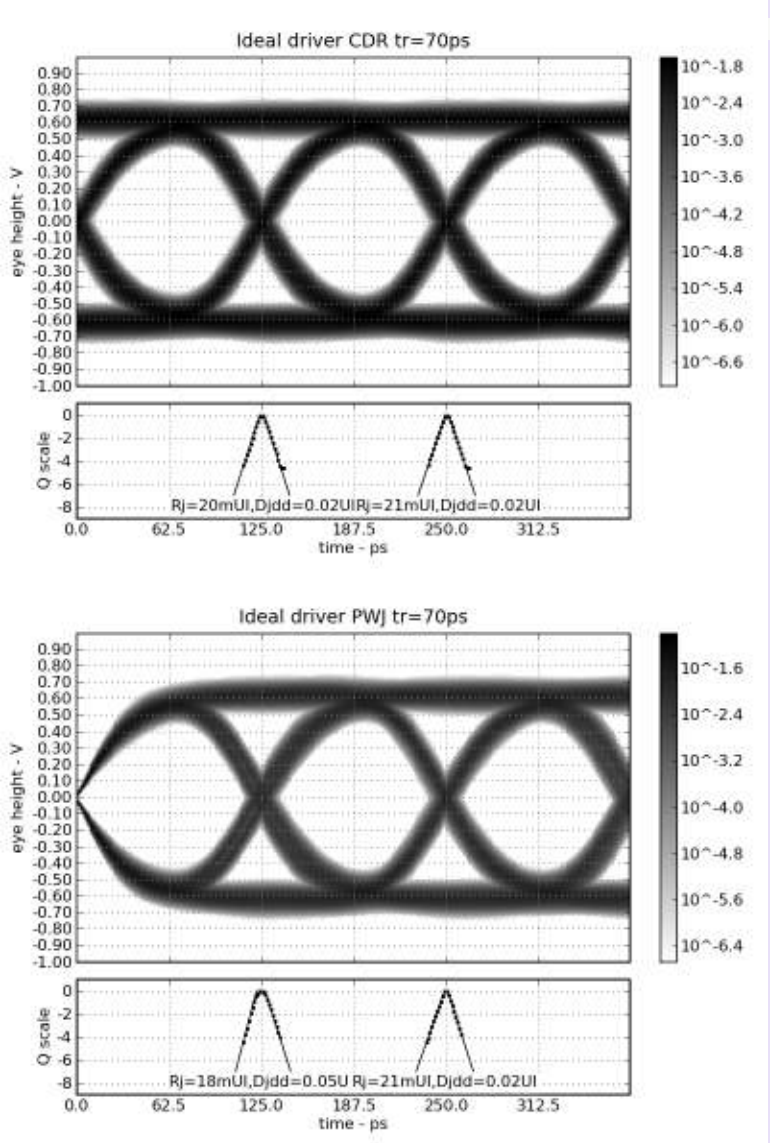
Extracting SDD12 die-pad to measurement plane

- Simplified procedure to de-embed to a compliance Tx model
  - ✓ Use die-pad Rise/fall time used by the Channel Compliance Tx model
  - ✓ Tx R_{OUT} and I_{OUT} determined by LF measurements
    - R_{DC} estimate needed from SMA to die-pad (20% accuracy ok)
  - ✓ Tx data pattern defined that can be used to make step measurement
    - Contains 2 rising steps and 2 falling steps offset by 1UI separated by clock pattern
- A well averaged measurement is made at the compliance measurement plane of rising and falling step using step data pattern
  - ✓ 1UI offset between rising and falling edges averages clock noise
- Step measurements are post processed in the frequency domain to yield pulse response for the channel



Example of Measuring Jitter at 8 GT/s

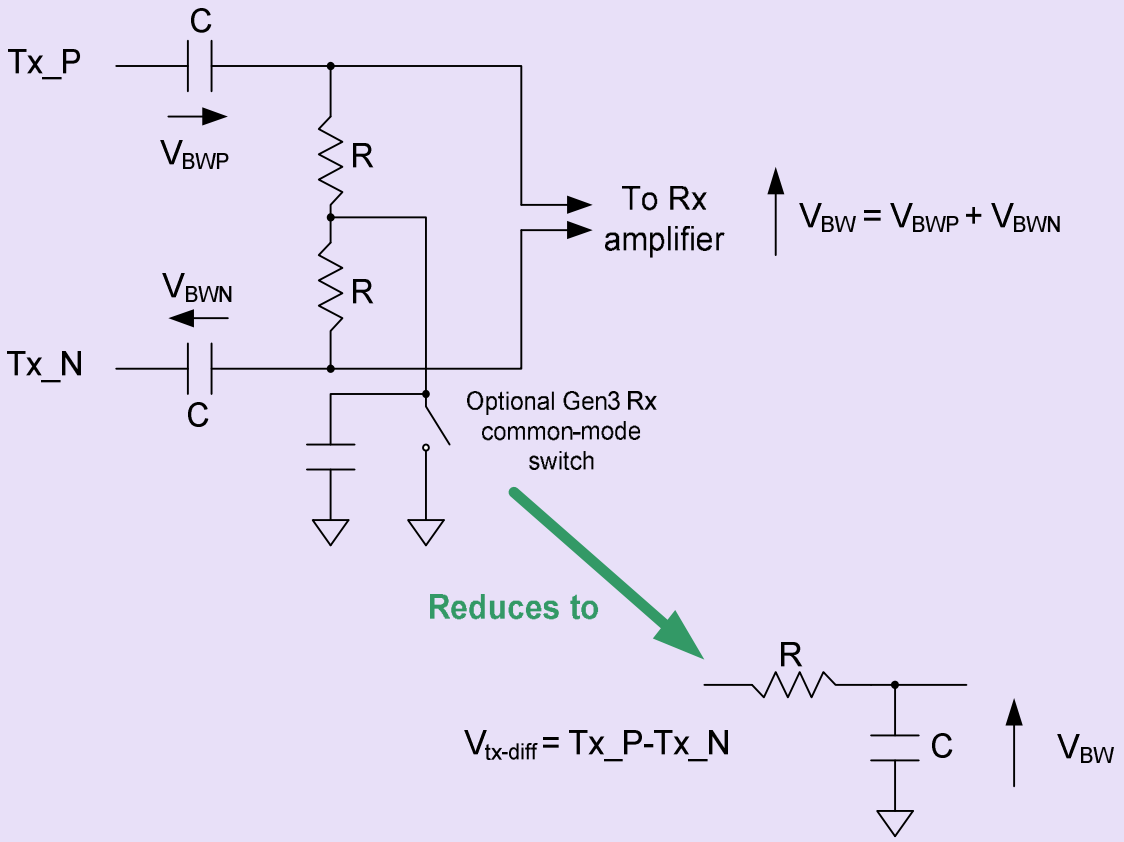
- Using extracted SDD12 calculate channel inverse and de-embed from measurement plane to die-pad
  - ✓ Frequency domain multiplication or time domain convolution
- Two trigger functions required
  - ✓ Idealized CDR model, approximated with a 10 MHz high pass
  - ✓ Edge triggered PWJ model
- For each case generate PDF, convert to Q-scale to get RJ and DJ-DD
- Extrapolate RJ to 10^{-12} BER to calculate TJ
- Measurements include scope noise floor which is largely RJ
  - ✓ This may need to be removed by a test equipment calibration procedure



Baseline wander from PRBS

- 8 GT/s will use scrambled data to improve signaling efficiency over 8b10b encoding used in 2.5 GT/s and 5 GT/s
- Unlike 8b10b a maximal length PRBS generated by an LFSR does not preserve DC balance
  - ✓ The average voltage level over a constant period of time varies slowly based on the pattern of the PRBS
  - ✓ In an AC coupled system this creates a slowly changing differential offset that that reduces eye height
- Different PRBS polynomials have different average run lengths through their pattern and so different peak differential offsets
  - ✓ Discriminating between a ‘good’ and ‘bad’ polynomial cannot be easily done by inspection or by a known mathematical closed form solution
  - ✓ The whole PRBS needs to be searched to find the peak excursion of the differential offset for a given AC coupling time constant
- When random data is xor’ed with the scrambler the ‘bad’ average run lengths are broken up
  - ✓ Worst case is a Pathological match between PRBS and data, which will have very low probability if the PRBS pattern is long

Model used for AC coupling

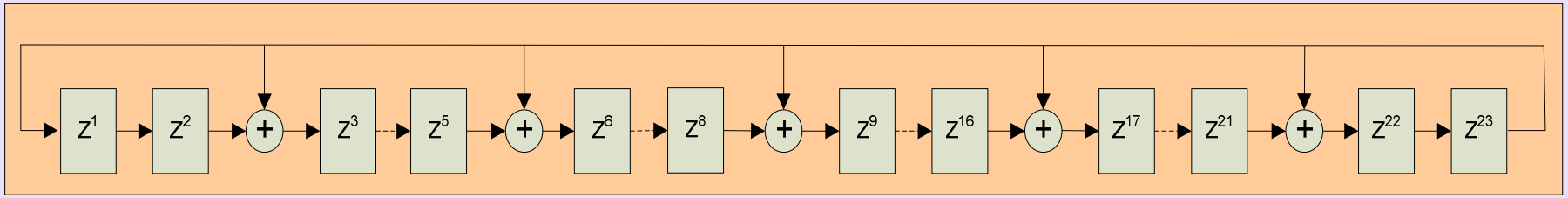


Calculate baseline wander by low pass filtering the differential voltage from Tx when driven by a PRBS

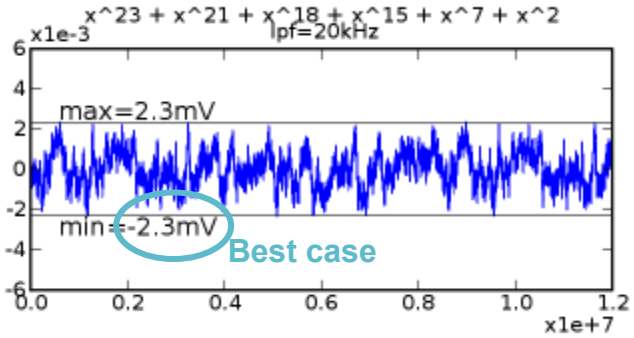
Scrambler Polynomial

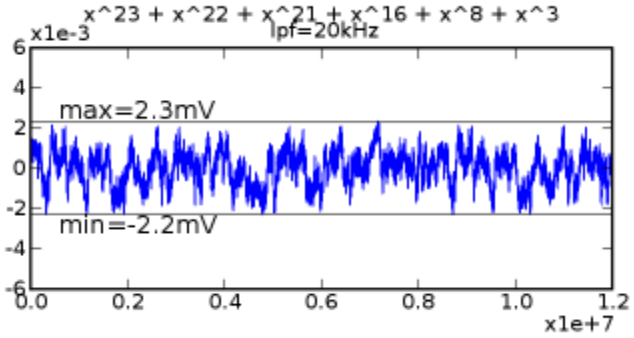
- 8 GT/s uses a 23 bit LFSR to produce the PRBS
  - ✓ Considered to be sufficiently random to get statistical relief from signal interference effects
- A PRBS23 has the following maximal length feedback taps
  - ✓ 2 taps : 2 sets
  - ✓ 4 taps : 146 sets
  - ✓ 6 taps : 2276 sets etc.
    - 6 tap polynomial chosen for its superior baseline wander characteristics
- To maintain commonality with previous PCI-E LFSR implementations, the Galois Polynomial: $z^{23} + z^{21} + z^{16} + z^{8} + z^{5} + z^{2} + 1$ is used

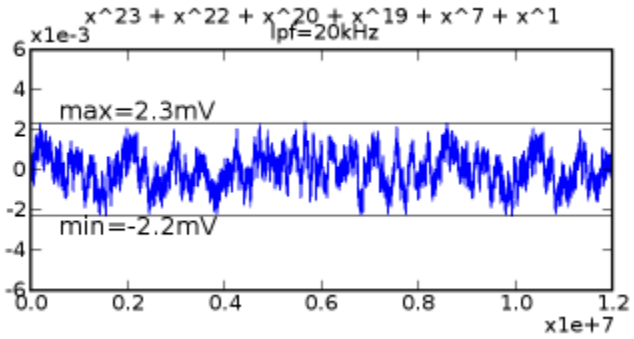
Galois Generator

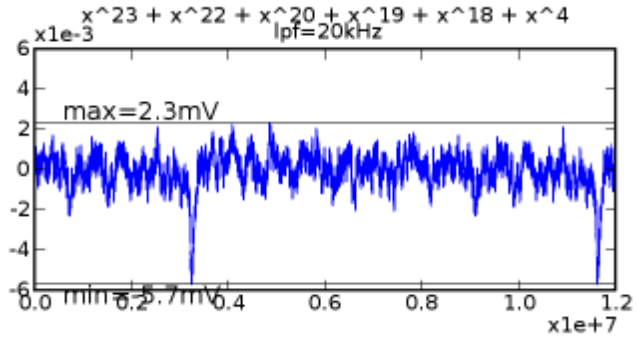


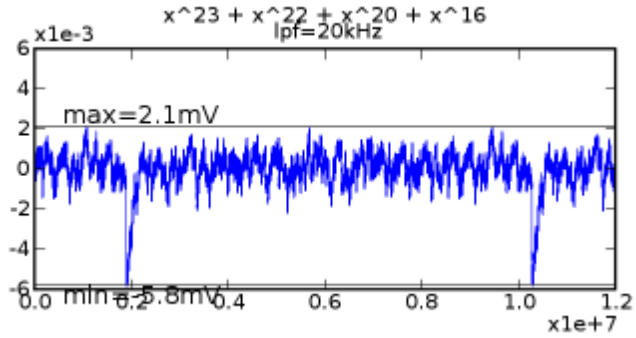
Three best and worst results

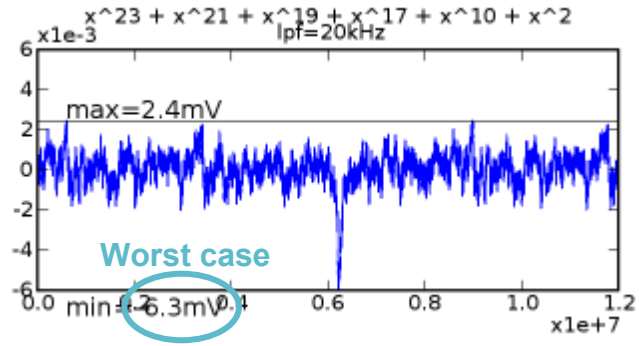












Inter-lane PRBS offsets

- To gain maximum statistical relief from crosstalk the data pattern between lanes needs to be uncorrelated
  - ✓ Worst case to consider is sending mostly 1's and 0's as PRBS for each lane is largely unchanged by data pattern
- De-correlating the crosstalk between lanes can be achieved by introducing a starting offset into the PRBS used for each lane
- It is sufficient to have 8 different offsets that can be repeated in a 16 lane link
  - ✓ Enough to cover nearest neighbor for 2D package breakouts
- There are several goals in choosing these offsets
  - ✓ Minimize correlation from a crosstalk interference perspective
  - ✓ Minimize logic for implementing the generator and offsets
  - ✓ Ensure there is an efficient parallel implementation for the generator

Tap Set Selection Criteria

- XOR-ing combinations of LFSR register stages produces time shifted (offset) versions of the base sequence.
  - ✓ The base sequence is the sequence observed at the z^{23} tap beginning with the initial state of 0x7FFFFF
- Galois XOR input taps selection criteria:
  - ✓ Constrain XOR input taps to 2 terms only (277 choices).
  - ✓ Maximize tap to tap sequence offset.
  - ✓ Minimize number of XOR input terms for 16-bit parallel implementation.
  - ✓ Further constrain inter-lane behavior by adopting one of the two mutually exclusive criteria:
    - Choose a set of LFSR output stages as the XOR inputs so as to minimize inter-lane correlation. (Minimum Galois Taps; MGT)
    - Choose linear dependent LFSR output stages so as to minimize inter-lane X-talk caused by simultaneous switching. (Linear Dependent Taps; LDT)

Linear Dependent Taps

- Galois generator with taps grouped in sets of 3 where the 3rd tap in the group is a "linear" combination of the other two taps. This guarantees, by a simple XOR rule, that within a group of three, only 2 lanes may change in the same time step
  - ✓ For optimal MB placement of > 8 lanes, the 3-tap groups are assigned to lanes as:

Lane	Linear Dependent Taps
0 Seq	A+B
1 Seq	B
2 Seq	B+C
3 Seq	C
4 Seq	C+D
5 Seq	D
6 Seq	D+A
7 Seq	A

  - ✓ The linear dependency is accomplished by having tap groups share common input terms. For example, a linear dependent tap set for a 5 stage LFSR:
    - 3 Taps terms: **{{1,0,1,0,0}, {1,0,0,0,1}, {0,1,0,0,1}}**

Tap Set Comparison

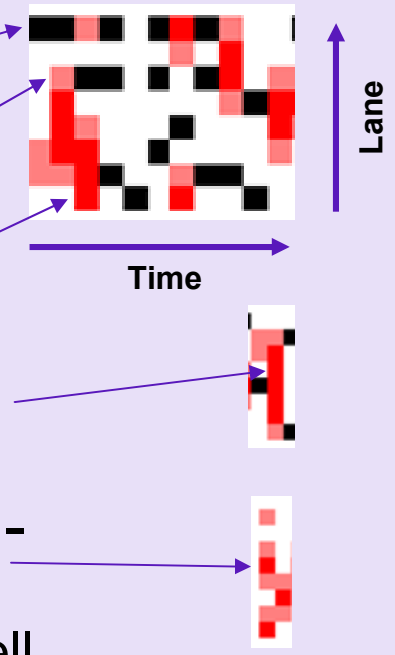
Min Galois Tap Set					Linear Dependent Tap Set				
Tap	**Tap Equation**	**Total Terms**	**Seq Offset**	**Initial Vect**	**Tap**	**Tap Equation**	**Total Terms**	**Seq Offset**	**Initial Vect**
0	z^10 + z^23	51	2963529	0x1d8f60	0	z^10 + z^14	86	3511479	0x1efedc
1	z^8 + z^22	41	3636240	0x71bc06	1	z^2 + z^14	55	2005633	0x6ef030
2	z^2 + z^18	34	3761017	0x7ee20c	2	z^14 + z^23	79	4322974	0x0371bc
3	z^5 + z^19	54	4322969	0x6e3780	3	z^2 + z^23	44	8263834	0x6d818c
4	z^6 + z^17	48	5668600	0x186ef0	4	z^4 + z^23	80	2478402	0x247840
5	z^13 + z^19	55	6196668	0x11bf18	5	z^2 + z^4	54	8388603	0x49f9cc
6	z^4 + z^16	60	7525386	0x443f3c	6	z^4 + z^10	75	0641191	0x39f720
7	z^1 + z^22	48	8263835	0x36c0c6	7	z^2 + z^10	59	1150909	0x700eec
	Total	**391**				**Total**	**532**		

Note that if the delay of an extra XOR stage can be tolerated in the design, the LDT total terms of 532 can be further reduced by adding a final XOR stage to each of the terms for sequences A, B, C, and D. The final XOR stages would produce the terms: A+B, B+C, C+D, and A+D. If this is done, the total terms is reduced to

59+55+44+54+(16*4) = 276

Visualizing crosstalk

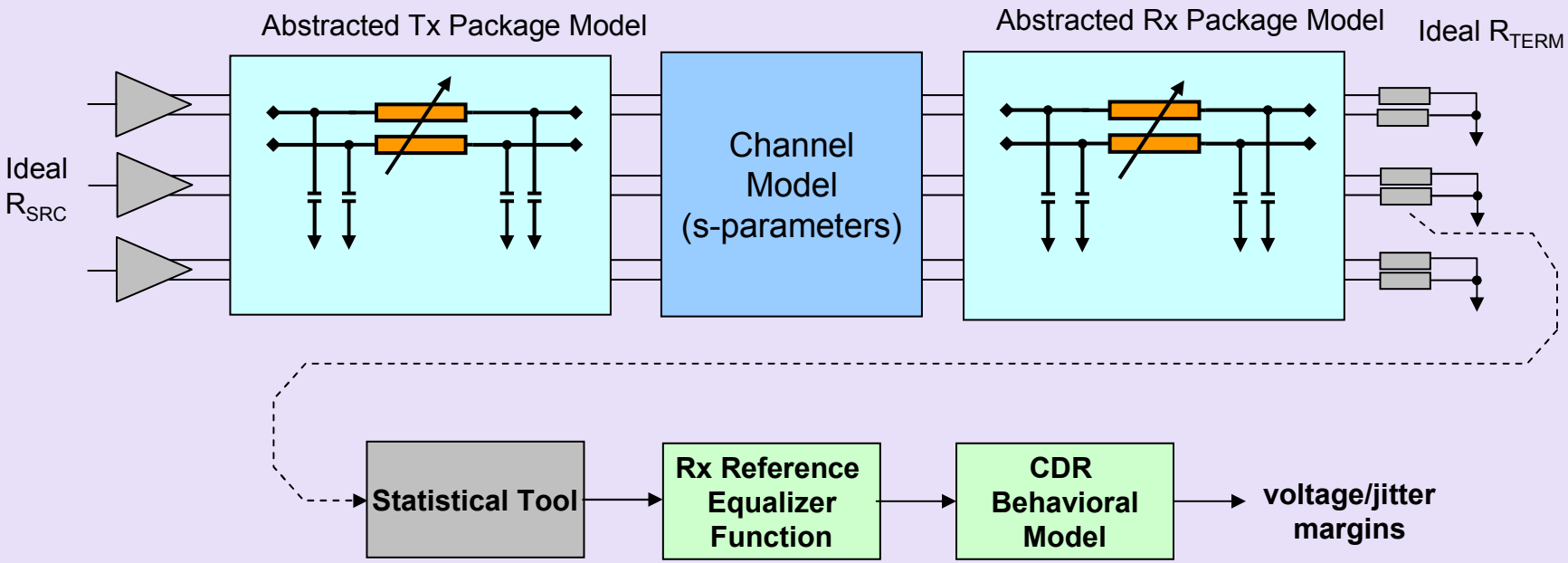
- Each track shows the change sequence for 8 lanes for MGT and LDT
- Color Encoding
  - ✓ White: no change in victim
  - ✓ Black: 1 change, victim only
  - ✓ Pink: 2 changes, victim and one adjacent aggressor
  - ✓ Red: 3 changes, victim and both adjacent aggressors
- MGT is marked by vertical red bands that occasionally span all 8 lanes
- LDT is marked by disjoint vertical pink-red-pink patterns
  - ✓ Lanes 0, 2, 4, 6 never contain a red or black cell by construction



Channel Validation Background

- Channel validation defined in PCIe 2.0 and enhanced in PCIe 3.0
  Channel pass/fail defined only in terms of Tx, Rx parameters
  - ✓ A channel is compliant if, when driven by worst case Tx into worst case Rx, the eye at Rx die pad meets Rx spec (After applying Rx equalizer and CDR behavioral models)
- Start with 5.0 GT/s approach
  - ✓ Capture channel as s-parameter or similar model
  - ✓ Define worst case Tx characteristics
  - ✓ Combine Tx and channel and observe results at far end of channel
- New ingredients are required for 8 GT/s
  - ✓ Tx and Rx parameters referenced to die pad, not the pin
  - ✓ Include abstracted Tx and Rx package models
  - ✓ Reference Rx equalization algorithm
  - ✓ Statistical tool captures data/channel/jitter interaction

Channel Validation Methodology

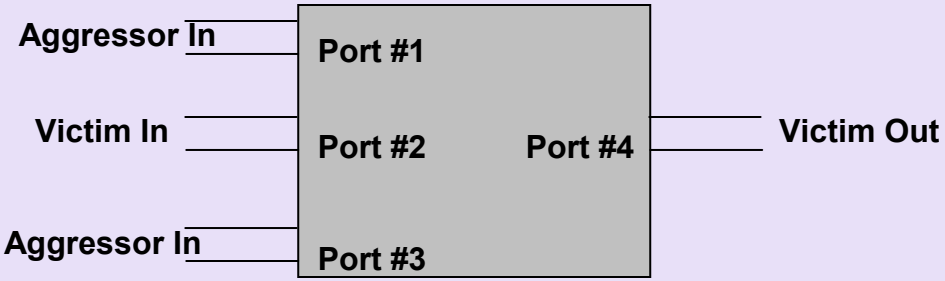


- Channel validation utilizes a combination of measured, fitted, and behavioral models
  - ✓ Channel is measured and converted into s-parameters
  - ✓ Tx, Rx package models are fitted
  - ✓ Rx reference equalizer and CDR are behavioral models
- Statistical tool convolves data pattern with pulse response of channel plus packages

Channel S-parameter Model

- May be obtained by measurement or extraction
  - ✓ VNA is the preferred measurement means
    - Better SNR than TDR/TDT
    - All s-parameter components can be directly obtained
    - Insertion loss, near/far end return loss, crosstalk
  - ✓ Measurement made from Tx pin to Rx pin
  - ✓ At least two aggressor pairs are required to capture crosstalk
    - Some layouts may require >2 aggressor pairs
  - ✓ Extraction from layout file is also acceptable

Client Channel Example

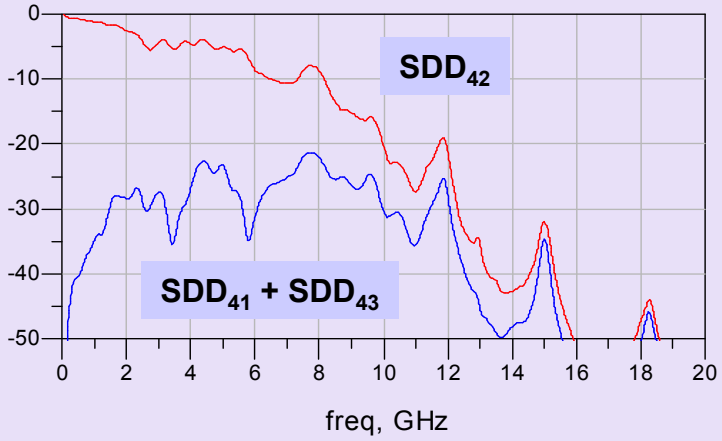


Simulated from Tx die pad to Rx die pad using ADS

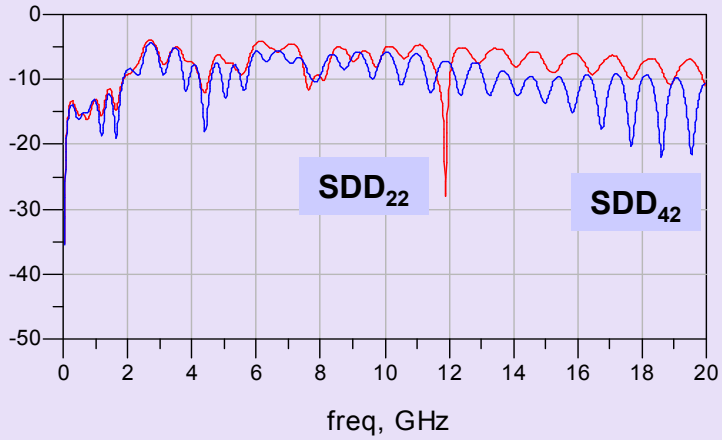
12 inch client channel with one connector routed on microstrip with $Z_{nominal}$ of 85 Ω

Includes two aggressor diff pairs

Plots display differential s-parameters



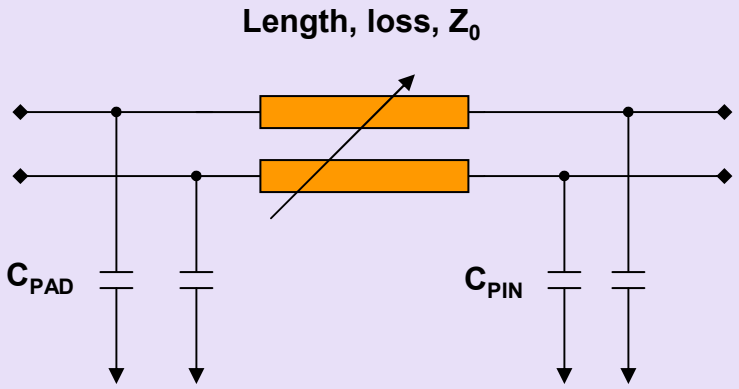
Insertion loss and forward crosstalk



Return loss

Abstracted Tx Package Model

- Fit between Tx model and DUT is done in time domain using pulse response and TDR measurement of DUT
  - ✓ The measured S-parameters of replica channel are used in the Tx model fit to approximate the DUT compliance channel
- Die-pad PWJ, TJ and DJ-DD can be obtained by calculating a channel inverse or by fitting with the model at measurement plane
- Example: Package is definable as a Pi model terms of C_{PIN}, C_{PAD}, and a lossy transmission-line with min/max swept length
  - ✓ Sweeping in necessary to excite potential package/channel resonances
  - ✓ assummes that discontinuities can be captured by C_{PAD} and C_{PIN}

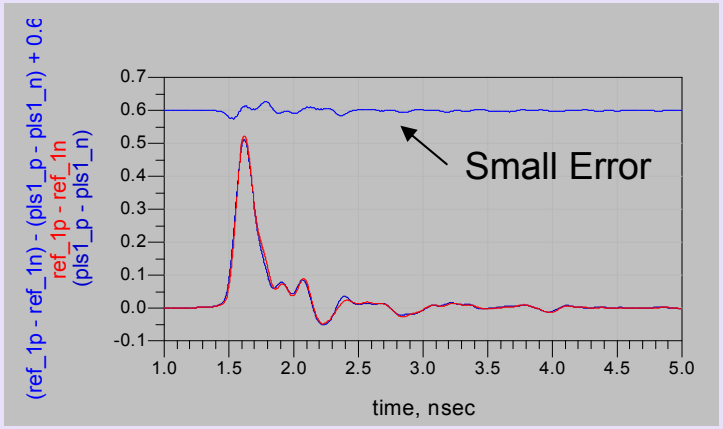


Package Parameters

$C_{PAD} \leq 1.5$ pf (max)
$C_{PIN} \leq 0.5$ pf (max)
50 mils ≤ Length ≤ 1500 mils
80 Ω ≤ Z_0 ≤ 100 Ω
loss/length 0.25 dB/GHz/Inch

Combined Package #1 Plus Channel Models

With abstracted package model

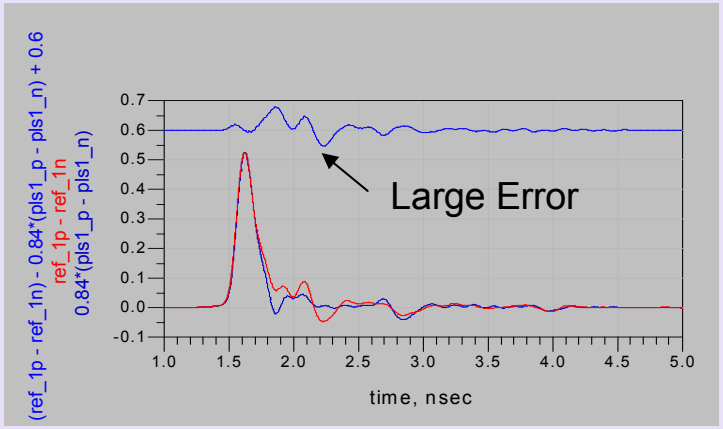


Single UI response at far end of channel

Red: Response with measured package s-parameters

Blue: Response for abstracted package

No abstracted package model



Single UI response at far end of channel

Red: Response with measured package s-parameters

Blue: Response with no package model

(But with corrections for delay and amplitude)

A properly fitted abstracted package model accurately captures the impedance discontinuity and loss characteristics of an actual package

Identifying Worst Case Package/Channel Combination

- Package parameters that are set to nominal values
  - ✓ Loss/length/GHz (fixed value that does not need to be swept)
- Package parameters that are set to maximum values
  - ✓ C_{PIN}, C_{PAD}
- Package parameters set to minimum and maximum values
  - ✓ Z_0: 80 Ω and 100 Ω
- Parameters that are swept
  - ✓ length: 100 – 1500 mils in 100 mil increments
- Both Tx and Rx packages need to be swept, but not necessarily as N^2
  - ✓ Long channels isolate Tx and Rx interactions with the channel

Worst Case Tx Circuit Parameters

- Channel tolerancing reuses the parameters defined in the Tx section of the specification
  - ✓ High speed voltage and jitter parameters are defined at Tx die pad
- Tx voltage parameters
  - ✓ V_{SWING}, De-emphasis presets and tolerances
- Tx jitter parameters
  - ✓ Pulse width jitter over single UI (jitter that can be amplified by the channel)
  - ✓ Data dependent jitter (channel's pulse response convolved with data pattern)
  - ✓ Jitter within CDR tracking range (1 to 10 MHz)
- Low frequency (<1.0 MHz) jitter need not be included in channel simulation, since CDR is assumed to track it
- Tx and Rx die parasitics (C_{PAD}) already captured in abstracted package model

Comprehending Crosstalk

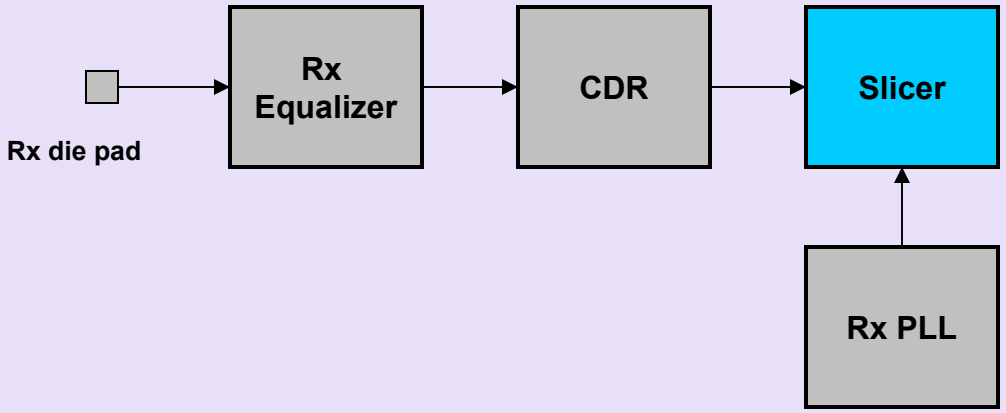
- Two sources of crosstalk must be comprehended
  - ✓ Channel induced
  - ✓ Tx and Rx package induced
- Channel induced crosstalk is already captured in channel model by means of aggressor traces
  - ✓ Number of aggressor traces will range between 0 and 4, depending on routing details
- Package crosstalk is still under investigation
  - ✓ One option may be to reference package crosstalk to Tx die pad as an RMS noise level
  - ✓ A similar approach could be used for the Rx, where an additional RMS noise level would be added during calibration of the tolerancing setup.

Tx De-Emphasis Settings

- Both transmitter and receiver utilize equalization, and both must be adjusted to match the particular channel under consideration
- Tx: Select one of N presets that represents best match to channel
  - ✓ Tap values TBD, but will need to address mobile, client, server channels
    - Preset #1: half swing for mobile apps, one postcursor tap
    - Preset #2: full swing no de-emphasis
    - Preset #3: full swing one postcursor and one precursor tap
    - Preset #4: full swing one postcursor and one precursor tap
- Tolerance of Tx de-emphasis settings used for channel validation must be consistent with worst case tolerances in the Tx specification

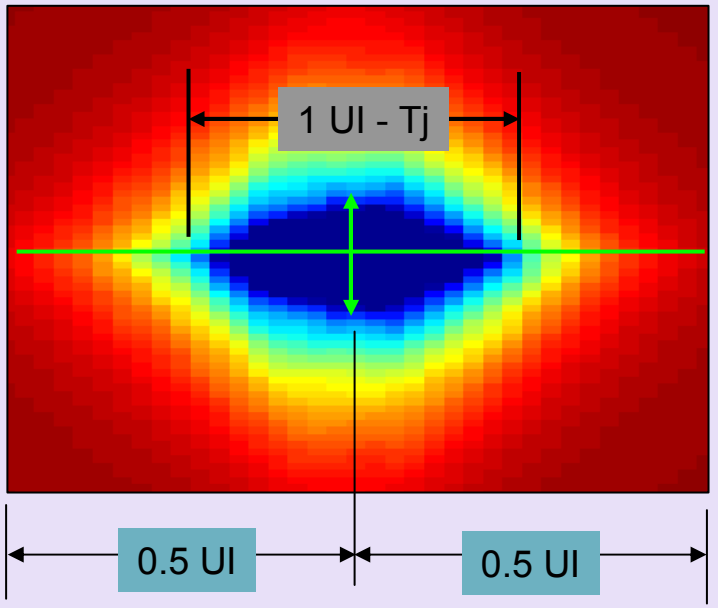
Observing the Output Signal

- Signal at Rx die pad will not convey meaningful results
  - ✓ Eye may be closed
- Desired signal observation point is at virtualized input to the Rx slicer
  - ✓ Rx reference equalization must be applied
  - ✓ CDR behavior must be comprehended



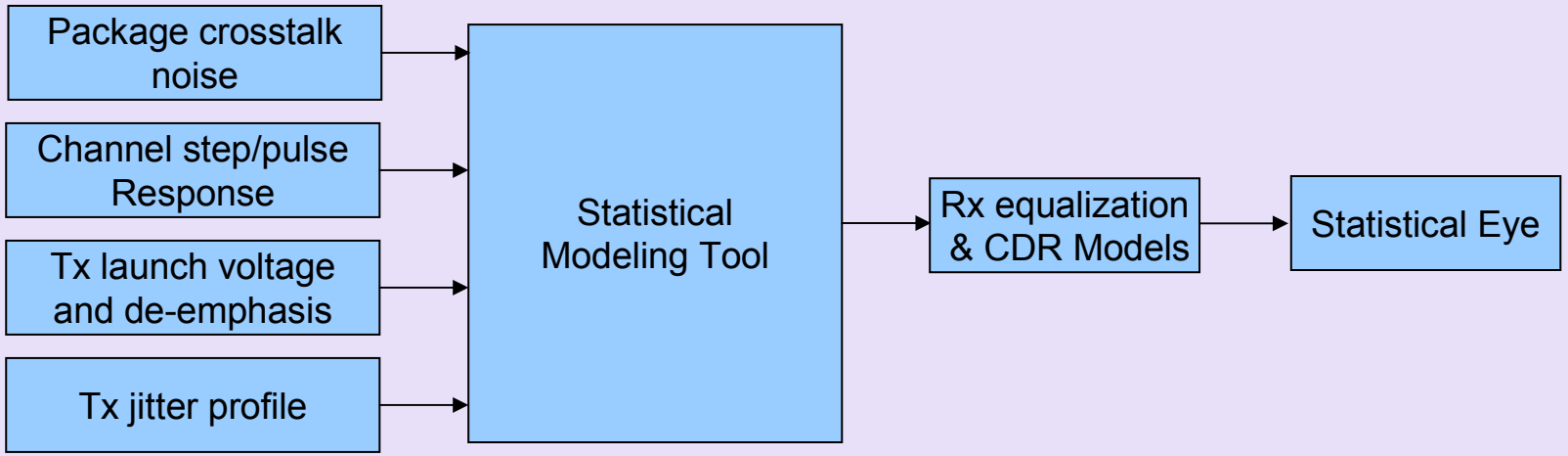
CDR Behavioral Model

- Channel tolerancing must make some basic assumptions regarding CDR characteristics
- Minimum assumption is how CDR samples eye with respect to UI boundaries
- Assume eye height is measured at median center of UI
- Other CDR characteristic may be its nonlinear behavior (bang-bang) function



Statistical Jitter Analysis Tool

- Required tool capabilities
  - ✓ Accept channel step or pulse response
    - Include crosstalk from adjacent lanes
  - ✓ Convolve channel response with PRBS data pattern
  - ✓ Include Dj, Rj terms
  - ✓ Generate statistical eye diagram
- Open source software (Stateye) is preferable
- Specification will need to include scripts or references thereto



Review: Channel Validation Steps

- Extract s-parameters for the channel under test.
- Append abstracted Tx and Rx package models to the channel model. Sweep Tx and Rx package parameters to determine the worst case package/channel interaction
- Select the Tx de-emphasis preset yielding minimum pulse distortion
- Run the virtual Rx equalizer training process to select optimum Rx equalization settings
- Using a statistical tool, simulate worst case Tx jitter and voltage into model consisting of channel plus abstracted Tx and Rx package models. Include Tx de-emphasis, Rx equalization, and CDR behavioral model.
- Resulting statistical eye must meet Rx voltage and jitter requirements as defined at the die pad

Rx Tolerancing Background

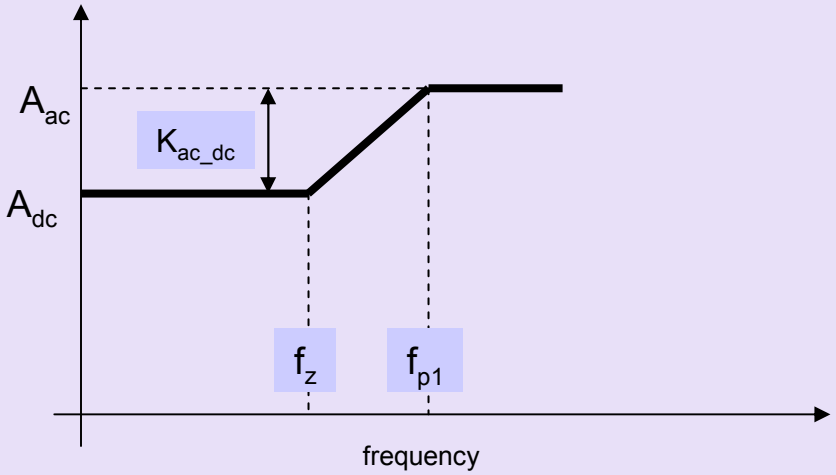
- Start with PCIe 2.0 approach
  - ✓ Step #1: calibrate test setup into reference load to yield worst case voltage/jitter margins
  - ✓ Step #2: replace load with DUT and observe BER
- Add enhancements based on PCIe 3.0 methodology
  - ✓ Dealing with closed eye at Rx
  - ✓ Channel interactions with non-ideal package
  - ✓ Select reference plane for monitoring voltage/jitter during calibration
  - ✓ Comprehend jitter statistically, including ISI – pattern effects
  - ✓ Updated jitter binning

Dealing with Closed Rx Eye

- At 8.0 GT/s Inter Symbol Interference (ISI) and other jitter effects will close the eye
  - ✓ Two possible approaches to address the problem
    - – Reference equalization to open eye
    - – Calibration of pattern generator so jitter is known without eye measurement
- Reference Rx equalization algorithm will open eye, making jitter measurement possible for the calibration process
  - ✓ Applies a minimum capability 1st order linear equalization algorithm
  - ✓ Replicates minimum capability equalization that any compliant Rx would apply
  - ✓ For a fixed calibration channel, reference equalizer parameters may be fixed

Rx Reference Equalizer

- Reference equalizer represents minimum Rx requirements to guarantee interoperability
  - ✓ Defined by a simple transfer function
  - ✓ Actual Rx equalizer must be as good or better
- Rx: Rx equalizer is defined by several parameters
  - ✓ AC vs. DC gain, Zero frequency
- Goal is to minimize number of parameters that need to be adjusted
  - ✓ AC vs. DC gain from K_{AC-DC} = 1 to 4 in 16 steps

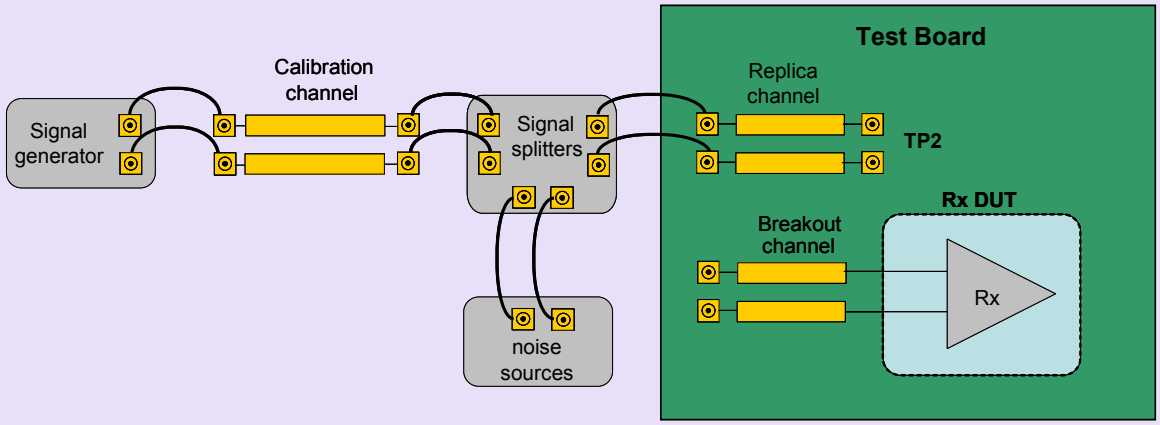


$$A_{dc} = A_{ac} / K_{ac\_dc}$$

$$f_{p1} = f_z * K_{ac\_dc}$$

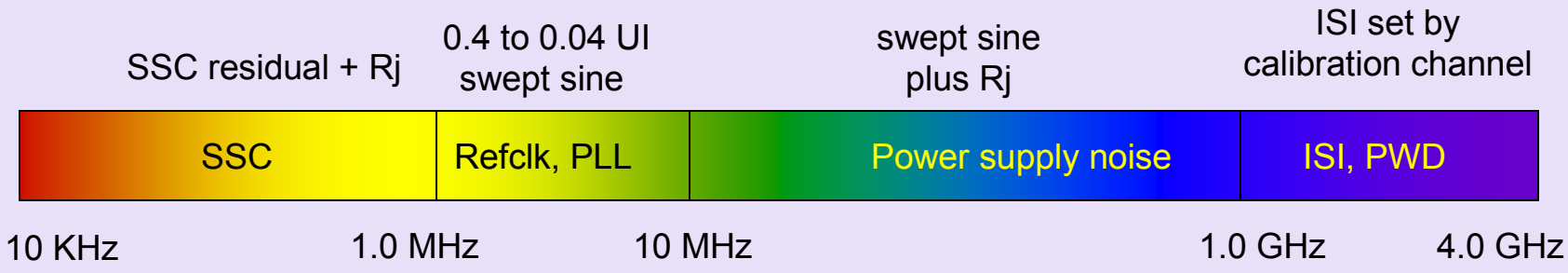
Selection of Reference Plane

- Selection of reference plane based on accuracy, ease of measurement, and post processing overhead
- The measurement reference plane for receive compliance testing is defined by TP2, which corresponds to the pin of the DUT:
  - ✓ Does not account for package characteristics
    - In particular, package return loss and package insertion loss
    - Voltage at die pads may be smaller for loss dominated package
    - Voltage at die pads may be larger for reflection dominated package



Jitter Injection

- A receiver must meet 10^{-12} BER when receiving a signal that has worst case jitter simultaneously over several frequency ranges
  - ✓ 10 KHz to 1.0 MHz: SSC residual and low frequency Rj
  - ✓ 1.0 MHz to 10.0 MHz: single tone frequency dependent sine
  - ✓ 10.0 MHz to 1.0 GHz: single tone sine plus Rj

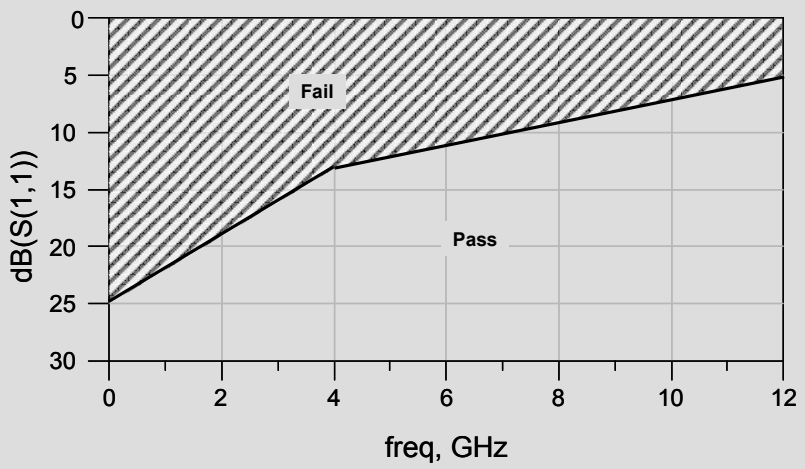


Calibration Channel

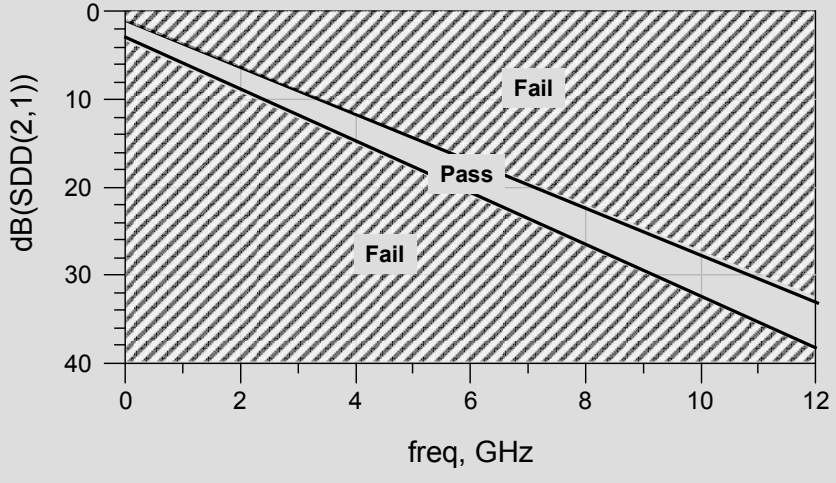
- Channel may be fabricated as isolated pair of transmission-lines matching both nominal $Z_{0\text{-DIFF}}$ and $Z_{0\text{-CM}}$
- Length selected to yield near maximum $V_{MIN\text{-}MAX\text{-}RATIO}$
  - ✓ Typical length for 8.0 GT/s is 15” of FR4 or 40” of Nelco 4000-13
- Calibration channel obviates need for Tx de-emphasis
  - ✓ Pattern generator drives full swing pulse output
  - ✓ Receiver does not know or care about de-emphasis, only about certain input voltage and jitter parameters
- Calibration channel should include 220 nf series caps to induce DC wander

Emulating ISI

- ISI is a key high frequency phenomenon that limits Rx performance
- May be easily generated with a calibration channel
- Calibration Channel also captures effects of pulse width distortion



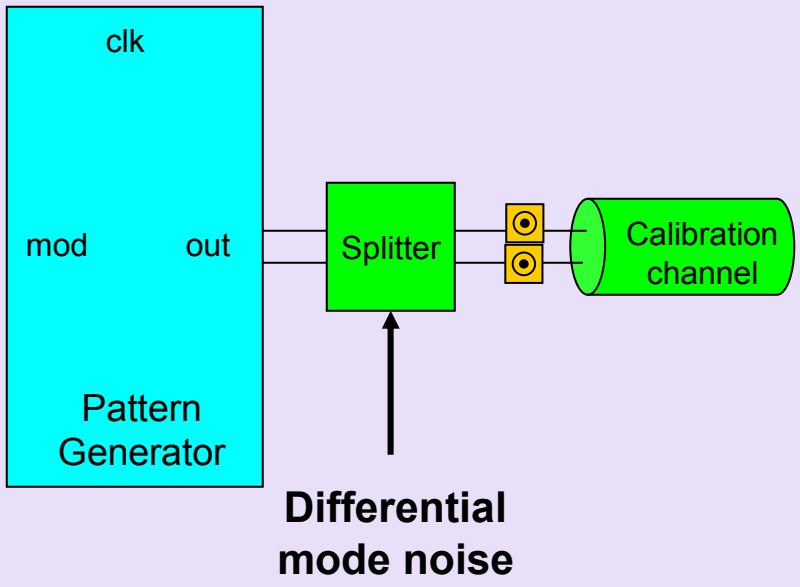
Calibration Channel Return Loss



Calibration Channel Insertion Loss

Tuning $V_{MIN-MAX-RATIO}$ and $T_{MIN-PULSE}$

- Calibration channel may not be exactly able to meet the $V_{MIN-MAX-RATIO}$ and $T_{MIN-PULSE}$ parameters
- Addition of a differential noise source at output of pattern generator gives us an additional degree of freedom



CDR and High Frequency Jitter

- CDR performance will be characterized in terms of jitter tracking over 1.0 to 10.0 MHz bandwidth
  - ✓ 0.4 UI at 1.0 MHz to 0.04 UI at 10 MHz
- High frequency jitter (10 to 1000 MHz) injected as a constant amplitude over range of frequencies
- Rx testing would drive sine wave of appropriate amplitude at several frequencies
  - ✓ Rx under test would need to meet 10^{-12} BER at each frequency

Sine Wave Freq	Jitter
1.0 MHz	0.4 UI
2.0 MHz	0.2 UI
5.0 MHz	0.08 UI
10.0 MHz	0.04 UI

Values for demonstration only

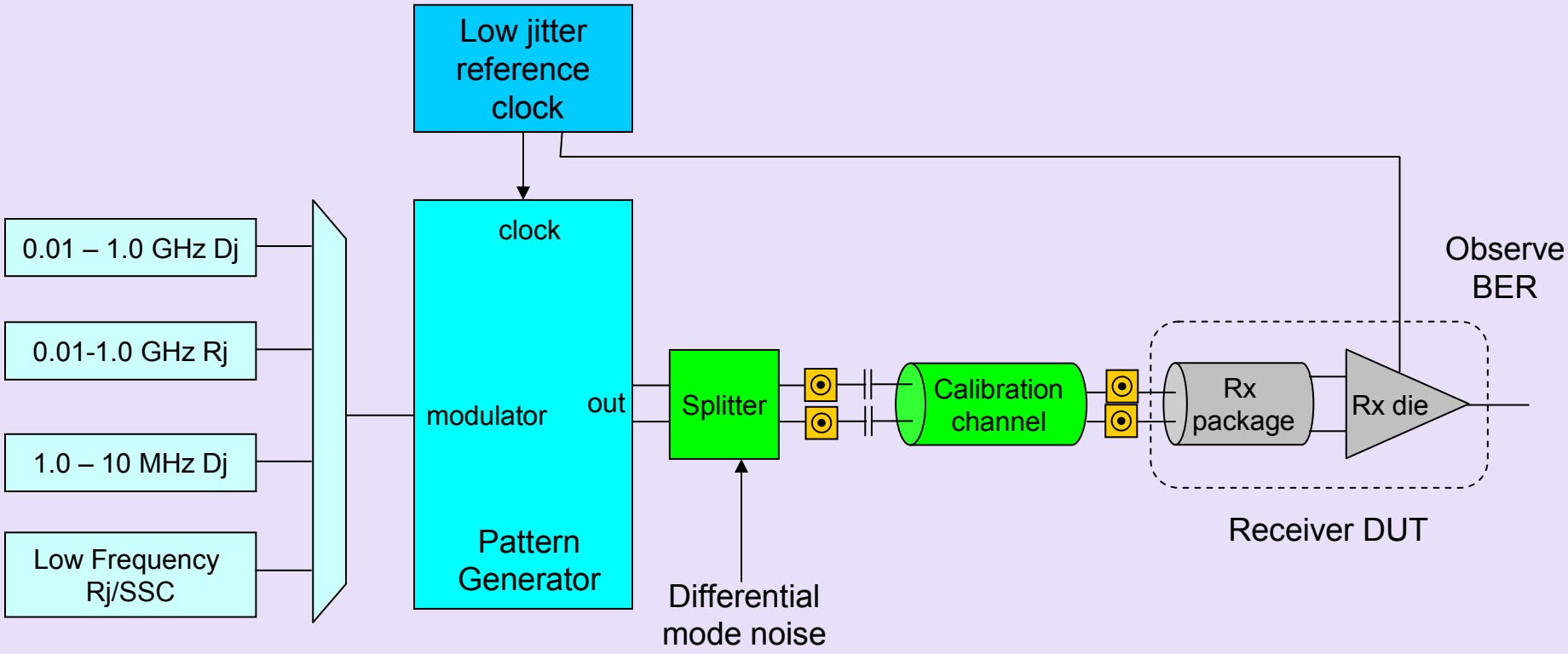
1.0 – 10 MHz Dj

Sine Wave Freq	Jitter
20 MHz	10 ps
50 MHz	10 ps
100 MHz	10 ps
200 MHz	10 ps
500 MHz	10 ps
1.0 GHz	10 ps

Values for demonstration only

10 MHz – 1.0 GHz Dj

Tolerancing Receiver Under Test



BER test needs to be run for each of the swept jitter frequencies

Thank you for attending the PCIe Technology Seminar

Acknowledgements to Gerry Talbot, Jeff Morriss and all EWG members for their contributions to this presentation.

For more information please go to www.pcisig.com