
PCI
SIG
PCI Express® 2.0
Architecture Overview / Compliance
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EXPRESS

Agenda

- Overview of PCIe® 2.0 Base Specification
  - ✓Protocol/Logical/Config
  - ✓Electrical
    - Jitter Overview
    - TX requirements
    - RX requirements
- Overview of PCIe 2.0 CEM Specification
  - ✓CEM vs Base Specifications
  - ✓Eye Diagram Limits
  - ✓MB and Add-in Card TX Methodologies
- Overview of PCI-SIG® 2.0 Compliance Program

PCIe 2.0 Protocol/Logical/Config Update Summary

- Speed Negotiation
  - ✓ Dynamic
    - Power management
    - Reliability (2.5 GT/s fallback)
  - ✓ Software notifications possible on changes.
- Config Changes
  - ✓ Target link speed
  - ✓ Hardware autonomous speed control
  - ✓ Link bandwidth change mechanism
- Electrical Idle Detection
  - ✓ New low frequency electrical idle exit sequence (EIES)
  - ✓ Sent periodically with TS1/TS2 (one every 2).
- Electrical Idle Entry
  - ✓ Option for logical detection for entry condition.

Jitter Overview

- System jitter must meet following relationship:

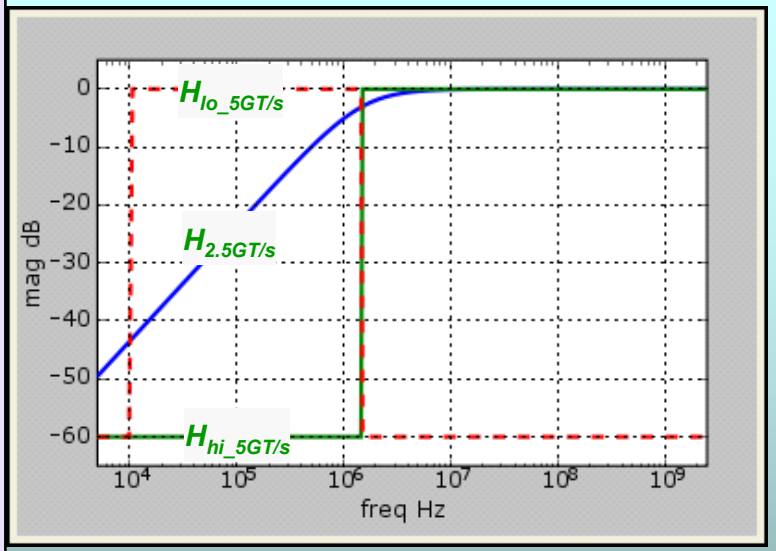
$$System\ T_J \equiv \sum Dj_{DD} + 2Q_{BER}\sqrt{\sum Rj_{DD}{}^2} \leq 1.0UI$$

$$Component\ T_J \equiv Dj_{DD} + 2Q_{BER}Rj_{DD}$$

  - Jitter is separated into two bins at 1.5 MHz
    - ✓ Below 1.5 MHz it is assumed that Rx CDR can track the jitter, up to some max
    - ✓ Above 1.5 MHz, it is assumed that CDR cannot track the jitter
    - ✓ Jitter > 1.5 MHz is counted in system jitter budget
  - Binning is utilized for Tx, Rx, and Refclk
    - ✓ Spec places upper limit on jitter for both bins

Tx Jitter Filtering

- Tx under test driven by “ideal”, very low jitter Refclk
- Different Tx filters applied for 2.5 vs. 5.0 GT/s
  - ✓ 2.5 GT/s utilizes a 1-pole HPF with fC of 1.5 MHz
  - ✓ 5.0 GT/s uses 2 filters
    - 10 KHz – 1.5 MHz brick wall BPF
    - 1.5 MHz brick wall HPF
- Filters remove jitter:
  - ✓ Measurement artifact
  - ✓ Otherwise trackable by Rx



$$H_{2.5GT/s} = \frac{s}{s + w_c} \qquad w_c = 2\pi f_T$$

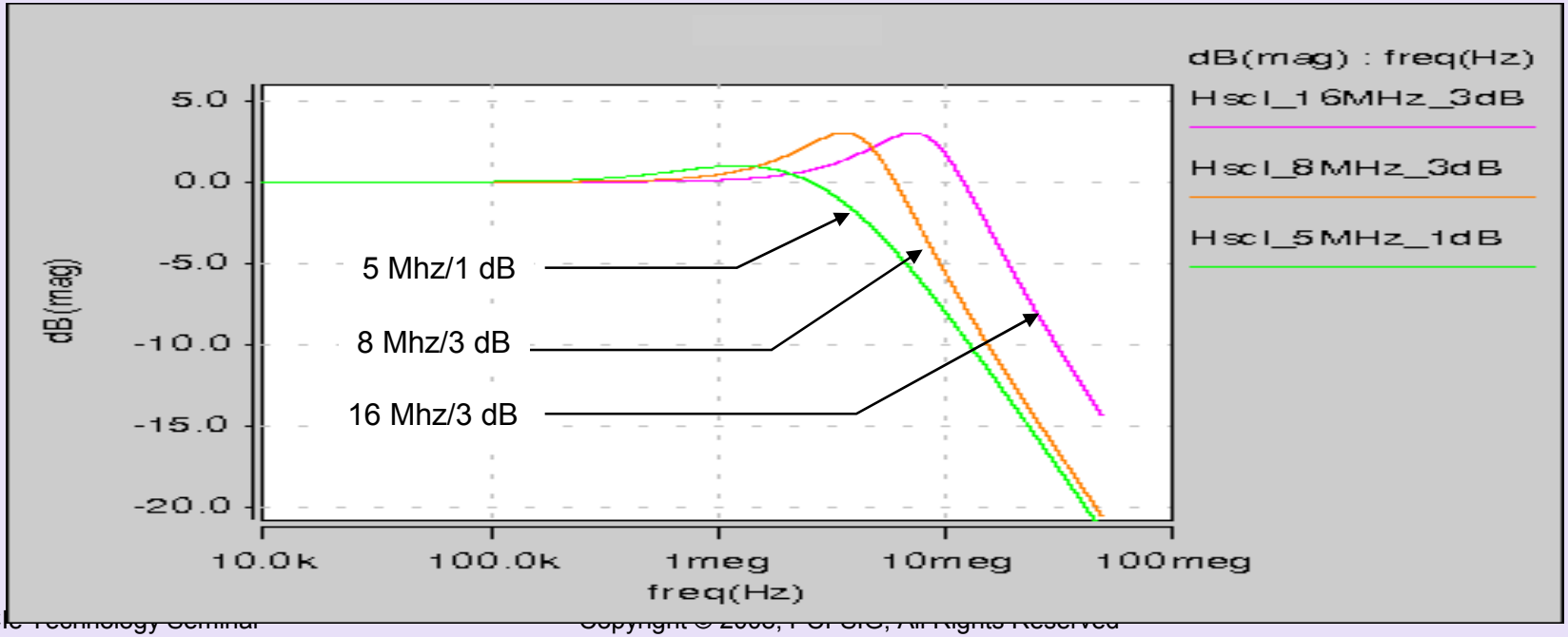
$$H_{hi\_5GT/s} = if\,(f >= f_T)\ then\ 1.0\ else\ 10^{-3}$$

$$H_{lo\_5GT/s} = if\,(f < f_{10kHz})\ then\ 10^{-3}$$
$$elseif\ (f < f_T)\ then\ 1.0$$
$$else\ 10^{-3}$$

$$f_T = 1.5MHz$$

Tx PLL Characteristics

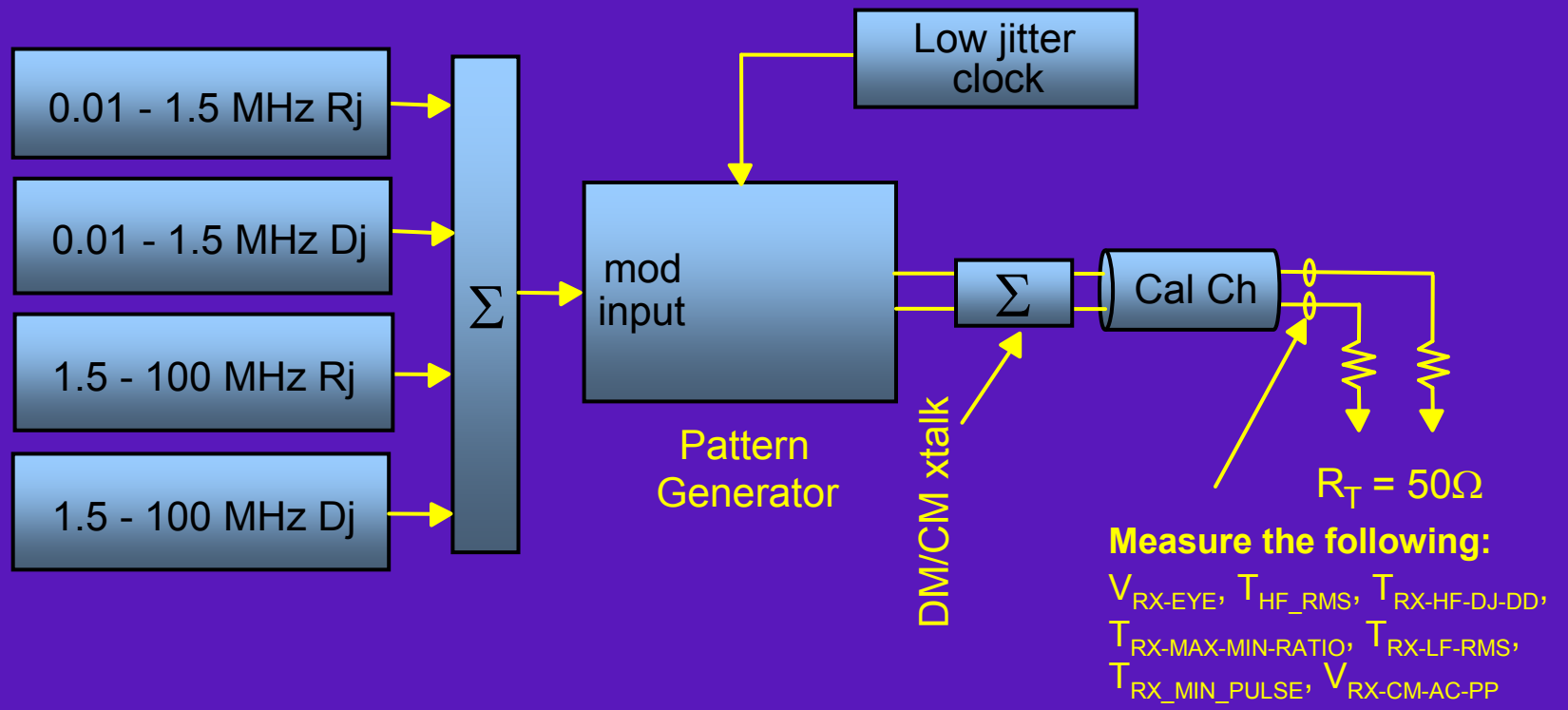
- 5.0 GT/s requires Tx PLL bandwidth and jitter peaking to be more tightly controlled than for 2.5 GT/s
  - ✓ 2.5G had sufficient margin to allow a wide (1.5-22 MHz) PLL range
- Two combinations of min PLL peaking/BW defined
  - ✓ 5.0 MHz with 1.0 dB or 8.0 MHz with 3.0 dB
  - ✓ Max PLL BW/pkg = 16 MHz/3.0 dB



Rx Characterization

- Advantages of a Tolerancing-based Rx spec
  - ✓ Minimizes guardbanding
  - ✓ Only output an Rx can provide is BER as function of inputs
  - ✓ Proven in other high speed Comm interfaces
- Procedure
  - ✓ Build test setup capable of injecting into receiver worst case margins as defined in Rx spec table
  - ✓ Calibrate setup into precision reference load
  - ✓ Replace reference load with Rx under test and observe BER
- Calibration Channel
  - ✓ Provides worst case VRX-MIN-MAX-RATIO

Calibrating Rx Margining Setup



- Test setup shown represents functionality only, not actual instruments
- Inputs adjusted until parameters at R_T are at minimum values defined in spec
- Low jitter Refclk obviates need for 2-port measurement
- Direct measurement of 10-12 BER is possible in <20 minutes
- Other lanes within same Rx under test need to be driven

PCIe 2.0 Key Design Challenges

- TX Jitter compliance
  - ✓ Requires very low jitter PLL
  - ✓ Requires very low jitter Refclk source
  - ✓ Requires delicate clock network design and layout
  - ✓ Requires very low noise supply
    - Needed to design Power Delivery which would reduce supply noise by more than 30% from Gen1
    - Accurate Power Delivery model which would take into account data dependent noise pattern
- RX Jitter compliance
  - ✓ Requires low latency clock recovery loop
    - Had to reduce loop latency by ~50% from Gen1
  - ✓ Requires very delicate and careful clock distribution design with accurate phase relationship.
  - ✓ Need to pay close attention to Rx input CAP (<1 pF) to avoid jitter penalty.
- Squelch
  - ✓ Difficult to limit threshold variation of the detector and detect both EI entry & Exit

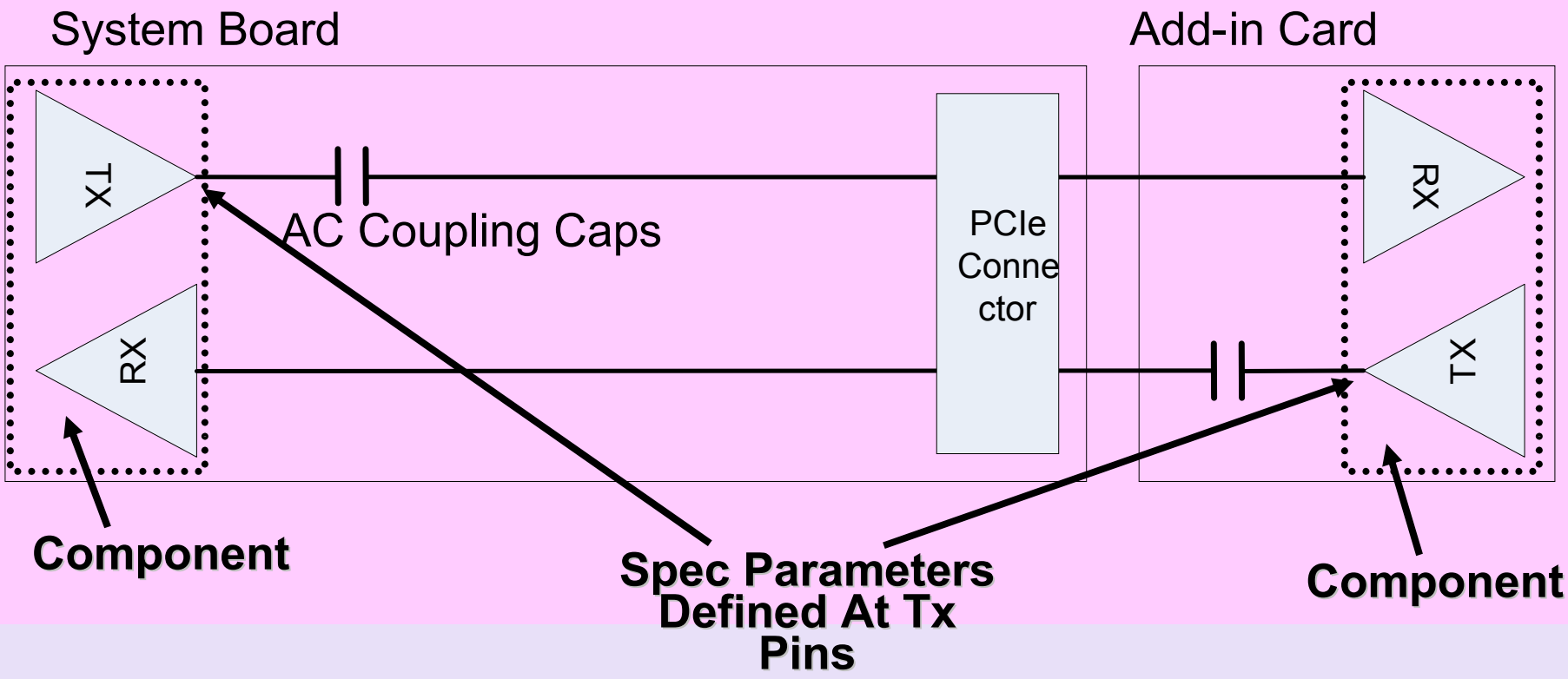
PCIe 1.1 – PCIe 2.0 CEM Changes

PCIe 1.1 CEM Spec Section	Areas Of Change
Auxiliary Signals	Reference Clock (Jitter)
Hot Insertion And Removal	None
Electrical Requirements	Electrical Budgets Eye Diagrams
Connector Specification	Signal Integrity Requirements and Test Procedures
Add-in Card Form Factors And Implementation	Card Interoperability

No Required Mechanical* Changes From 1.1 CEM Spec

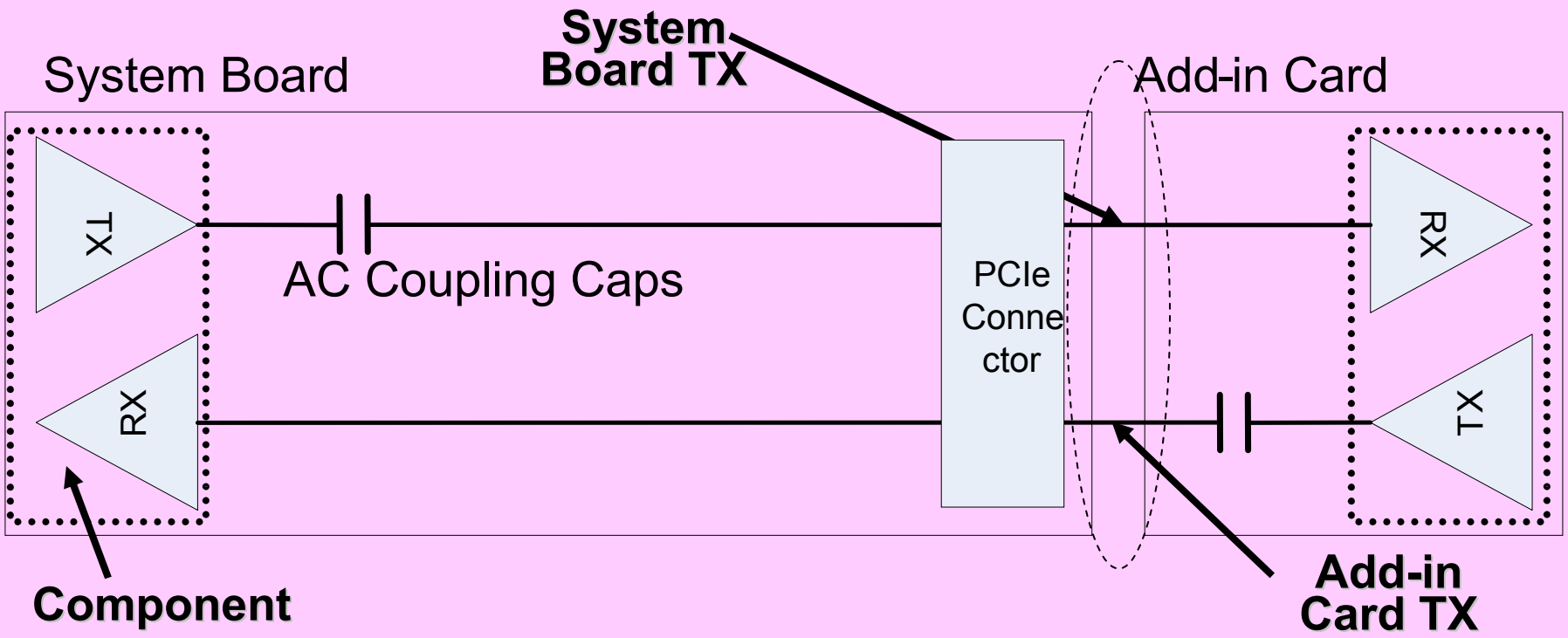
***Connecter Retention Ridge Optional**

PCIe Base 2.0 – Tx



Base TX Spec Is A Chip Spec At Chip Pins

PCIe CEM 2.0 – Tx Path

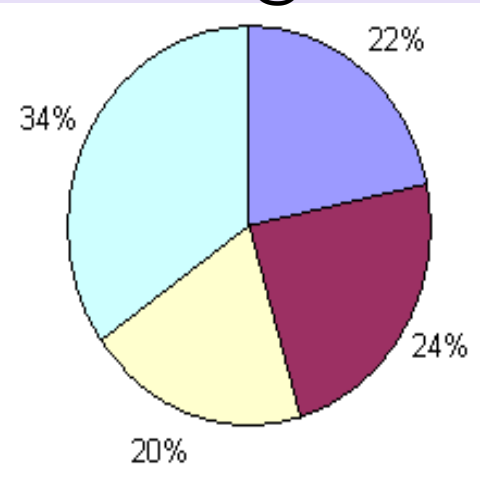


CEM Spec Defines TX Requirements for Chip + Interconnect

No Separate TX Chip Or Interconnect Only Requirements

CEM Budgets & Topologies

1.1 CEM @ 10^{-12}

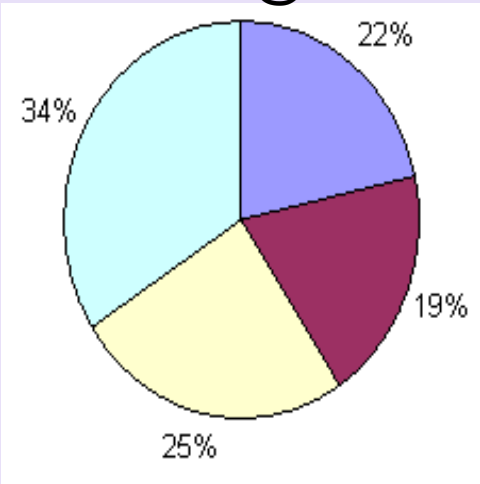


$$T_J = \sum D_J + \sqrt{\sum R_J^2} \leq 400 \quad ps$$

Relative budget percentages unchanged between 2.5 and 5.0 GT/s. Overall budget half the size.

- **TX**
- **Clock**
- **Channel**
- **RX**

2.0 CEM @ 10^{-12}

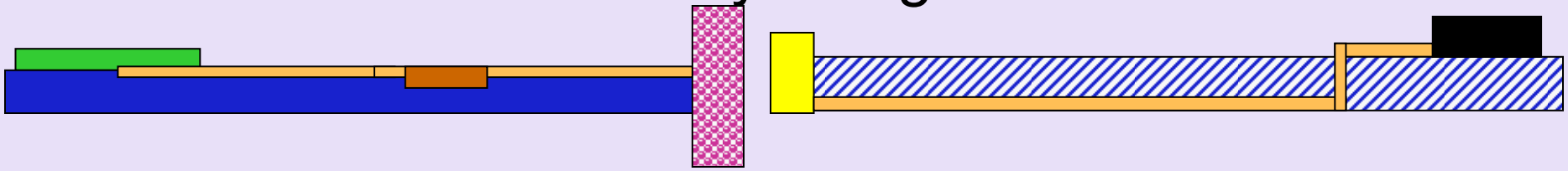


$$T_J = \sum D_J + \sqrt{\sum R_J^2} \leq 200 \quad ps$$

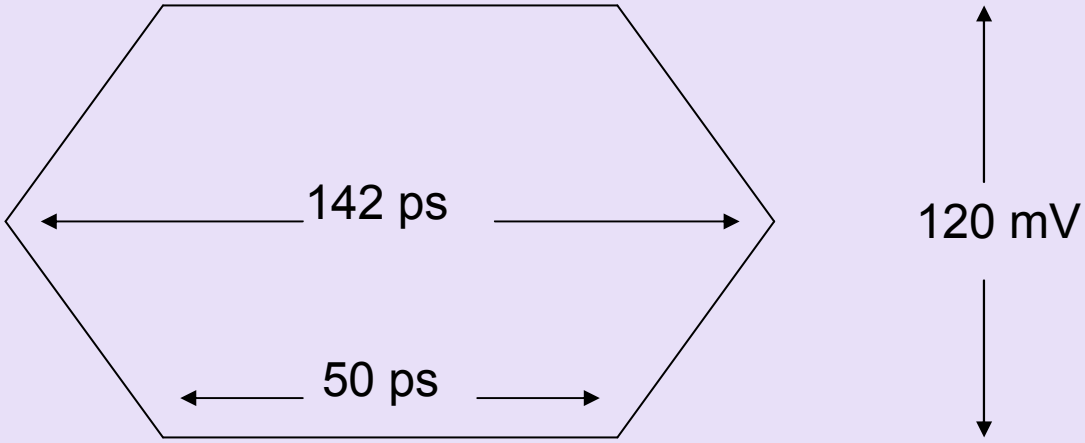
	2.5G – One Connector	2.5G – Two Connector	5G – One connector	5G – Two Connector
Channel Impedance	100Ω	100Ω	85Ω	85Ω
Trace Type	Microstrip	Microstrip	Microstrip	Stripline
MB Length	12”+	16”+	6-8” – 85Ω	16” – 85Ω

Tx Eye Methodology

- Simulate end to end eye diagrams

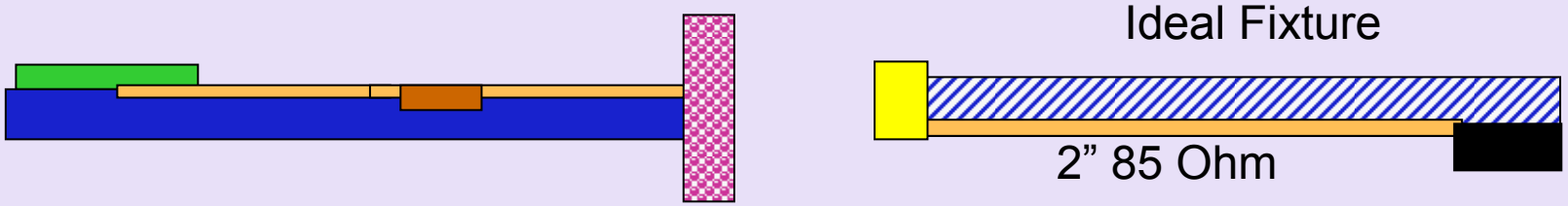


- Identify all end to end failures (worst case pattern)
  - 120 mVolt Eye Height (Base Spec Rx Pin Limit)
  - 142 ps Eye Width (Interconnect only) (Base Spec Channel Limit)



System Board Tx Eye Methodology

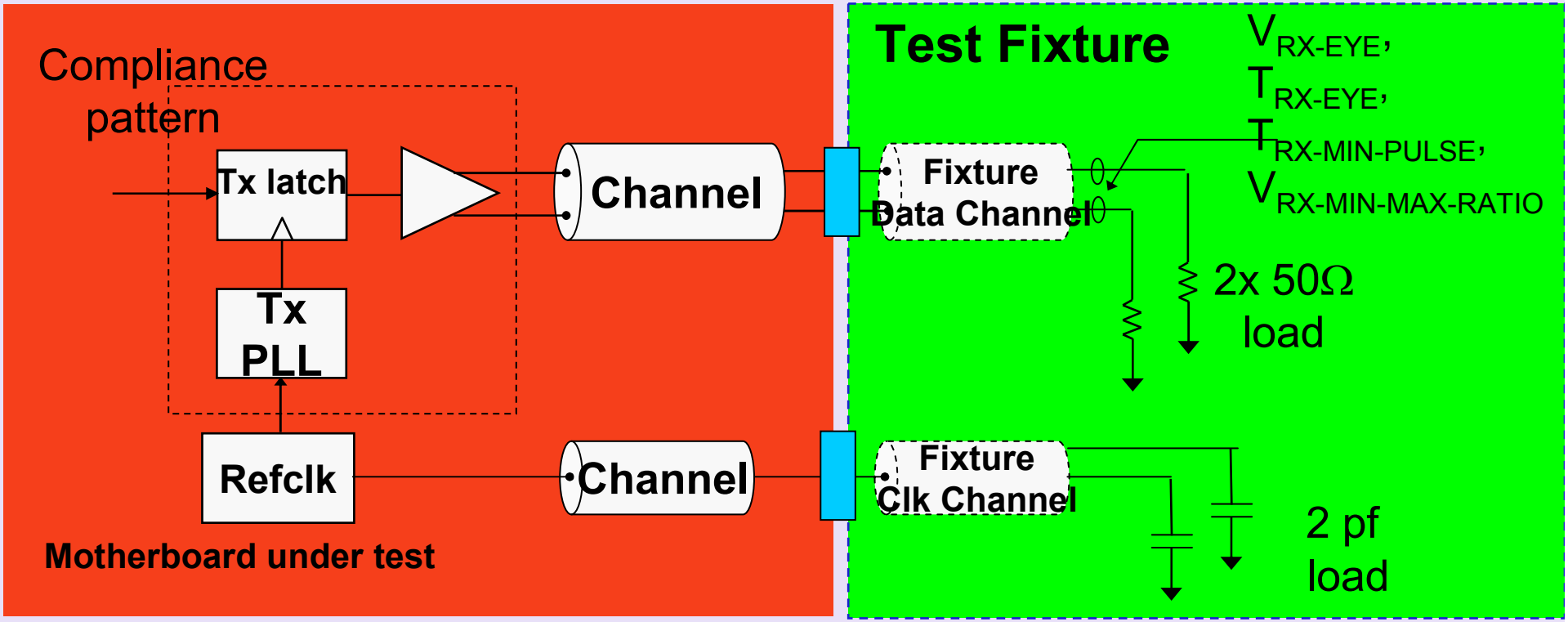
- Simulate end to connector eye diagrams



- Use CMM pattern as with real world test
- Correlate with end to end worst case pattern failures

- CEM eye specifications include ideal fixture
  - ✓ No need to de-embed if similar fixture used.

Testing Tx on MB



- Data and Refclk Output Tested At Connector
- Refclk margins same as those defined in base spec
- How do you test transmitter jitter on a motherboard with a real clock?
  - ✓ Ref clock jitter appears on transmitter up to transmitter PLL bandwidth

Dual-Port Approach

- Sample TX and Clock Simultaneously at MB Connector
- Low Pass Filter Clock with PLL Limits
  - ✓ 5 MHz 1 dB Peaking
  - ✓ 8 MHz 3 dB Peaking
  - ✓ 16 MHz 3 dB Peaking
- Add Transport Delay. Max ~ 3ns for Add-in Card.
- Use Filtered Clock To Calculate TX Jitter With Each Filtered Clock Record

Real System PLL Factored Into Measurement
Real System Delay Factored Into Measurement
Random Jitter From RefClk and TX RSS Together

Card/Slot Interop – New Req'ts

Connector / Card	x1	X4	X8	x16
x1	Required	Required	Required	Required
x4	No	Required	Required	Required
x8	No	No	Required	Required
x16	No	No	No	Required

All PCI Express Add-in Cards must be able to negotiate and operate in all smaller link widths from the full link width down to x1. **x2 and x12 link widths are optional.**

The upstream PCI Express components on a system board must be able to negotiate and operate in all smaller link widths from the full link width down to x1. **x2 and x12 link widths are optional.**

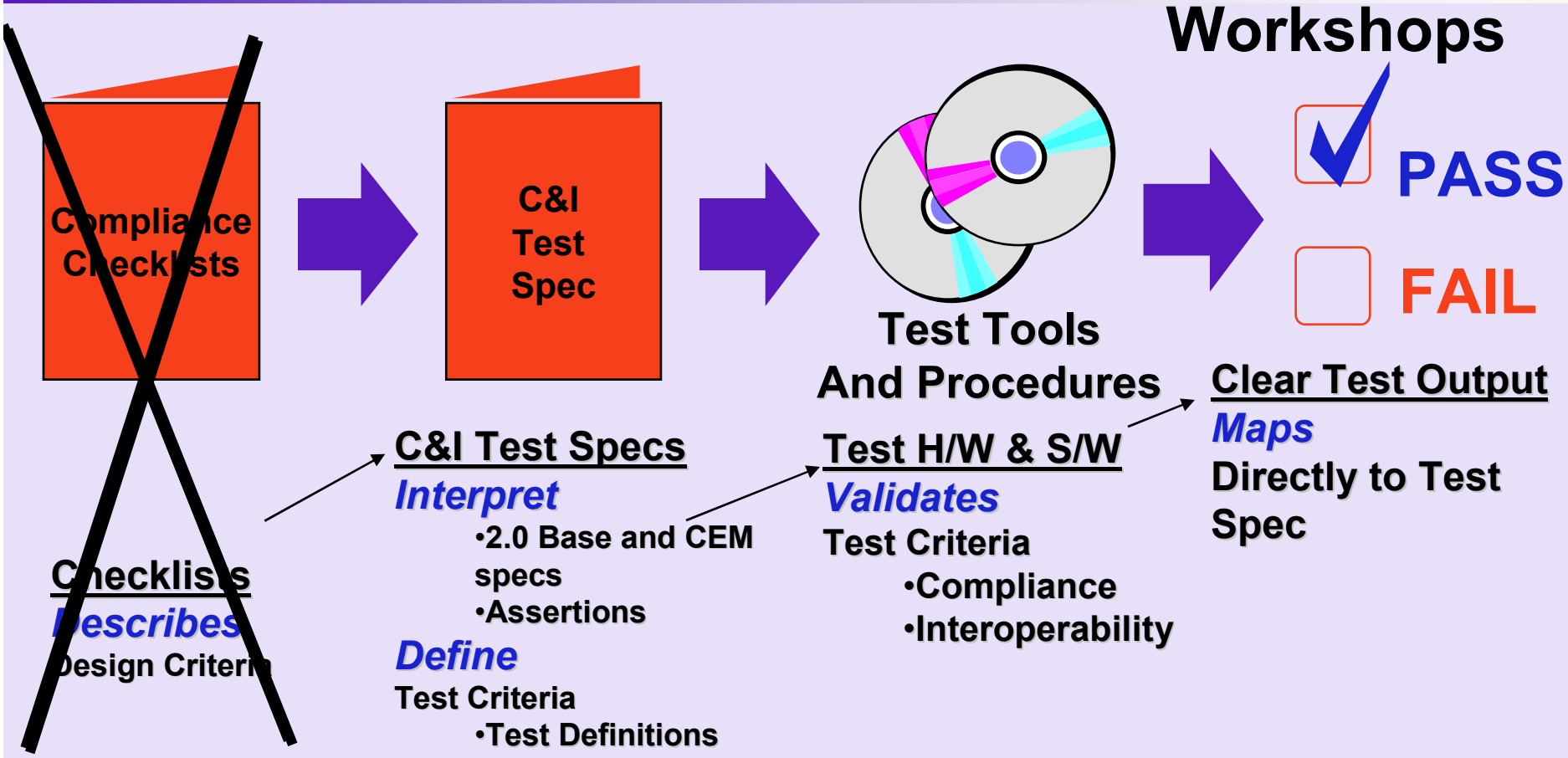
New For CEM 2.0

PCIe® 2.0 Compliance and Interoperability

Agenda

- PCIe® 2.0 Compliance Process
- PCIe Compliance Test Areas
- PCIe Electrical Tests and Tools
- PCIe Protocol Testing
- Platform BIOS Testing
- PCIe Configuration Tests
- PCIe Compliance Summary

PCIe 2.0 Compliance Process



Predictable path to design compliance

Same process as 1.x – except checklists removed

PCI Express 2.0 Integrators List Status

- March 10, 2008 Formal FYI period started
  - ✓ All test specifications have completed 60 day member review at the .9 level.
  - ✓ All 2.0 tests are completely implemented and have been run at compliance workshops.
  - ✓ All test equipment/software required for testing is available for PCI-SIG member download/purchase.
- September 2008 Compliance Workshop. Integrators list testing starts.
  - ✓ All test specifications released for members at 1.0 level.

PCIe 1.1 Compliance Test Areas

- **Physical layer**
  - ✓ Examine electrical signaling
- **Configuration Space**
  - ✓ Verify required fields and values
- **Link & Transaction layer**
  - ✓ Exercise protocol boundary conditions
  - ✓ Inject errors and check error handling
- **Platform Configuration**
  - ✓ Check BIOS handling of PCI Express devices

Available on PCISIG website

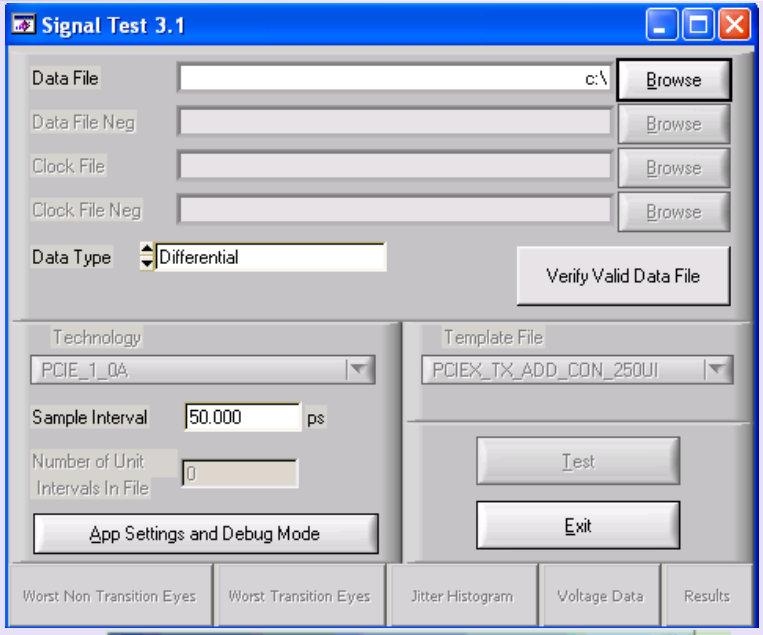
PCIe 2.0 Compliance Test Updates

- **Physical layer**
  - ✓ New CLB and CBB fixtures.
  - ✓ New Sigtest.
    - – Jitter separated into Rj and Dj.
    - – Total jitter projected @ E-12 BER
    - – Motherboard jitter and reference clock testing done with 2 port method.
  - ✓ New Clock Tool
    - – Provides clock phase jitter test to 2.0 base specification.
  - ✓ PLL Bandwidth
- **Configuration Space**
  - ✓ Updated PCIeCV for new fields and capabilities
- **Link & Transaction layer**
  - ✓ Run existing tests at 5.0 GT/s.
- **Platform Configuration**
  - ✓ PCIe 1.x PTC tests.
  - ✓ Future release modified to include simulated devices with 2.0 fields, capabilities, etc.

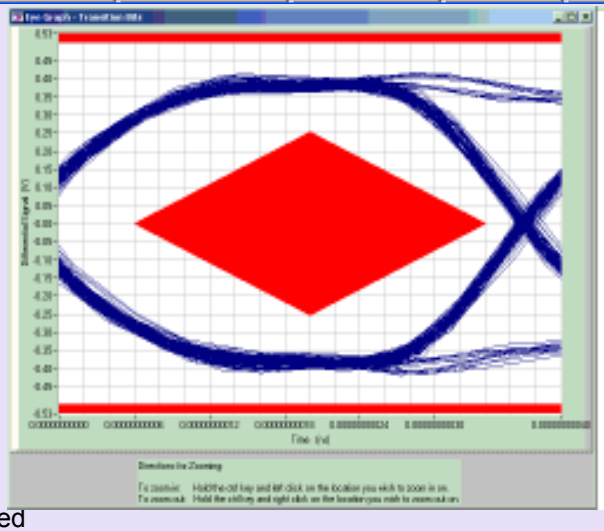
Test Specs released at .9 revision level for member review.

PCIe 2.0 Electrical Tests & Tools

- **Signal Quality Analysis H/W and S/W**
  - ✓ Rj, DJdd, and TJ @ E-12
  - ✓ Eye pattern, jitter and bit rate analysis
  - ✓ Upstream and downstream signaling
  - ✓ Electrical Compliance Base Board, CBB 2.0
  - ✓ Electrical Compliance Load Board, CLB 2.0
  - ✓ Stand-alone Windows-based eye diagram analysis S/W
  - ✓ Electrical test procedures

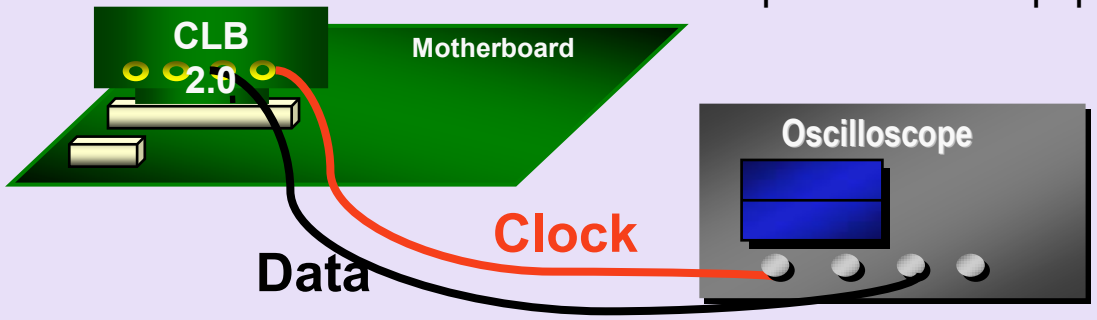


- **Jitter Analysis DLL**
  - ✓ Rj/Dj Separation
  - ✓ Dual Port Motherboard Test
  - ✓ Clock Recovery
  - ✓ Interpolation
  - ✓ Transition/non-transition eye points
  - ✓ Goal - Promote consistent solutions



PCIe 2.0 Motherboard Electrical Tools

- **Motherboard Test Procedure**
  - ✓ CLB 2.0 Standard Test Fixture connected to slot under test.
  - ✓ Lane under test and clock connected through fixture to oscilloscope.
  - ✓ Motherboard under test enters compliance mode.
    - Fixture provides features to select different compliance speeds and de-emphasis levels.
  - ✓ Data lane and reference clock sampled simultaneously
    - 25 ps or smaller sample interval. At least 1 million UI.
  - ✓ Standard Post Processing Analysis Software (Sigtest 3.1.9)
    - Supports All Common RT Scope Data Formats
  - ✓ Standard Test Procedures For Specific Test Equipment



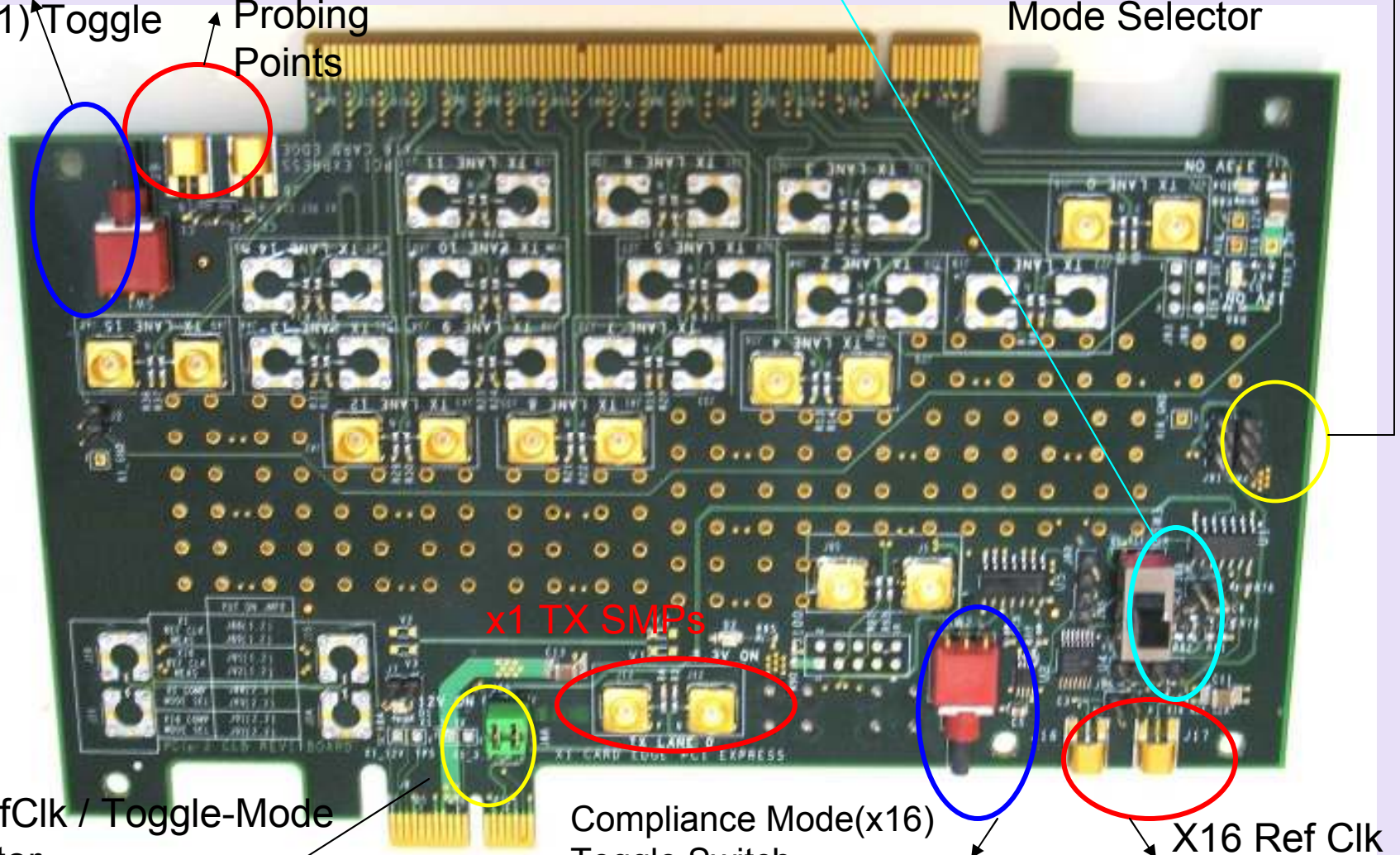
•Capture waveform on oscilloscope
•Run signal analysis software

Same Basic Motherboard TX Test Setup/Process Used For 1.1 Program

Real-Time Scope, Post Processing Software, Compliance Mode, etc . .

New 2.0 CEM Dual Port Method Test Clock and Data Simultaneously

CLB 2.0 (compliance) Features

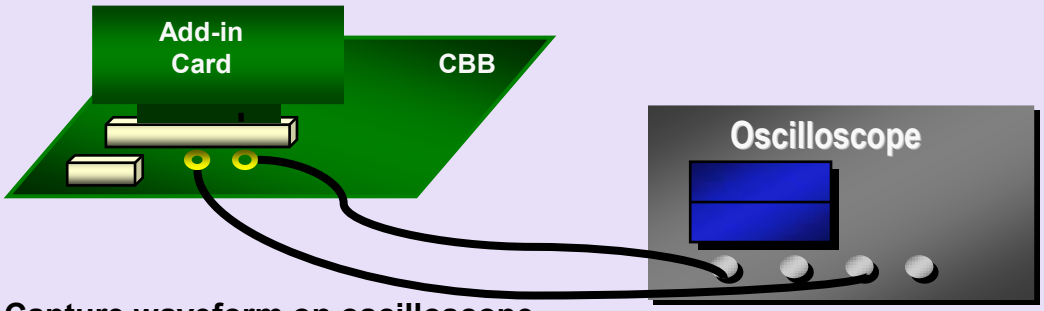


PCIe Reference Clock Jitter Testing

- **Rev 1.1 CEM specification puts new requirements on platform RefClk jitter**
- **1.1 FYI test available to analyze jitter on RefClk**
  - ✓ Clock Jitter analysis tool available through PCI-SIG.
  - ✓ Uses standard Compliance Load Board
- **2.0 FYI testing can be performed using 2.0 CLB and Clock Jitter Analysis tool.**
  - ✓ This test is not required by the 2.0 CEM spec. Reference clock jitter is measured as part of the standard dual port motherboard test for 2.0.

PCIe 2.0 Adapter Electrical Tools

- **Add-in Card Test Procedure**
  - ✓ CBB 2.0 Standard Test Fixture with add-in card to test connected.
  - ✓ Lane under test connected through fixture to oscilloscope.
  - ✓ Add-in card under test enters compliance mode.
    - Fixture provides features to select different compliance speeds and de-emphasis levels.
  - ✓ Data lane sampled.
    - 25 ps or smaller sample interval. At least 1 million UI.
  - ✓ Standard Post Processing Analysis Software (Sigtest 3.1.9)
    - Supports all common RT Scope data formats
  - ✓ Standard Test Procedures for specific test equipment



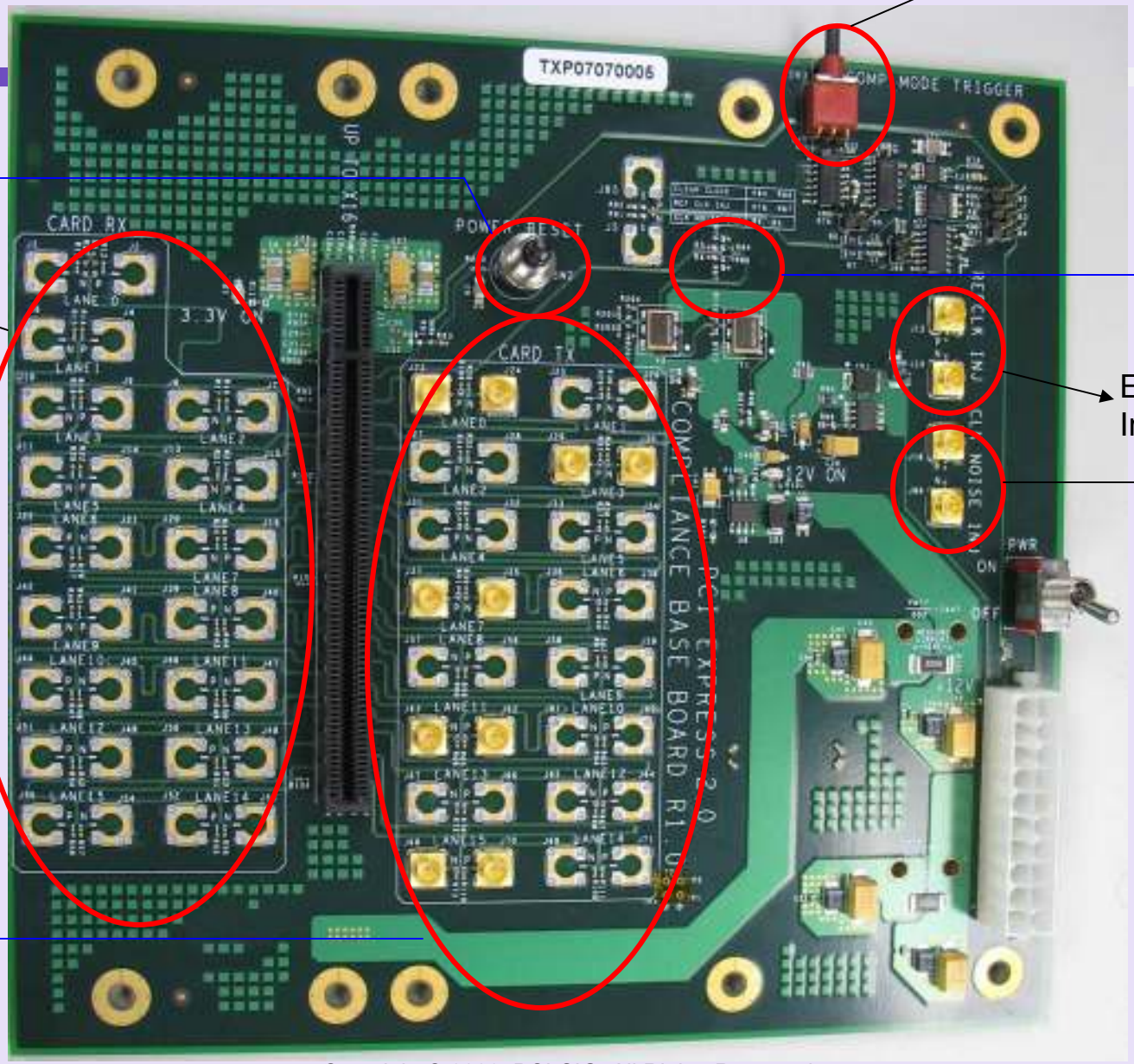
•Capture waveform on oscilloscope
•Run signal analysis software

Revised CBB for PCIe 1.1

Same Basic AIC TX Test Setup/Process Used For 1.1 Testing

RT Scope, Post Processing Software, Compliance Mode, etc . .

CBB 2.0 Features



CBB and CLB 2.0 Versions Can be Used for 2.5 GT/s Testing

Clean Clock 1.1 Add-in Card Testing

- 1.1 Compliance base board built to have a RefClk with very little jitter
- Provides accurate picture of device-under-test jitter
- 2.0 CBB offers lower jitter clock and continues 1.1 clean clock add-in card test model.
- For test fixture availability, visit www.pcisig.com

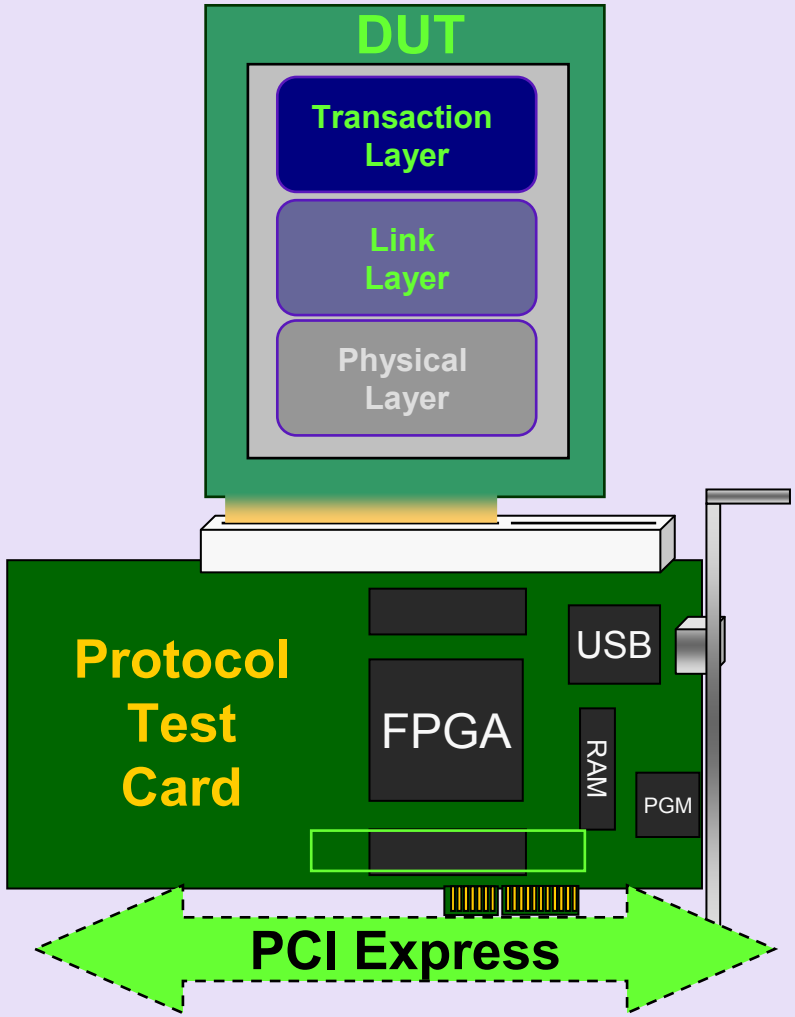
PLL Bandwidth Testing

- Required test for 2.0 integrators list
- Test outline
  - ✓ Sinusoidal phase jitter is added to reference clock from 0 to 25 Mhz in small frequency increments.
    - Reference clock jitter is calibrated to 43.6 ps under 2.0 spec filter.
  - ✓ Transmitter jitter is measured at each point.
  - ✓ 3 dB point and peaking in transmitter response are determined from data.
    - 3 dB point must be between 8 and 16 Mhz with peaking < 3 dB peaking
    - 3 dB point must be between 5 and 16 Mhz with peaking < 1 dB.
  - ✓ Testing is repeated with reference clock jitter calibrated to 43.6/2 ps.
- 3 sets of equipment used at compliance workshops. One result must pass.
  - ✓ Spectrum analyzer.
  - ✓ Synthesys Research clock recovery module.
  - ✓ Agilent DCA-J clock recovery module.
  - ✓ Detailed procedures will be available on website.

Additional 2.0 Electrical Tests Under Consideration

- **PCB Impedance**
  - ✓ Verify Tx and Rx differential impedance are within CEM limits
- **Receiver Packet Error Rate**
  - ✓ Functional testing with reference Add-in cards and Motherboards using loopback

PCIe Protocol Testing



- **Test Control software running on platform or Device Under Test (DUT) initiates test traffic**
- **PTC monitors and acts on that traffic**
  - ✓ Checking protocol
  - ✓ Injecting errors

PCI Express 2.0 PTCs

- Two selected. Both will be run at workshops and add-in card must pass with at least one
  - ✓ Agilent
  - ✓ Lecroy

PCIe Link / Transaction Compliance Tests

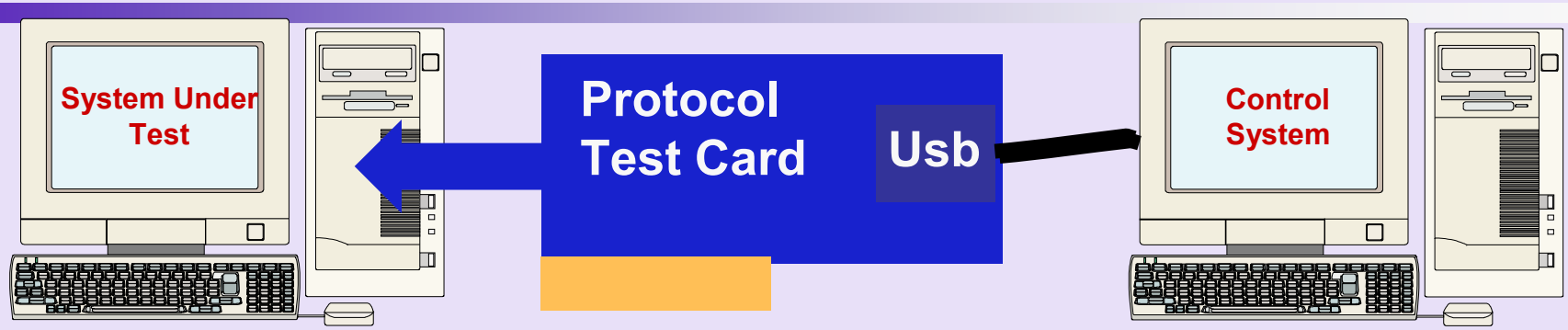
- **Described in Link Layer Test Spec and Transaction Layer Test Spec**
- **Tests**
  - ✓ Reserved fields – Device ignores them
  - ✓ NAK response – Device will resend after receiving NAK
  - ✓ Replay Timers – Device will resend packet if no response
  - ✓ Replay Count - Device will resend multiple times when no response
  - ✓ Link Retrain - Device will retrain if continued no response
  - ✓ Replay TLP order – Device replays TLPs in proper order
  - ✓ Bad CRC - Device detects, drops, and logs (DLLPs & TLPs)
  - ✓ Undefined packet – Device ignores
  - ✓ Bad Sequence Number – Device detects, drops, and logs
  - ✓ Duplicate TLP - Device returns data once
  - ✓ Request Completion – Issue UR for config requests not supported

Link/Transaction tests must also be run at 5.0 GT/s for 5.0 GT/s Integrators List.

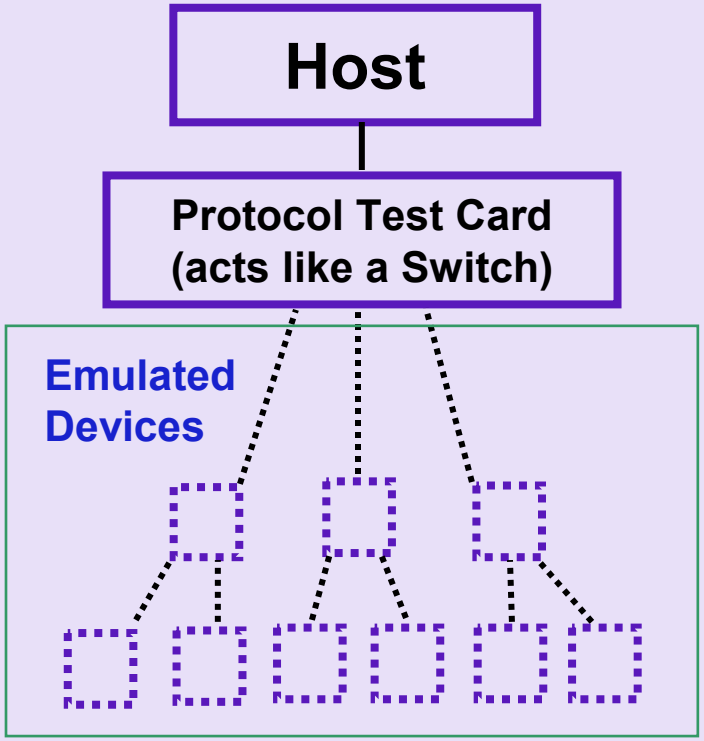
New Test – Link Training with Reserved Bits Set

- Reserved Bit Link Training Test
  - ✓ Address real-world interoperability between different generation devices
  - ✓ Set reserved bits in training sets
  - ✓ Confirm that link training completes, ignoring reserved fields
  - ✓ Test spec is currently under development
  - ✓ Required for 2.0 integrators list.
  - ✓ FYI for 1.1 integrators list.
- Introduced as FYI at August 2007 Compliance Workshop

Platform BIOS Testing



- Protocol Test Card Can Represent Any Hierarchical Multi-Device/Bridge Topology

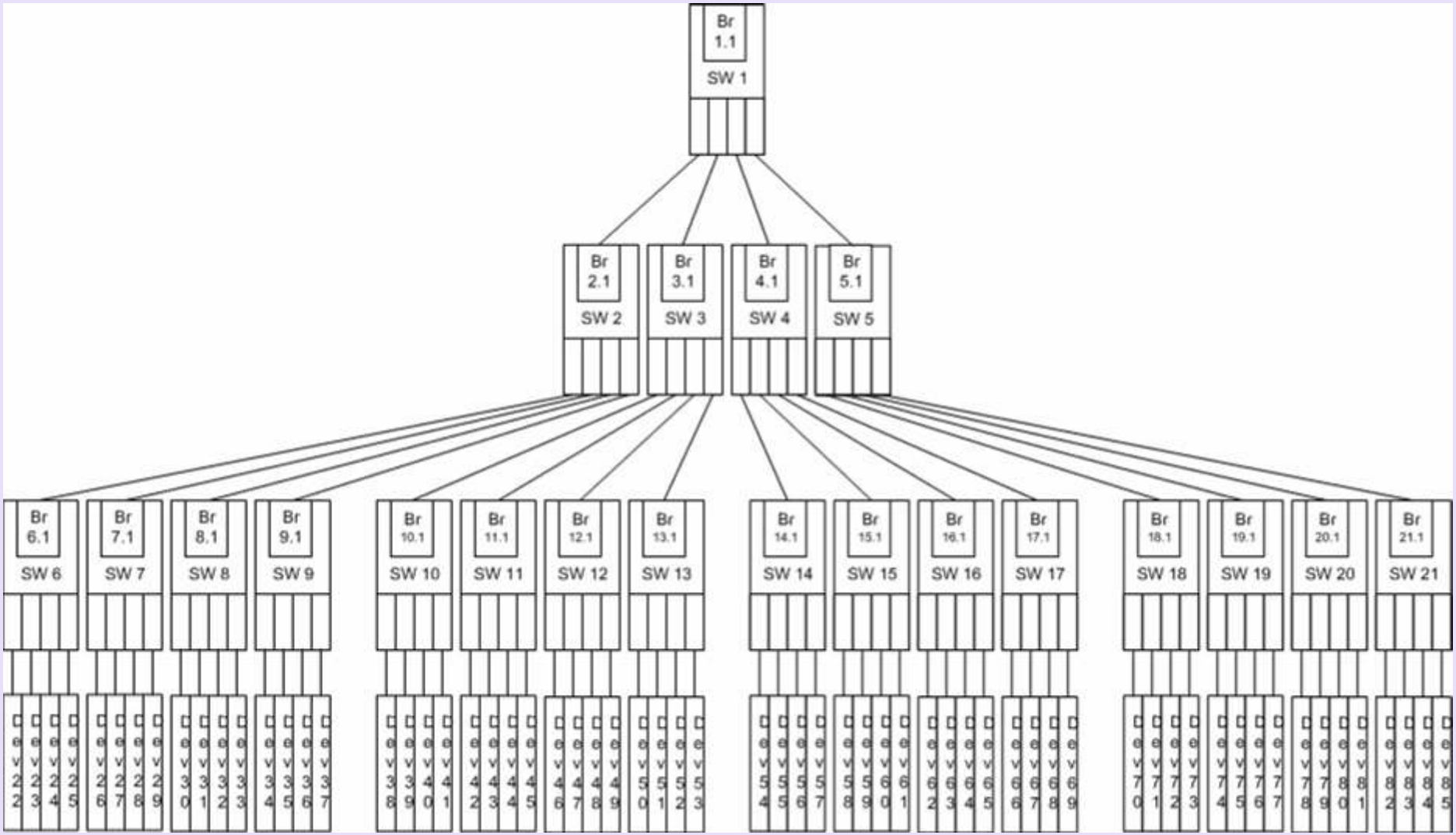


- Device Decodes All Type 0 and Type 1 Configuration Cycles

PCIe BIOS Test

- Multiple Functions per device
- Different BAR combinations
  - ✓ I/O, Mem, 64bit
  - ✓ Various size requests
  - ✓ Prefetchable, non-prefetchable
- Bridges With Resource Requests
- ASPM Configurations
- Option ROMs
  - ✓ Varying sizes
  - ✓ Different for each device function
  - ✓ Shrinkable, removable
- Complex Multiple Switch and Bridge Topologies

Worst Case Topology



PCIe 2.0 Bios/Firmware Test Updates

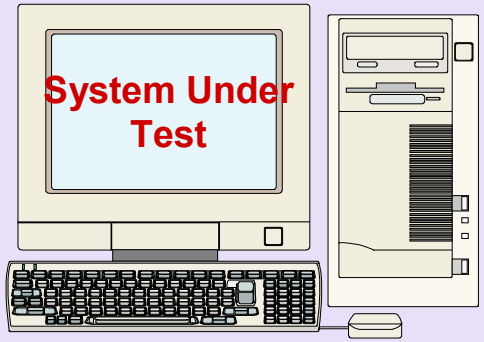
- Use existing PCIe 1.x Agilent PTC and tests (for now)
- Minor updates to existing test cases to add simulated devices that have 2.0 registers, capabilities, etc.
  - ✓ Ensure that Bios/Firmware doesn't choke on new fields, etc.
- May update to run at 5.0 GT/s for future 2.0 IL testing

PCIe Configuration Test Areas

- Registers and Capabilities
  - ✓ Default Values
  - ✓ Characteristics
  - ✓ Required registers and capabilities
  - ✓ Covered Areas
    - 1.0a PCI Express Spec
    - 1.1 PCI Express Spec
    - PCI 2.3/3.0 Spec
    - PCI Express Bridge Spec
    - PCI PM Spec (1.1, 1.2)
- Functional
  - ✓ Configuration Stress
- System
  - ✓ Accurate Slot Reporting
  - ✓ Basic Hot Plug Event Reporting

Configuration Tests – Diagram

System Test



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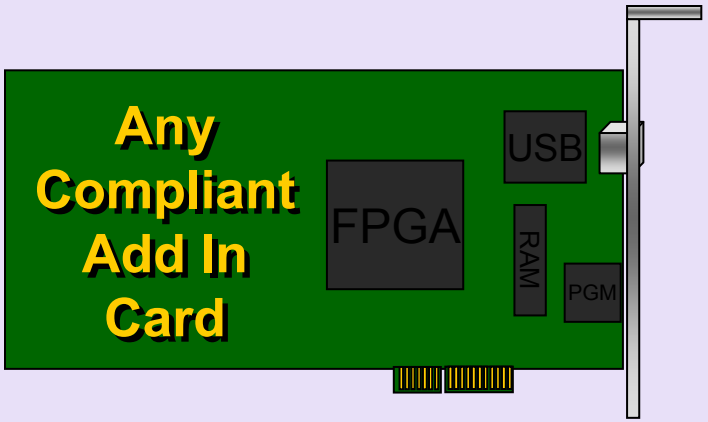
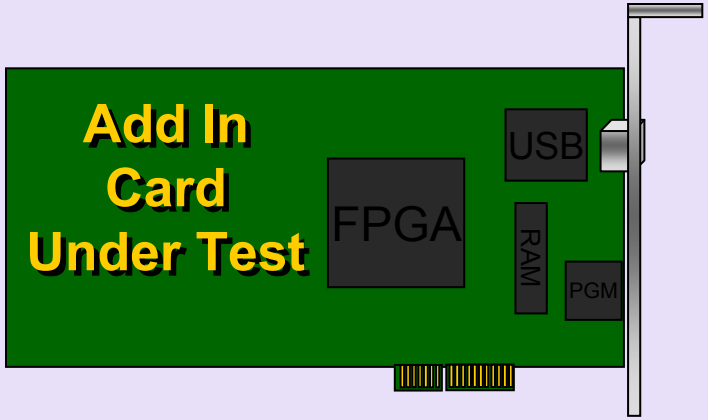


Add in Card Test



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PCIe 2.0 Configuration Test Additions

- Updates to PCIeCV
  - ✓ Cover new registers, fields, capabilities.
  - ✓ Standard tests for default values, field characteristics, etc.
  - ✓ Test options:
    - 2.0 spec only (for 2.0 compliance)
    - 1.1 or 2.0 spec (1.1 compliance or ECNs included in 2.0 spec)
- New tests
  - ✓ Link Width
  - ✓ Link Speed
- All PCIECV tests must run at 2.5 GT/s and 5.0 GT/s for devices applying for the 5.0 GT/s 2.0 Integrators List.
- 1.4.6 Source available for member download on PCI-SIG website.

PCIECV – 2.0 Link Speed Test

- Gold System
  - ✓ 5.0 GT/s capable, 2.0 spec compliant system used for testing add-in cards.
- Set target link speed to limit maximum link speed and then write retrain link bit. Disable autonomous width or bandwidth changes on both components.
  - ✓ Upstream 2.5 Downstream 5.0 Result 2.5
  - ✓ Upstream 5.0 Downstream 5.0 Result 5.0
- Test criteria
  - ✓ Autonomous Bandwidth Status must never be set
  - ✓ Config registers must never be reset
  - ✓ Actual link speed matches expected link speed

PCIECV – 2.0 Link Width Test

- CEM 2.0 spec requires x4 and x8 to be supported as intermediate widths.
- Specified in 2.0 Config test spec
- Testing only static link width support
- Use low cost mechanical adaptors to do all testing with standard x16 slot.
- Insert in riser card, and check that the link comes up in the correct link width

Connector / Card	x1	X4	X8	x16
x1	Required	Required	Required	Required
x4	No	Required	Required	Required
x8	No	No	Required	Required
x16	No	No	No	Required

FYI PCIe 2.0 Compliance Test Summary

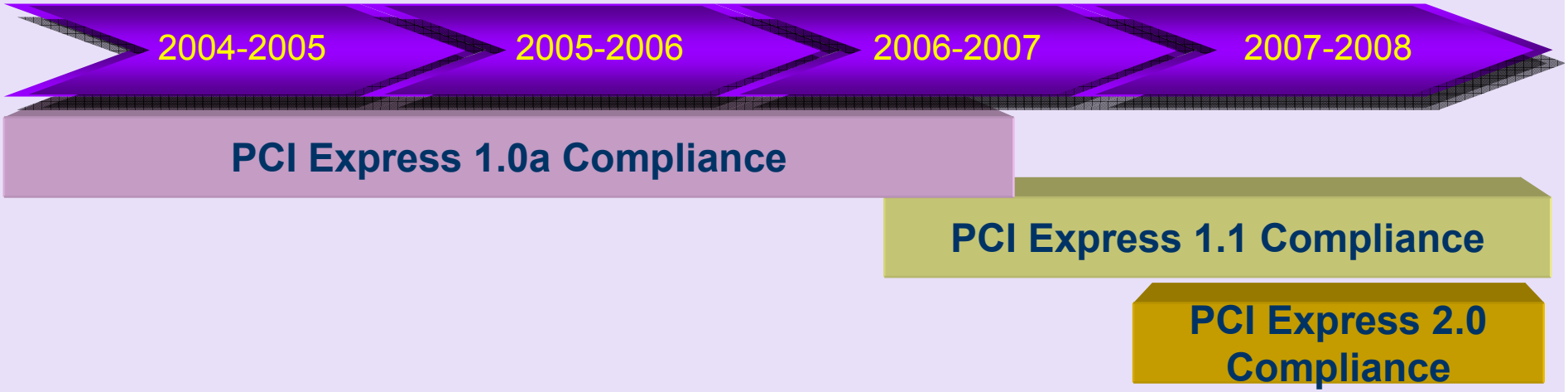
- The following is available on www.pcisig.com:
  - ✓ Link/Transaction
    - Agilent and Lecroy 2.0 PTC ordering information.
    - Agilent and Lecroy test procedures.
    - Agilent and Lecroy test software
  - ✓ Electrical
    - CBB 2.0 / CLB 2.0 availability and ordering information
    - Sigtest 3.1.9
    - Procedures using RT Scope
    - PLL bandwidth test procedures
  - ✓ Config
    - PCIeCV 1.4.6

PCIe 2.0 Compliance Summary

Test	Device Type		
	Endpoint	Root	Switch / Bridge
Physical Layer (Electrical) - Sigtest 3.1.9 - CBB / CLB 2.0 - PCI Express PHY Test Spec 2.0 - Test procedures for RT scopes	**Required**	**Required**	**Required**
PLL BW Testing	**Required**		**Required**
Configuration Space - PCIECV 1.4.6 - PCI Express Configuration Test Spec 2.0 - PCI Express Configuration Test Procedure 2.0	**Required**		**Required**
Link and Transaction Layer - 2.0 PTC - PTC test software - PCI Express Link Layer Test Spec 2.0 - PCI Express Transaction Layer Test Spec 2.0 - PCI Express Link/Transaction Test Procedures 2.0	**Required**		**Required**
Clock Jitter - ClockTool version 1.3		**FYI only**	
Platform BIOS Test - 1.1 PTC - PCI Express Platform BIOS Test Software v0.90		**Required**	

PCIe Compliance Summary

- **Final PCI Express 2.0 specifications available now**
  - ✓ Your compatible architecture for new designs!
- **PCI Express 1.1 compliance collateral and integrator's list available**
- **PCI Express 2.0 integrator's list start in September 2008.**
- **PCI Express 2.0 testing collateral available on PCISIG website**
- **For all PCI Express material, visit www.pcisig.com**
  - ✓ **Final (rev 1.0) PCIe 2.0 test specifications for electrical, config, link, transaction available.**



Thank you for attending the PCIe Technology Seminar

For more information please go to www.pcisig.com