
PCI
SIG®

Implementation of PCIe™ in a Gigabit Ethernet Chip

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Integrated MAC-PHY controller for PCIe

- Agere Systems has developed an Integrated MAC-PHY controller for PCI Express®.
  - ✓ ET1310 is a single chip network Interface solution for Gigabit Ethernet.
  - ✓ The device combines a gigabit Ethernet host controller and MAC with Agere Gigabit Ethernet TruePHY™ technology and a high-performance, fully compliant PCI Express 1.0a host system interface

Implementing PCIe in ET1310

- Implementation and verification of fully compliant PCI Express 1.0a host system Interface

  - ✓ Complex Verification Platform
  - ✓ Verification Challenges
  - ✓ Successful Verification

Verification Challenges

- Functional verification is becoming a major bottleneck in the chip design cycle.
- Ever increasing complexities of the IC
- Increasing use of reusable IP blocks
- Each new system IC and IP Core must be verified
- Eliminate discrepancies between the design and its specifications
- Ensure that the manufactured device functions properly.

Verification of PCIe in Gigabit Ethernet Controller

- We have used an IP core for the PCI Express in our Integrated MAC-PHY controller
- How do we verify this is fully PCI Express 1.0a compliant?
- Create a Test Environment for Directed Random Verification

Directed Random Verification

The advantages of directed random verification method are:

- Evenly covers a huge verification space with limit effort
- Generates combinations that test writers may not have considered
- Insure the testing of specific area of interests

Directed Random Verification Steps

- Extract features from design specification
- Identify possible causes of errors (interface, protocol, data)
- Identify corner cases from implementation specification
- Group like features and relevant errors into testbases
- Identify configurations for each testbase
- Identify verification components (Drivers, Monitors, etc) for testbase

Directed Random Verification Steps (cont)

- Code verification components
- Write scenarios (lightly constrained typical test sequences)
- Construct a scoreboard (calculate, store and compares expected data)
- Develop functional coverage metrics and temporal check
- Run scenarios with multiple different seeds and identify holes in functional coverage reports
- Write directed (highly constrained) testcases to cover holes

Verification Technologies and Tools

- **Dynamic Simulation**
  - ✓ Dynamic simulation at both RTL and gate-level was performed.

- **Testbench Automation**
  - ✓ To support directed random verification we used testbench automation to generate the directed random stimulus to drive the Design Under Test.

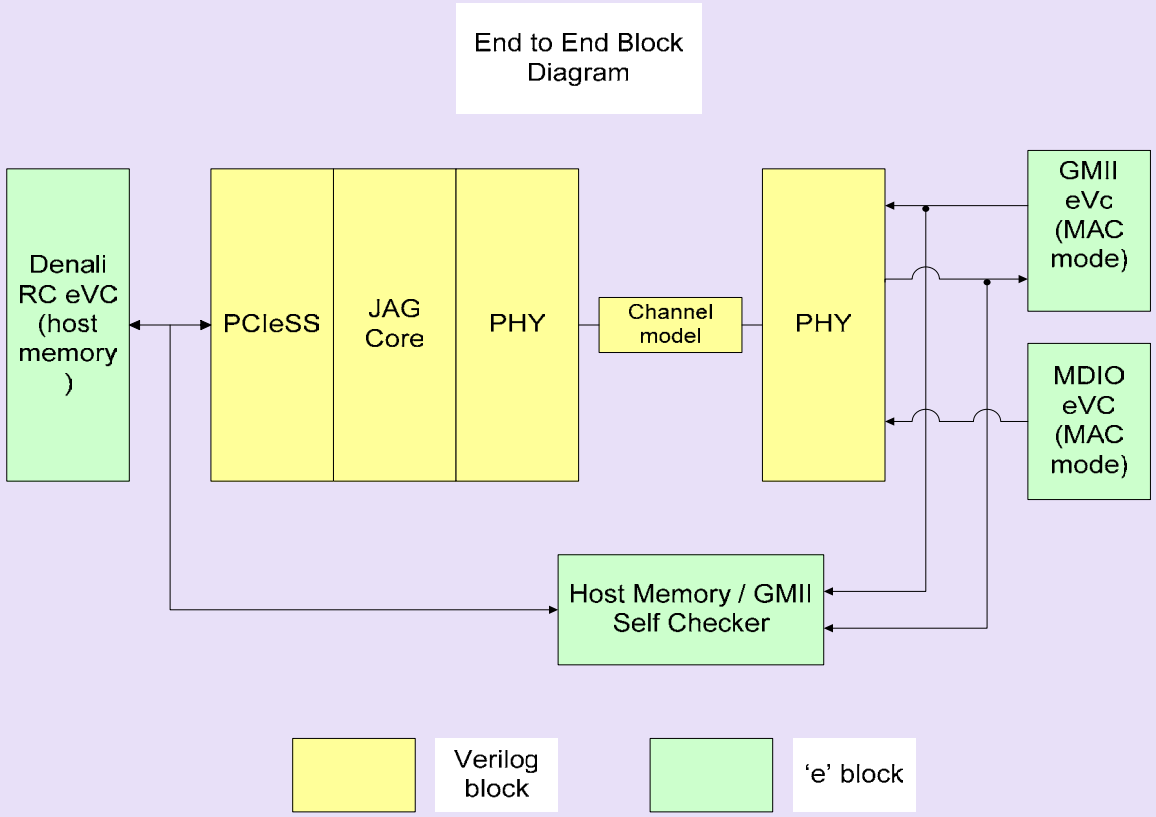
Functional & Code Coverage

- Functional coverage is used to ensure that the vital functionality of the Design Under Test has been exercised and verified by the directed random seed test cases executed.

- Code coverage tool was used to provide an assessment of the quality of the test suites. It also identifies the untested areas of the design.

Verification environment

- Agere Gigabit Ethernet Controller verification environment



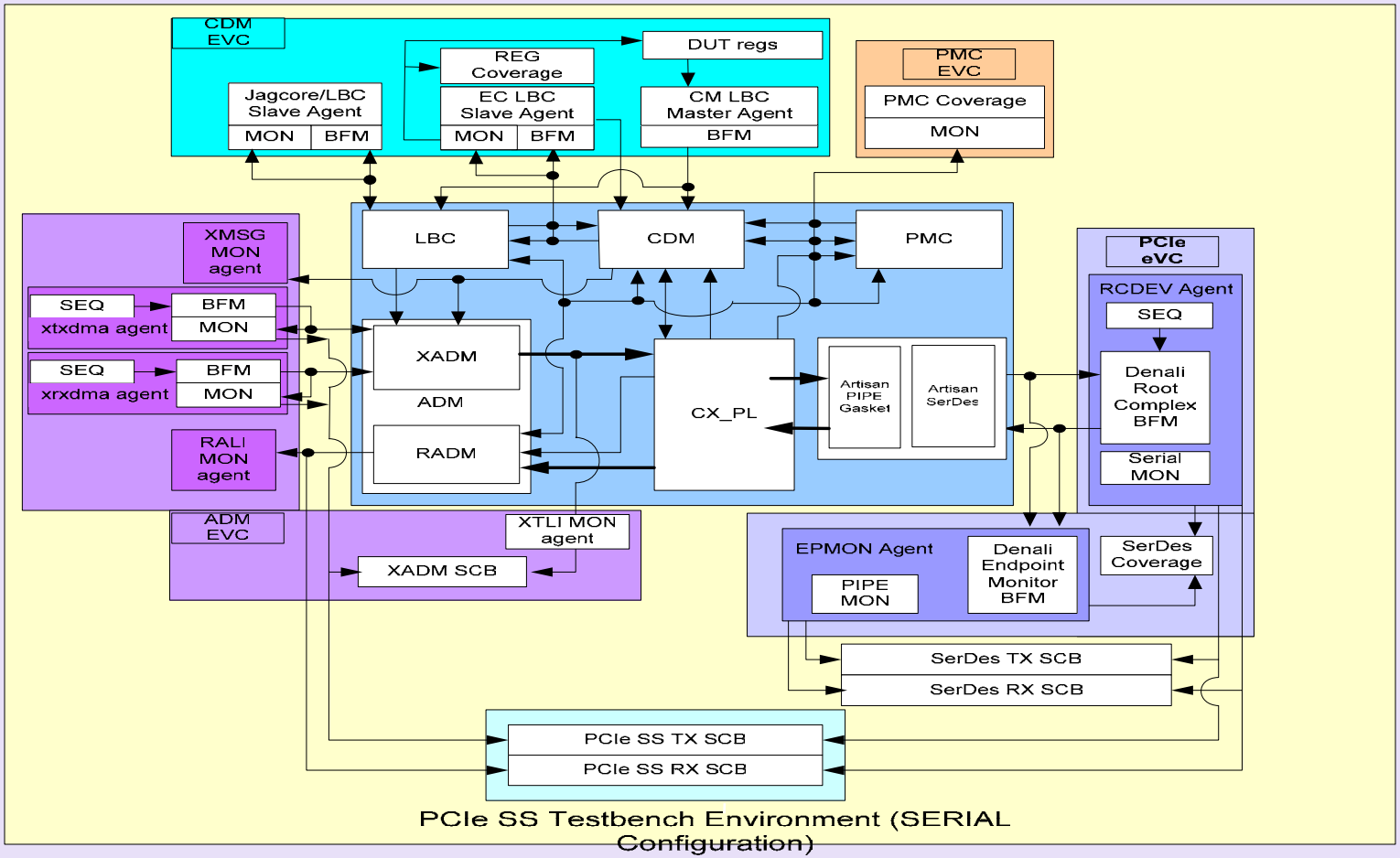
PCIe Verification

- Since PCI Express is a complex protocol, a separate test environment was created to verify the PCI Express.
- The PCIe testbench environment is a highly configurable testbench environment used for the functional verification of the PCI Express Subsystem.
- Besides the digital logic the PCIe Subsystem also support a SERDES for PCIe front-end for serial transmissions on the PCI Express link.

PCIe Verification (cont)

- To support the dual configurations of PIPE and SERIAL, majority of the top level PCIe verification environment remains unchanged.
- The PCI Express e Verification Component support a configuration interface that allows it to hook up to and drive the SERDES Serial interface as well as the Port Logic PIPE interface.

PCI Express Verification Environment (Serial)

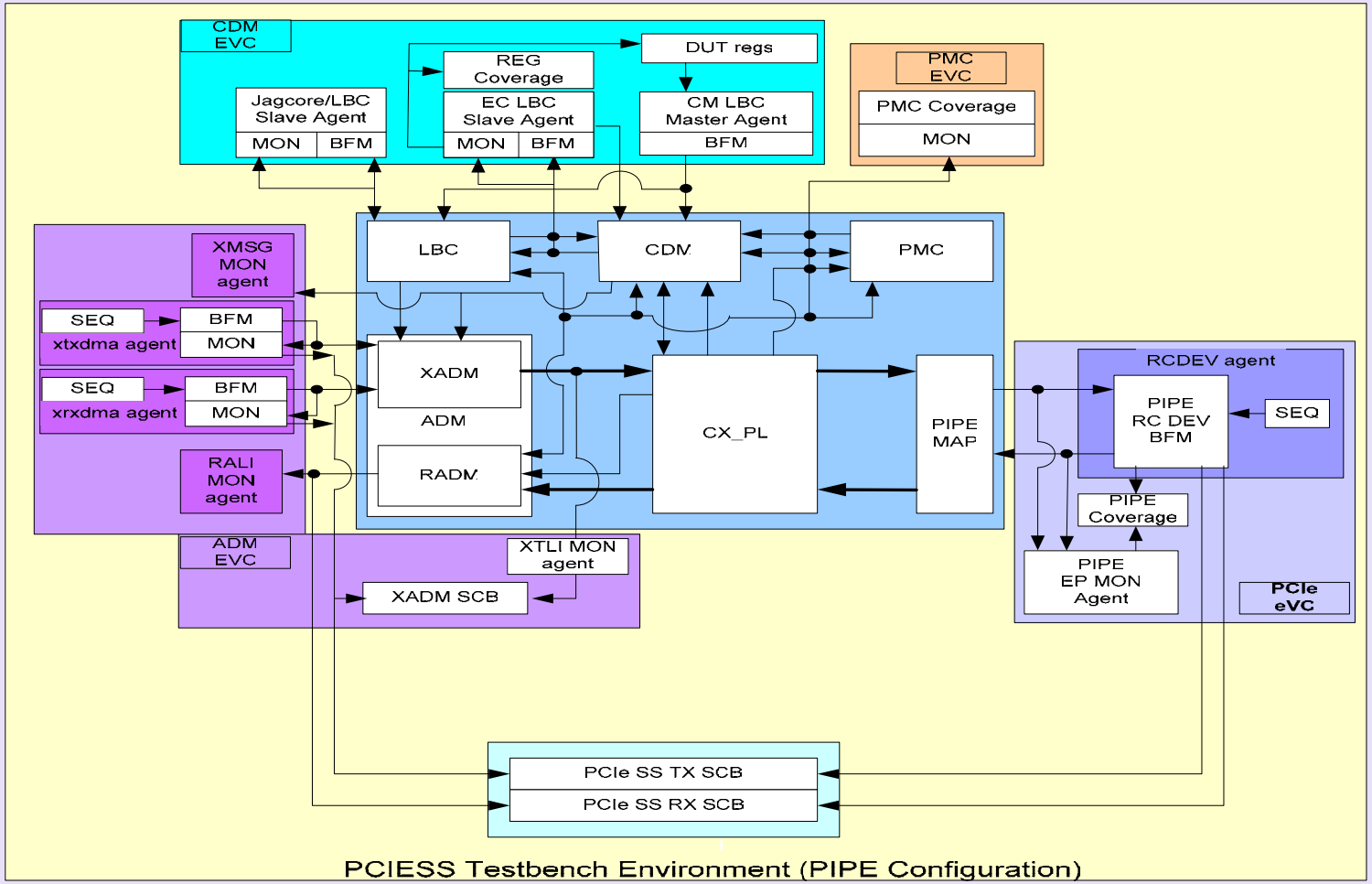


PCIe SS Testbench Environment (SERIAL Configuration)

PCI Express Verification Environment (Serial) (cont)

- Includes the SERDES block as part of the Design Under Test.
- PCIe eVC gets configured to hook up to the SERDES Serial interface.
- SERDES Serial monitor and functional coverage.
- Serial Link agent functions as a source for the SERDES Block Scoreboards.

PCI Express Verification Environment (PIPE)

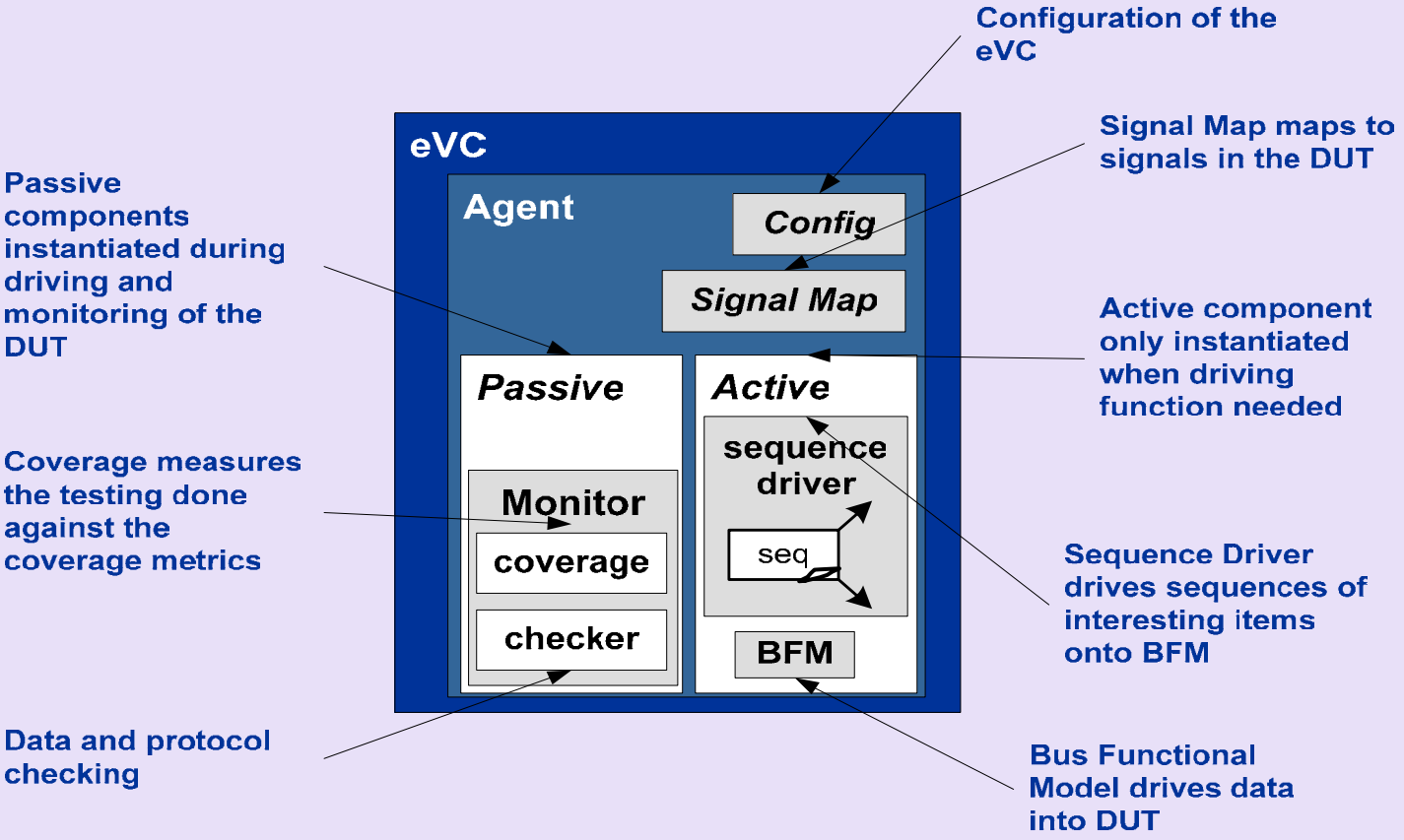


PCIESS Testbench Environment (PIPE Configuration)

PCI Express Verification Environment (PIPE) (cont)

- Excludes the SERDES block from the Design Under Test.
- PCIe eVC hooks up to the MAC layer PIPE gasket on the Port Logic RTL.
- SERDES scoreboards are also excluded from the testbench environment.

Verification Component Requirements



Reference : Cadence Design System ***e*** Reuse Methodology *(**e**RM)*

PCI Express Verification Component

- The PCIe eVC is developed to speed up testbench development for any PCI Express based application designs (endpoints, switches, and root complex devices).
- The PCIe eVC perform as a transceiver: a requestor and completer as defined by the PCI Express Base Specification 1.0a.
- The PCIe eVC is built to support a industry standard interface, PCI Express 1.0a

PCI Express Verification Component

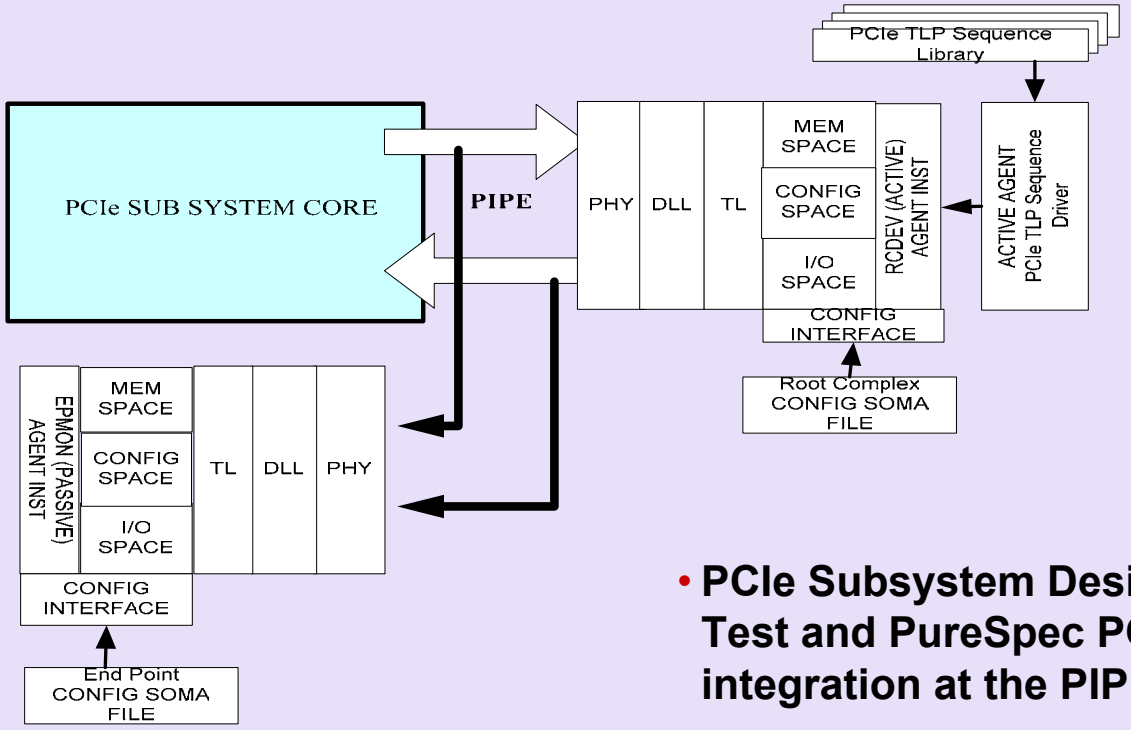
- The PCIe Verification Component features:
  - ✓ Support active device mode operations for Root Complex (RC), Switch (SW), Endpoint (EP) and Bridge (BR) PCI Express ports.
  - ✓ Support passive monitor mode operations for Root Complex, Switch, Endpoint and Bridge PCI Express ports.
  - ✓ Support configuration of multiple agent instances to support a complex verification environment.

PCI Express Verification Component (cont)

- ✓ Support Transaction Layer PCI Express transaction sequence generator.
- ✓ Each agent instance supports a user programmable and configurable PCI Express Memory and Configuration space.
- ✓ Each agent provides a back door access to the PCIe memory and configuration space for dynamic load and access.
- ✓ Support callbacks event hook methods at the Physical, Data and Transaction layers of the Denali PCIe model.
- ✓ Support configurable operation at the Phy serial, 10bit Parallel and the 16bit data PIPE interfaces.

Topology of the PCIe eVC

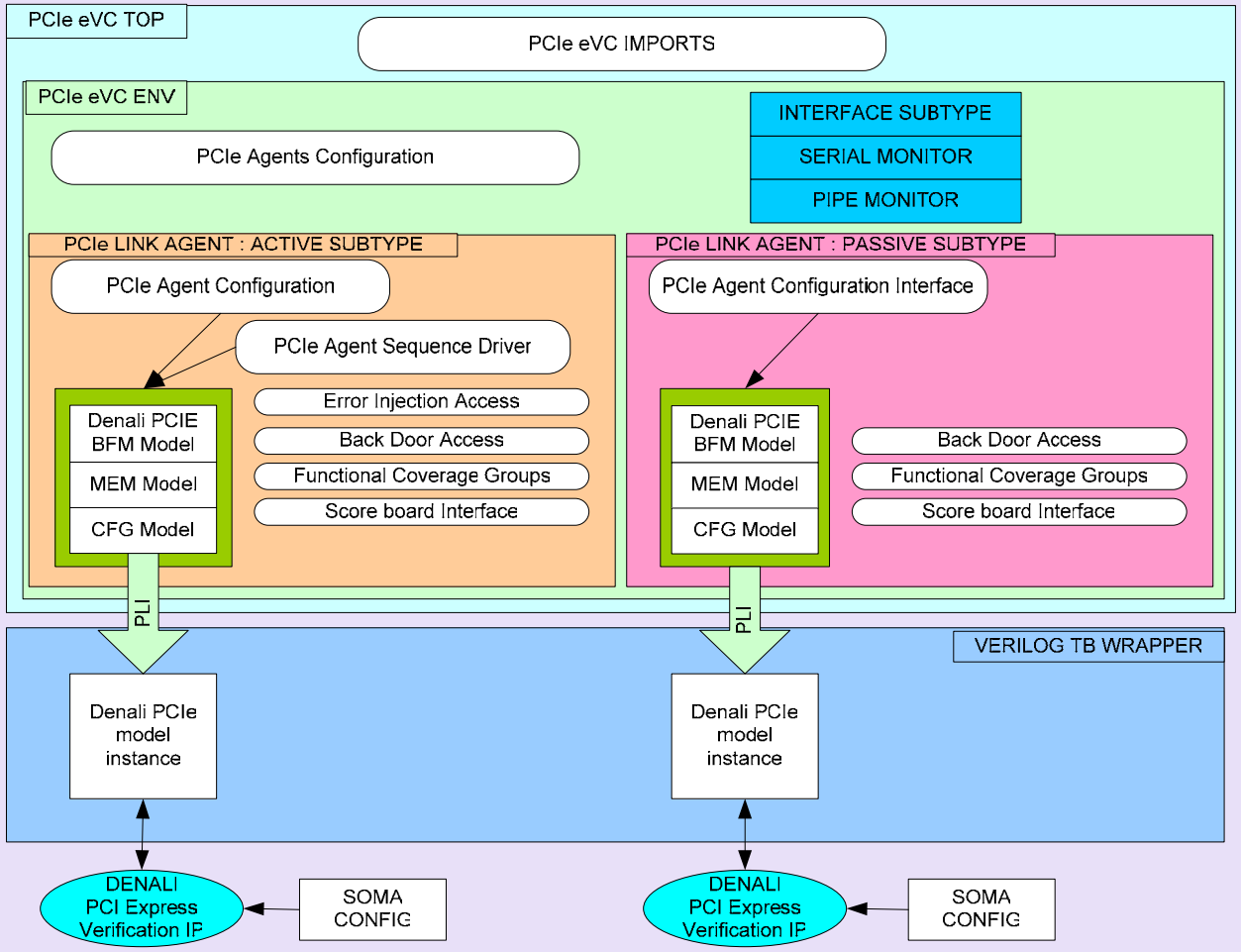
- Topology of the PCI Express eVCs



- **PCIe Subsystem Design Under Test and PureSpec PCIe *e*VC integration at the PIPE Interface .**
- **I/O space is shown for feature illustration only.**

PCIe eVC Architecture

PCIe eVC Architecture overview



PCIe eVC Architecture (cont)

- The PCIe eVC is highly configurable and versatile.
  - ✓ The eVC can be configured and hooked into any verification environment to verify a Root Complex, Switch, End Point or Bridge applications
- The PCIe eVC supports a layered architecture.
  - ✓ The first and outer most layer imports and loads all the eVC source code files. The second layer provides a configuration interface to instantiate multiple active device mode (PCIe requester and completer) or passive monitor mode (PCIe protocol checker only) components.

PCIe eVC Architecture (cont)

- The PCIe link agents configured as active agents have a transaction sequencer component enabled.
  - ✓ This enables the user to get the active agent to perform as a requester.

- The components of the eVC :
  - ✓ PCIe Link Agent
  - ✓ PCIe Sequence Driver
  - ✓ Serial/PIPE Interface Monitor

PCIe eVC link agent

- The PCIe link agent encapsulates the Denali PCIe verification IP.
  - ✓ The Denali IP model is a compiled C model. The PCIe eVC integrates this model into Specman™ via the PCIe eVC link agent wrapper.
- The link agent wrapper provides the following interfaces:
  - ✓ PCI Express Link interface
  - ✓ PCIe Configuration, Memory and I/O space access interface
  - ✓ SOMA(Specification of Model Architecture) file interface
  - ✓ Back door access interface

PCIe eVC link agent (cont)

- To extract the trigger or callback events that occur across the 3 PCI Express layers (PL,DLL,TL).
- To extract the data packets (PLP, DLP, TLP) from the respective PCI Express layers.
- Enable error injection, functional coverage and score-boarding.
- Check PCI Express protocol compliance across all transmit and receive datapaths.

PCIe eVC Sequence Driver

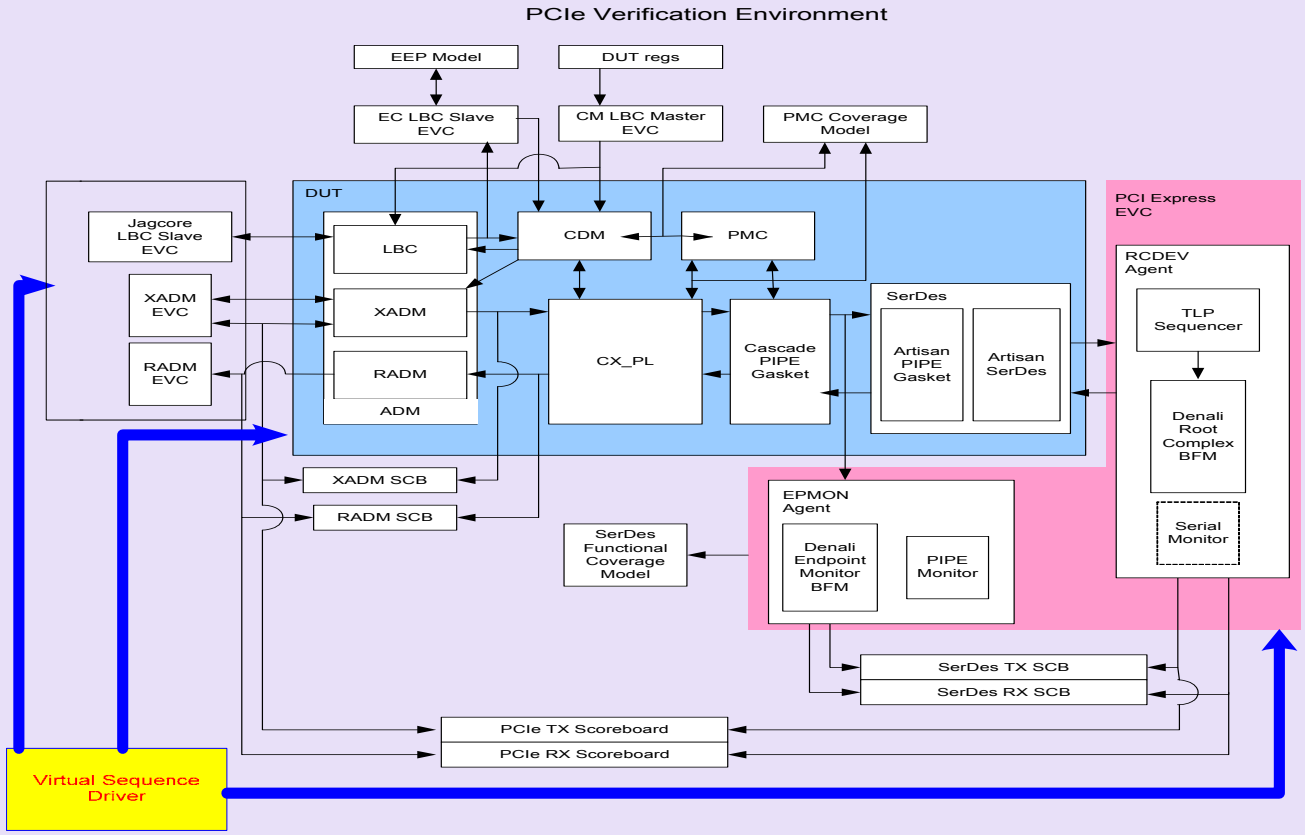
- The PCIe eVC provides a complete transaction layer sequence driver and a sequence library.
- A robust interface to the test writer to create transaction layer packet (TLP) scenarios.
- All types of TLP generation is supported.

Main Features of the PCIe agent

- Can be configured to operate as different PCI Express Devices each having a unique instance of the PCIe agent.
- Provide instantiation and access to the Denali PCIe Protocol C Model and Memory model.
- Provide back door access to the configuration, memory and I/O spaces of the encapsulated Denali C model.
- Provide support callback events to snoop the PCIe transactions flowing through the PCIe agent.
- Provide functional coverage for the transaction level traffic transmitted and received by each PCIe agent.
- Provide support for Sequence hook up.

Virtual Sequence Driver

- Virtual sequences are used to synchronize and dispatch the BFM sequences to BFM drivers.

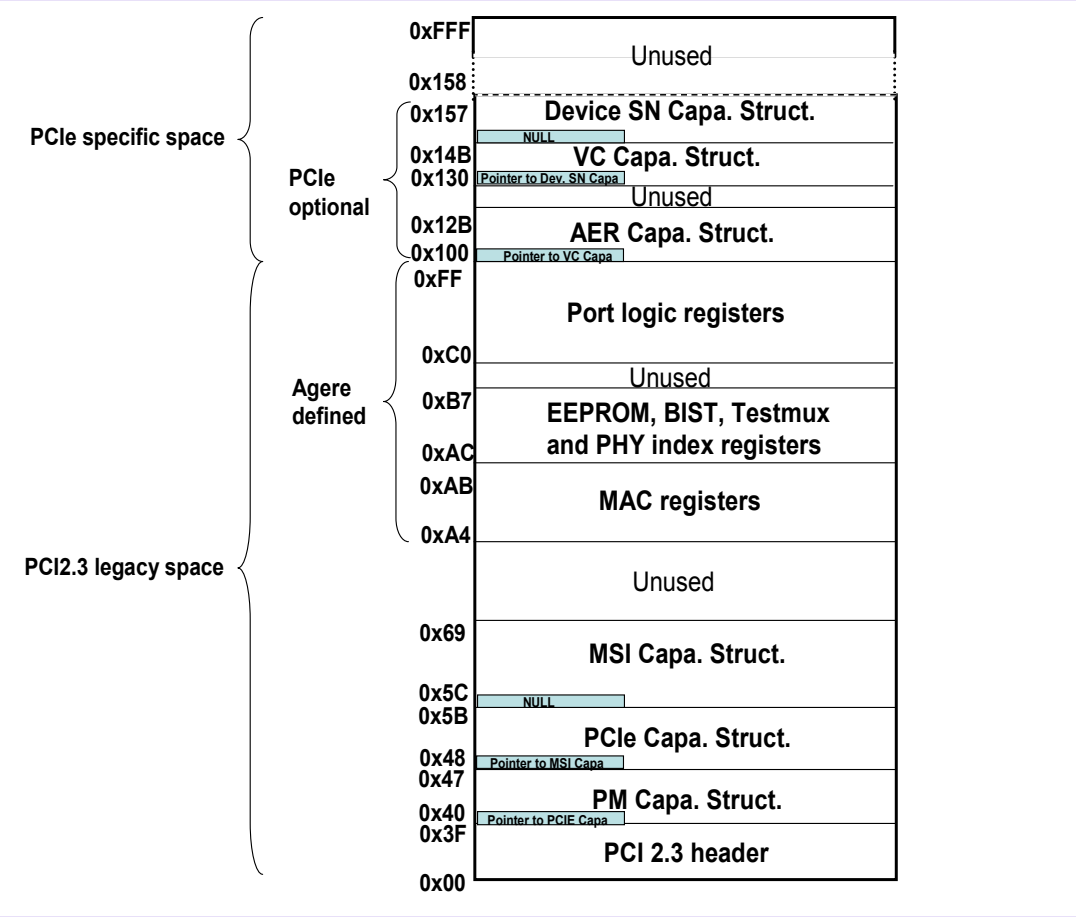


Virtual Sequences (cont)

- BFM sequences can only do sequences of their own type ---tightly connected to their own type and items
- Virtual sequences can do sequences of other types
- Drive more than one agent
- Model a more generic driver

PCIe Configuration Sequences

- ET1310 PCI Express register resource map



PCIe Configuration Sequences (cont)

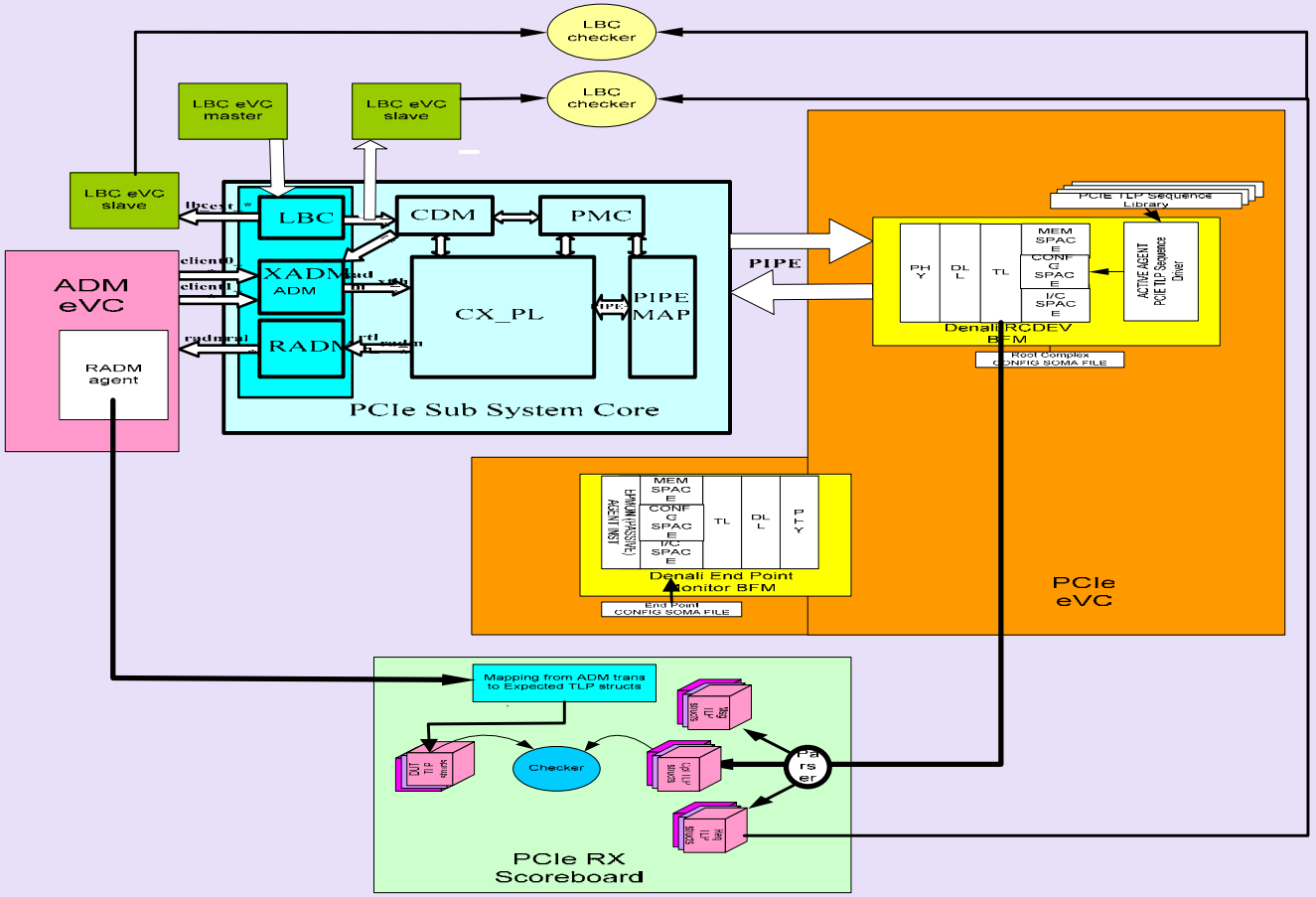
- The complete ET1310 PCIe configuration sequence is actually composed of semi-independent subsequences.
- Each subsequence impacts a natural set of logical register blocks shown in the previous diagram.
- High-level modeling of the configuration processes.
- Knowing what our device is and its precise specification allows to shortcut some procedures that would happen in a real system.

PCIe Configuration Sequences (cont)

- Completer (Target, Slave) and Requester (Initiator, Master) enabling
- Register block: PCI 2.3 header
- Expansion ROM enabling
- PM (Power Management) initial settings
- PCI compatible basic error reporting enabling
- MSI settings
- Ack/Nak latency timer and Replay timer settings
- Advanced Error Reporting settings

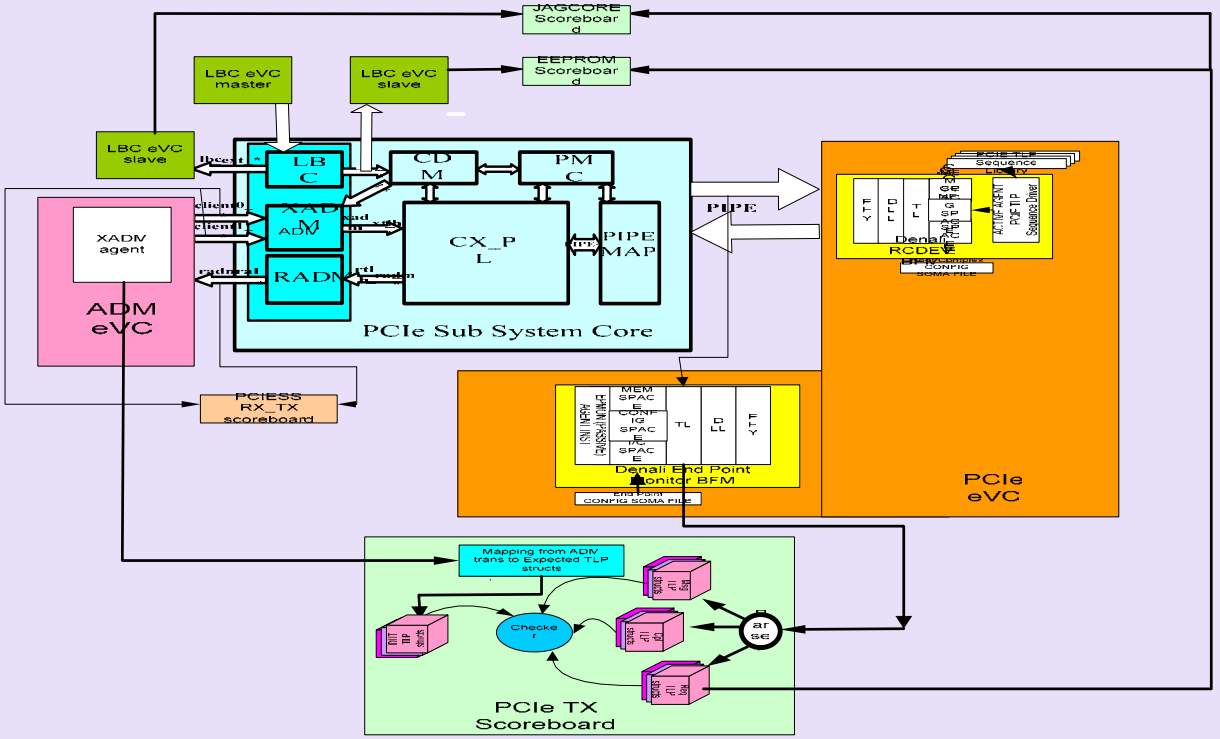
PCIe Scoreboard

- PCIe Scoreboard (RX path)



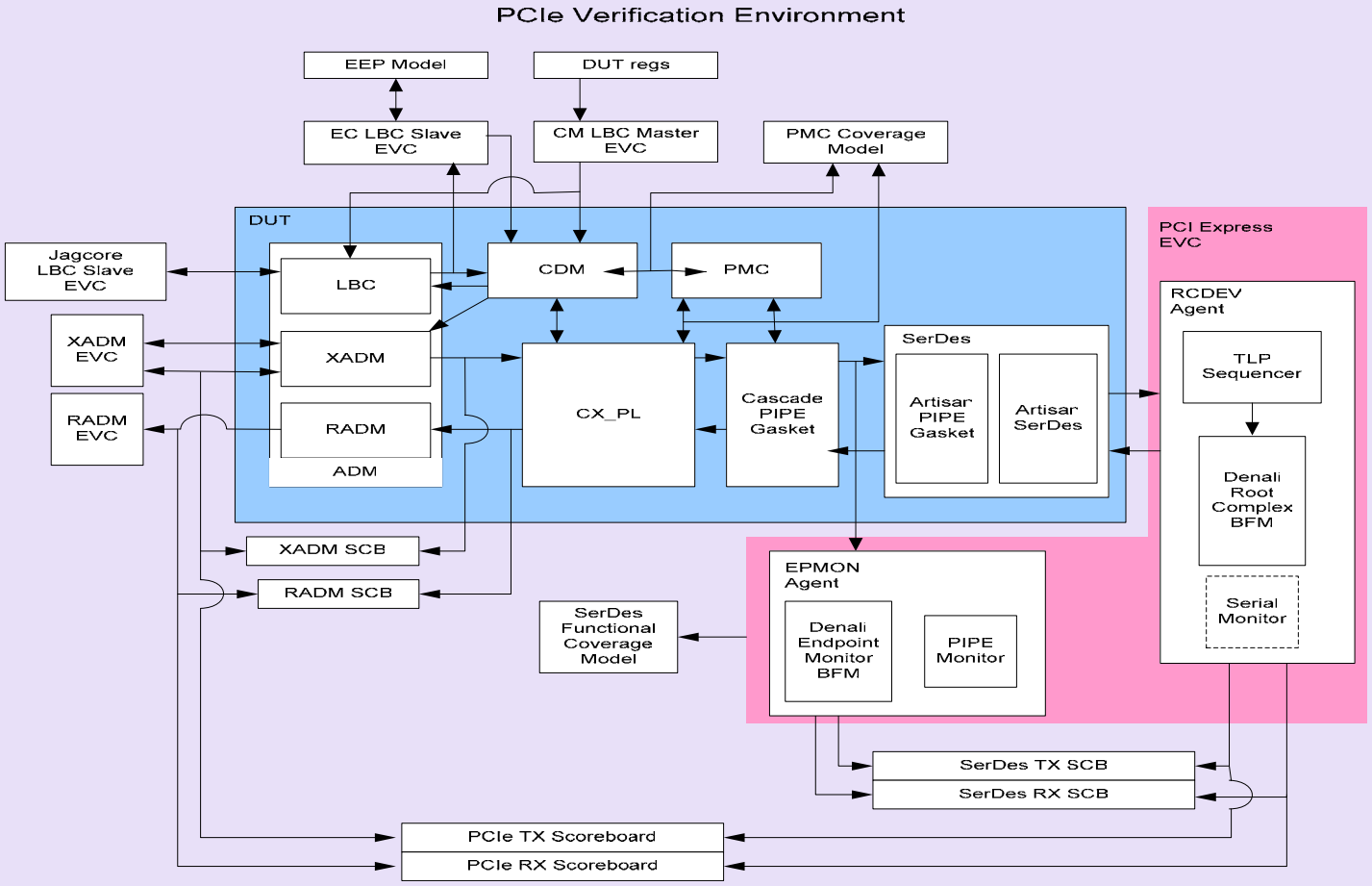
PCIe Scoreboard (cont)

- PCIe Scoreboard (TX path)



SERDES Scoreboard

- SERDES scoreboard in PCIe verification env:



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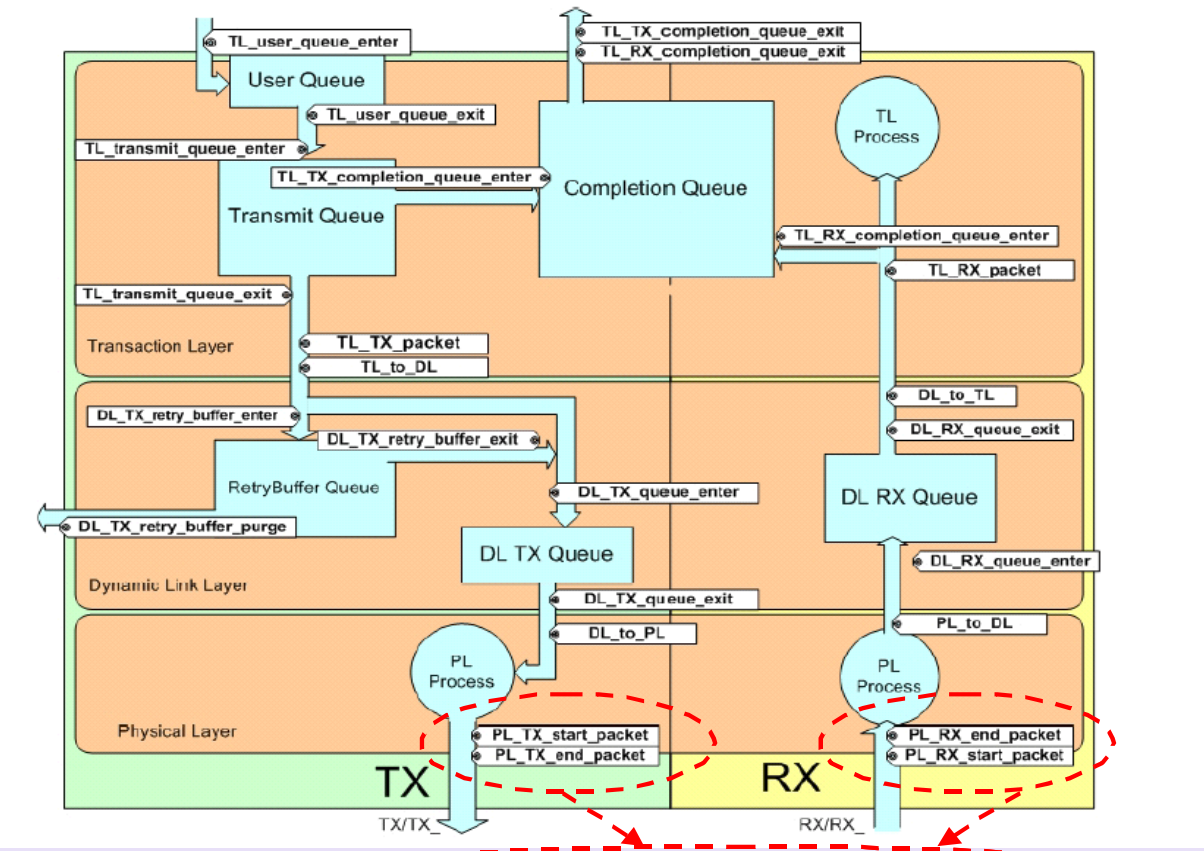
SERDES Scoreboard (cont)



Denali Callbacks Used to Support SerDes Scoreboard

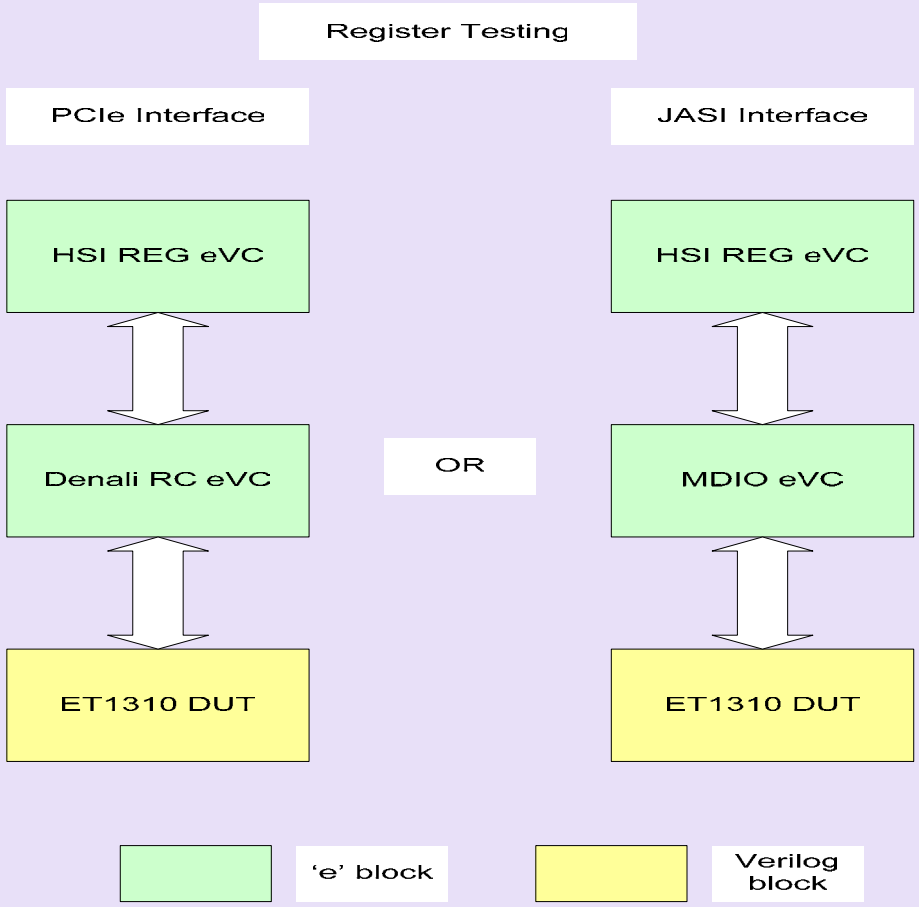
Reference : Denali PureSpec for PCI Express User's Manual

Register Testing

- The PCIe configuration registers are most commonly accessed with PCI Express configuration reads and writes. The MAC-PHY registers are most commonly accessed with PCI Express memory reads and writes.
- The HSI Reg eVC is used throughout the verification environment and in the tests to perform the reads/writes.
- PCIe configuration registers and MAC-PHY memory mapped registers can also be accessed with the JASI protocol. JASI is a proprietary protocol developed by Agere.

Register Testing (cont)

Register Testing



Successful Verification

- Use of right tools for the verification process
- Use the correct information to automate the verification process
- Make verification environment close to the real operating environment
- Stressing the design as much as possible

Proof of Successful Verification

- Current Silicon Status
- Demonstrated PCIe interoperability across multiple chipsets
  - ✓ Intel PCI Express Chip Sets
  - ✓ Interoperability test with SiS, VIA, nVIDIA, on-going with ATI
  - ✓ Demonstrated interoperability with Intel, VIA, ATI and nVIDIA at PCI-SIG compliance workshop
- Silicon Status proves the successful verification !

References

- PCI Express Base Specification, version 1.0a - PCI Express (PCI-SIG)
- PureSpec Based eVC for PCI Express Verification – Anand Chavan , Agere Systems, Denali MemCon 2004
- PureSpec for PCI Express User's Manual - Denali Software, Inc.
- e Reuse Methodology (eRM) Developer's Manual- Cadence Design Systems, Inc

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