



PCI

SIG[®]

The logo features the text "PCI" in a bold, italicized, black sans-serif font. A stylized blue swoosh, composed of two curved segments, connects "PCI" to "SIG". The text "SIG" is also in a bold, italicized, black sans-serif font, followed by a registered trademark symbol (®). The entire logo is set against a dark blue background with a bright, glowing light source on the right, creating a lens flare effect.



PCI-SIG® Architecture Overview

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IC Design Engineer
LSI Corporation



What's all this PCI stuff anyway?

- **Presentation will cover basic concepts and their evolution from PCI through PCI-X™ to PCI Express®**
 - ✓ **Specs written assuming designers have these key background concepts**
 - ✓ **High level overview of PCI, PCI-X, PCI Express**

- **Update on new software controls in PCIe 2.0**

PCI Background



Revolutionary AND Evolutionary

■ PCI

✓ Revolutionary

- Plug and Play jumperless configuration (BARs)
- Unprecedented bandwidth
 - 32-bit / 33MHz – 133MB/sec
 - 64-bit / 66MHz – 533MB/sec
- Designed from day 1 for bus-mastering adapters

✓ Evolutionary

- System BIOS maps devices then operating systems boot and run without further knowledge of PCI
- PCI-aware O/S could gain improved functionality



Revolutionary AND Evolutionary

■ PCI-X

✓ Revolutionary

- Unprecedented bandwidth
 - Up to 1066MB/sec with 64-bit / 133MHz
- Registered bus protocol
 - Eased electrical timing requirements
- Brought split transactions into PCI “world”

✓ Evolutionary

- PCI compatible at hardware *AND* software levels
- PCI-X 266/533 added as “mid-life” performance bump
 - 2133MB/sec at PCI-X 266 and 4266MB/sec at PCI-X 533



Revolutionary AND Evolutionary

■ PCI Express (aka PCIe®)

✓ Revolutionary

- Unprecedented bandwidth
 - x1: 250MB/sec in *EACH* direction
 - x16: 4000MB/sec in *EACH* direction
- “Relaxed” electricals due to serial bus architecture
 - Point-to-point, low voltage, dual simplex with embedded clocking

✓ Evolutionary

- PCI compatible at software level
 - Configuration space
 - Power Management
 - Of course, PCIe-aware O/S can get more functionality
- Transaction layer familiar to PCI/PCI-X designers
- System topology matches PCI/PCI-X

PCI Concepts



PCI Concepts

- **Address spaces**
 - ✓ **Memory – 64-bit**
 - ✓ **I/O – 32-bit (non-burstable since PCI-X)**
 - ✓ **Configuration (“Config”) – Bus/Device/Function**

- **Key configuration space regs/concepts**
 - ✓ **Base Address Registers (BARs)**
 - 64-bit vs 32-bit addressing
 - ✓ **Linked list of capabilities**

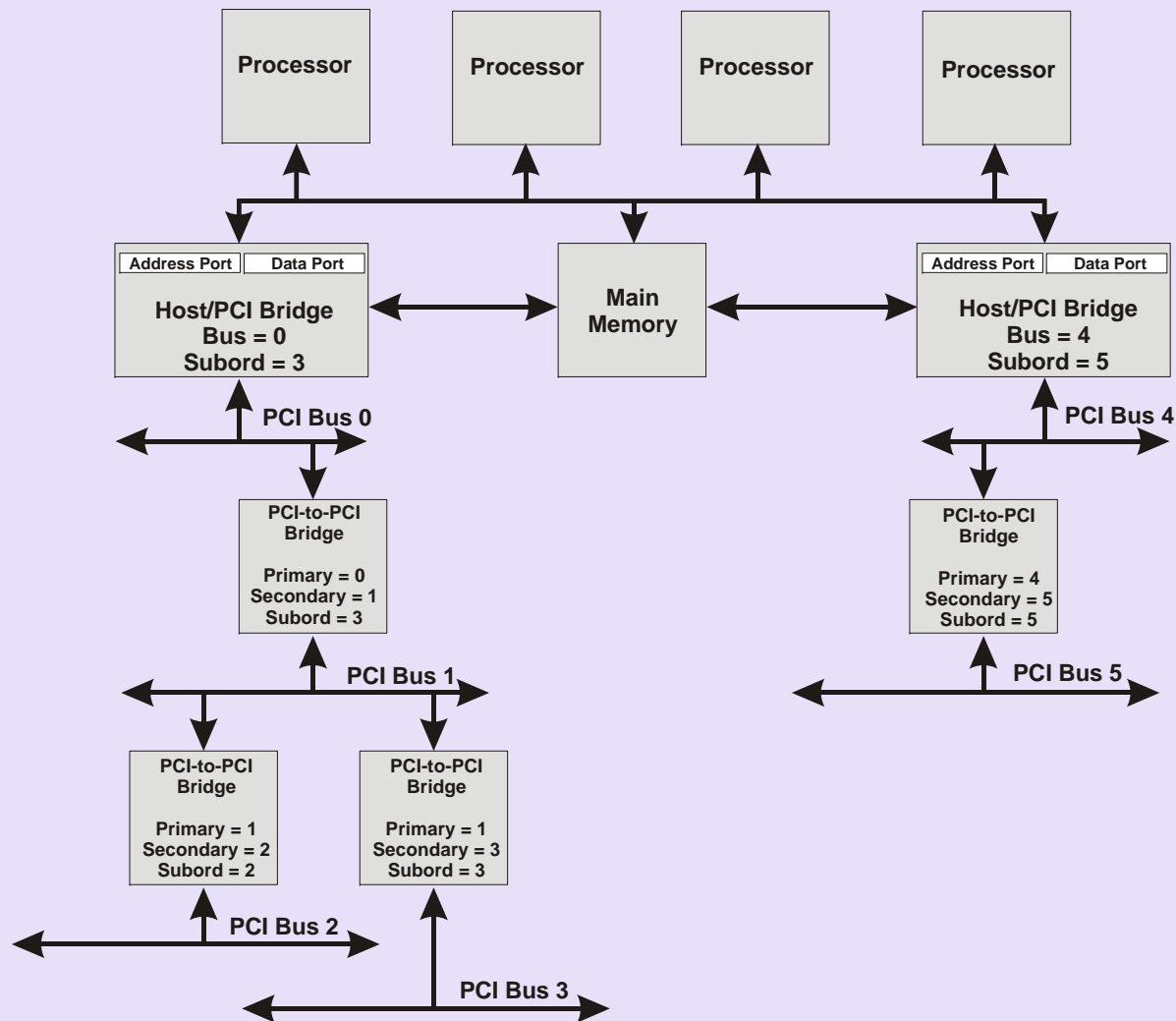
Address spaces – Memory & I/O

- **Memory space mapped cleanly to CPU semantics**
 - ✓ 32-bits of address space initially
 - ✓ 64-bits introduced via Dual-Address Cycles (DAC)
 - Extra clock of address time on PCI/PCI-X
 - 4DWORD header in PCI Express
 - ✓ Burstable
- **I/O space mapped cleanly to CPU semantics**
 - ✓ 32-bits of address space
 - Actually much larger than CPUs of the time
 - ✓ Non-burstable
 - Most PCI implementations didn't support
 - PCI-X codified
 - Carries forward to PCI Express

Address spaces – Configuration

- **Configuration space???**
 - ✓ Allows control of devices' address decodes without conflict
 - ✓ No conceptual mapping to CPU address space
 - Memory-based access mechanisms introduced with PCI-X and PCIe
 - ✓ Bus / Device / Function (aka BDF) form hierarchy-based address
 - “Functions” allow multiple, logically independent agents in one physical device.
 - E.g. combination SCSI + Ethernet device
 - 256 bytes or 4K bytes of configuration space per device
 - PCI/PCI-X bridges form hierarchy
 - PCIe switches form hierarchy
 - Look like PCI-PCI bridges to software
 - ✓ “Type 0” and “Type 1” configuration cycles
 - Type 0: to same bus segment
 - Type 1: to another bus segment

Configuration Space (cont'd)





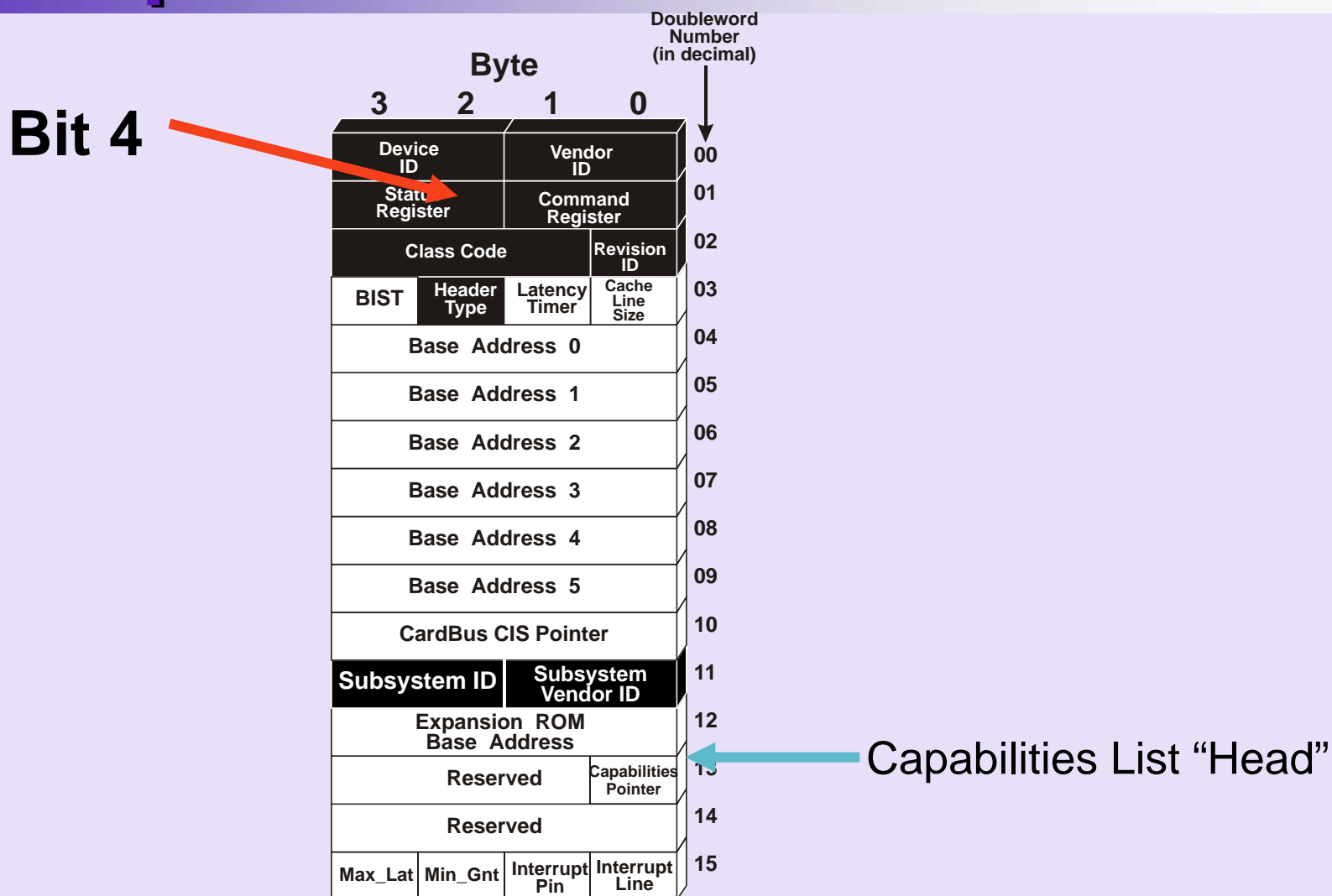
Using Configuration Space

- **Device Identification**
 - ✓ VendorID: PCI-SIG® assigned
 - ✓ DeviceID: Vendor self-assigned
 - ✓ Subsystem VendorID: PCI-SIG
 - ✓ Subsystem DeviceID: Vendor
- **Address Decode controls**
 - ✓ Software reads/writes BARs to determine required size and maps appropriately
 - ✓ Memory, I/O, and bus-master enables
- **Other bus-oriented controls**

Byte				Doubleword Number (in decimal)
3	2	1	0	
Device ID		Vendor ID		00
Status Register		Command Register		01
Class Code			Revision ID	02
BIST	Header Type	Latency Timer	Cache Line Size	03
Base Address 0				04
Base Address 1				05
Base Address 2				06
Base Address 3				07
Base Address 4				08
Base Address 5				09
CardBus CIS Pointer				10
Subsystem ID		Subsystem Vendor ID		11
Expansion ROM Base Address				12
Reserved			Capabilities Pointer	13
Reserved				14
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	15



Using Configuration Space – Capabilities List





Using Configuration Space – Capabilities List (cont'd)

- **Linked list**

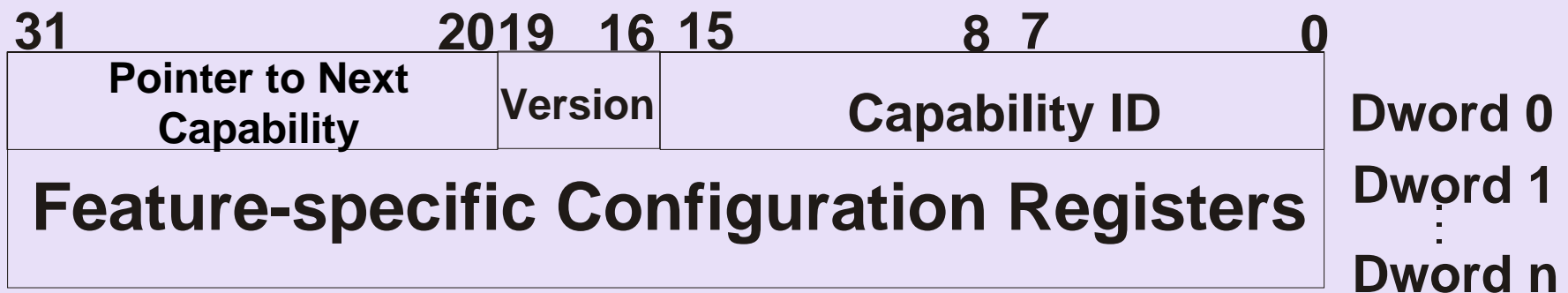
- ✓ **Follow the list! Cannot assume fixed location of any given feature in any given device**
- ✓ **Features defined in their related specs:**
 - PCI-X
 - PCIe
 - PCI Power Management
 - Etc...





Using Configuration Space – Extended Capabilities List

- PCI Express only
- Linked list
 - ✓ Follow the list! Cannot assume fixed location of any given feature in any given device
 - ✓ First entry in list is **always** at 100h
 - ✓ Features defined in PCI Express specification



Interrupts

- **PCI introduced INTA#, INTB#, INTC#, INTD# - collectively referred to as INTx**
 - ✓ **Level sensitive**
 - ✓ **Decoupled device from CPU interrupt**
 - ✓ **System controlled INTx to CPU interrupt mapping**
 - ✓ **Configuration registers**
 - **report A/B/C/D**
 - **programmed with CPU interrupt number**
- **PCI Express mimics this via “virtual wire” messages**
 - ✓ **Assert_INTx and Deassert_INTx**

What are MSI and MSI-X?

- **Memory Write replaces previous interrupt semantics**
 - ✓ PCI and PCI-X devices stop asserting INTA, INTB, INTC, INTD once MSI or MSI-X mode is enabled
 - ✓ PCI Express devices stop sending Assert_INTx and Deassert_INTx TLPs once MSI or MSI-X mode is enabled

- **NOTE: *Boot devices* and any device intended for a non-MSI operating system generally must still support the appropriate INTx signaling!**

MSI vs MSI-X

- **MSI uses one address with a variable data value indicating which “vector” is asserting**
- **MSI-X uses a table of independent address and data pairs for each “vector”**
 - ✓ **Allows software to control aliasing (when fewer vectors are allocated than requested)**
 - ✓ **Table size supports more vectors than MSI structure allowed**

PCI-X Explained



What is PCI-X?

- “PCI-X is high-performance backward compatible PCI”
 - ✓ PCI-X uses the same PCI architecture
 - ✓ PCI-X leverages the same base protocols as PCI
 - ✓ PCI-X leverages the same BIOS as PCI
 - ✓ PCI-X uses the same connector as PCI.
 - ✓ PCI-X and PCI products are interoperable
 - ✓ PCI-X uses same software driver models as PCI
- PCI-X is faster PCI
 - ✓ PCI-X 533 is up to 32 times faster than the original version of PCI
 - ✓ PCI-X protocol is more efficient than conventional PCI

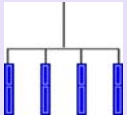
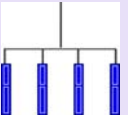
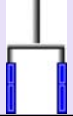
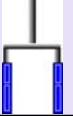
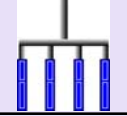
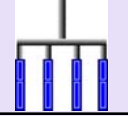
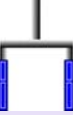
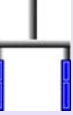






PCI-X Modes and Speeds



Mode 1



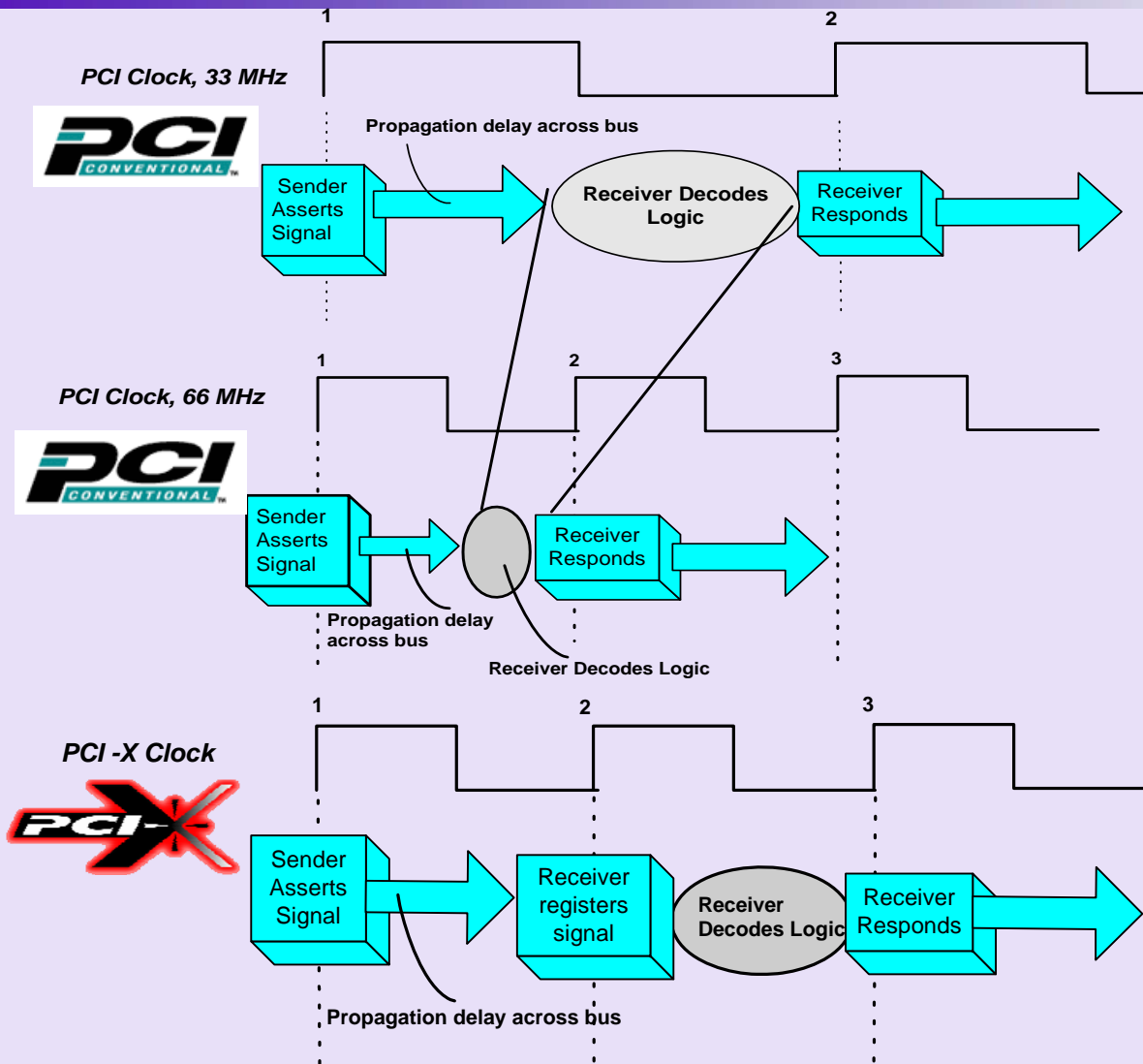
Mode 2

Mode	V _{I/O}	64-Bit		32-Bit		16-Bit	Error Prot	Conf Bytes	DIM
		Slots*	MB/s	Slots*	MB/s				
PCI 33	5V/3.3V		266		133	N/A	par	256	N/A
PCI 66	3.3V		533		266	N/A	par	256	N/A
PCI-X 66	3.3V		533		266	N/A	par or ECC	256	yes
PCI-X 133 (operating at 100 MHz)	3.3V		800		400	N/A	par or ECC	256	yes
PCI-X 133	3.3V		1066		533	N/A	par or ECC	256	yes
PCI-X 266	1.5V		2133		1066	533	ECC	4K	yes
PCI-X 533	1.5V		4266		2133	1066	ECC	4K	yes

* For lower bus speeds, # slots / bus is implementation choice to share bandwidth



Registered Bus Protocol



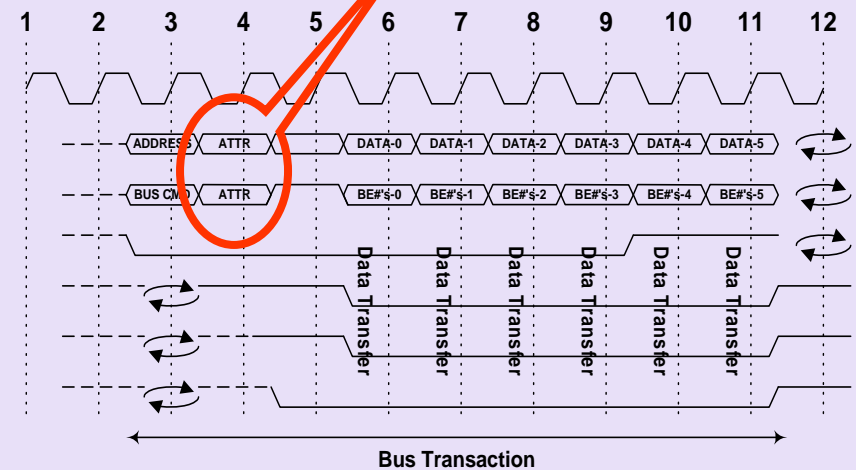
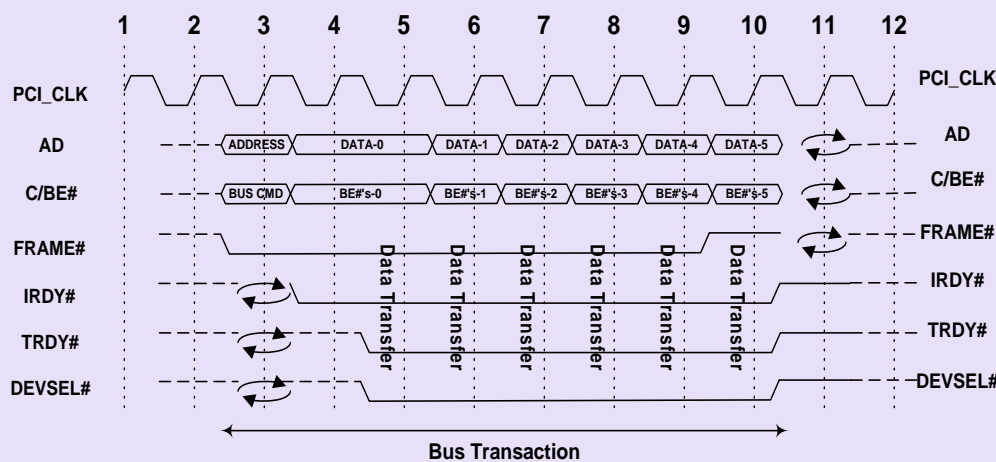
- PCI @ 33MHz
 - ✓ 30 ns period
 - ✓ 7 ns setup time
- PCI @ 66MHz
 - ✓ 15 ns period
 - ✓ 3ns setup time
- PCI-X registered protocol allocates a full clock period for logic decision
 - ✓ @ 66MHz - 15ns
 - ✓ @ 133MHz - 7.5ns



PCI 2.x/3.0 vs. PCI-X Mode 1

- Same bus and control signals
- Evolutionary protocol changes
- Clock frequency up to 133 MHz

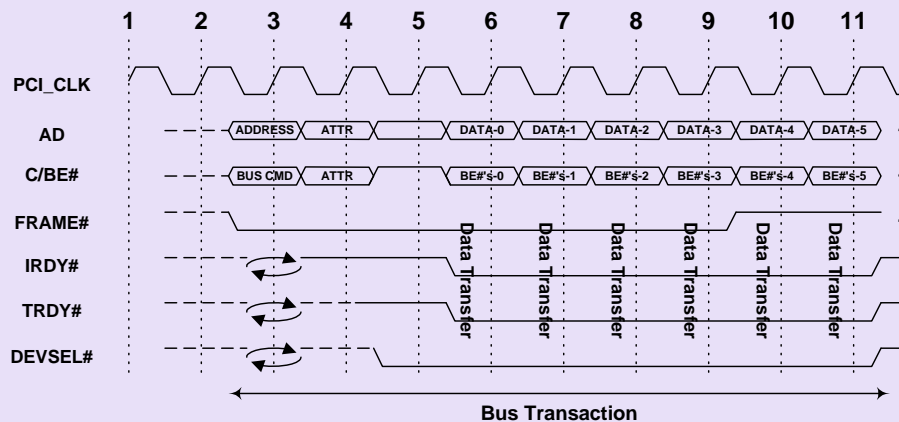
New “Attribute”
phase for
enhanced features



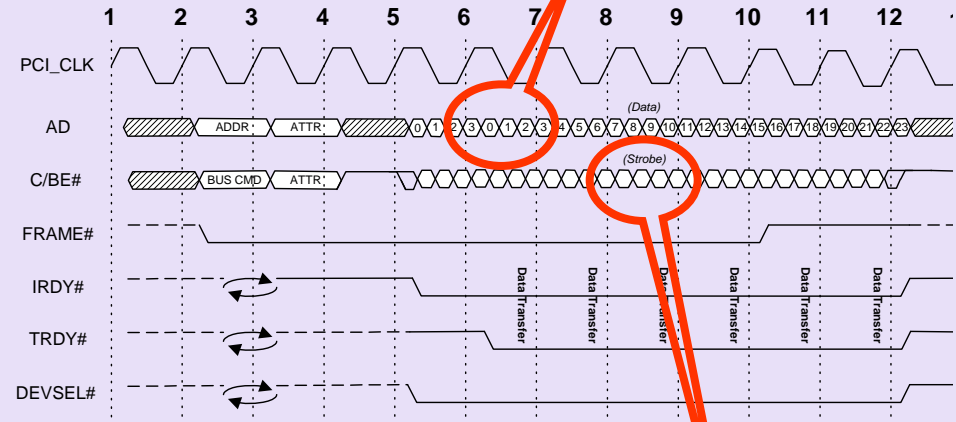


PCI-X 66/133 (Mode 1) vs. PCI-X 266/533 (Mode 2)

- Same bus and control signals
- PCI-X 266 moves 2x the data
PCI-X 533 moves 4x the data
- Clock frequency up to 133 MHz



PCI-X 66/133 (Mode 1)



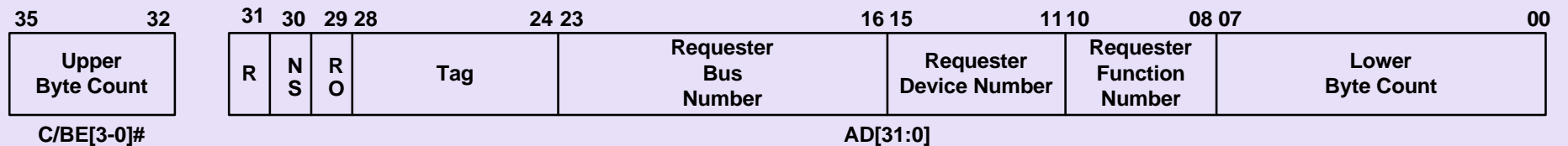
PCI-X 533 (Mode 2)

**source-
synchronous
data strobes
share C/BE pins**

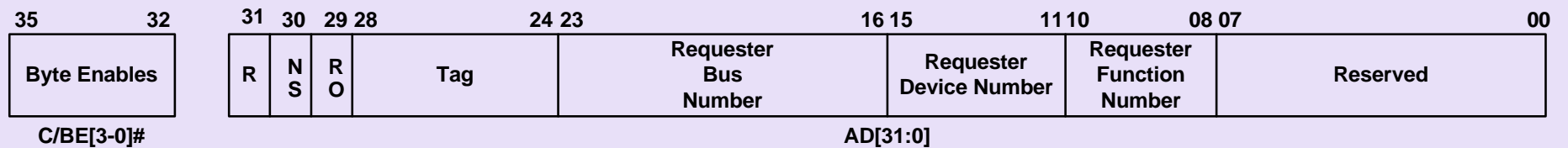


Transaction Attributes

Requester Attributes for Burst Transactions



Requester Attributes for DWORD Transactions



RO -- Relax ordering

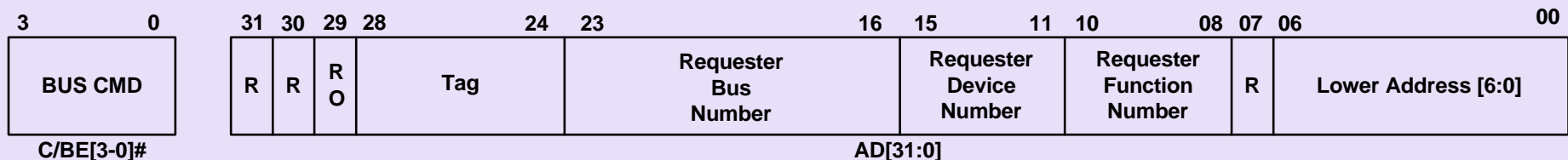
NS -- No Snoop

R -- Reserved



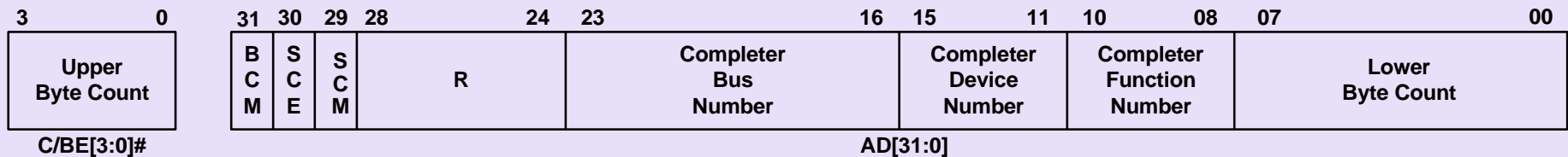
Transaction Attributes

Split Completion Address



RO -- Relaxed ordering

Completer Attributes



SCM -- Split Completion Message

SCE -- Split Completion Error

BCM -- Byte Count Modified

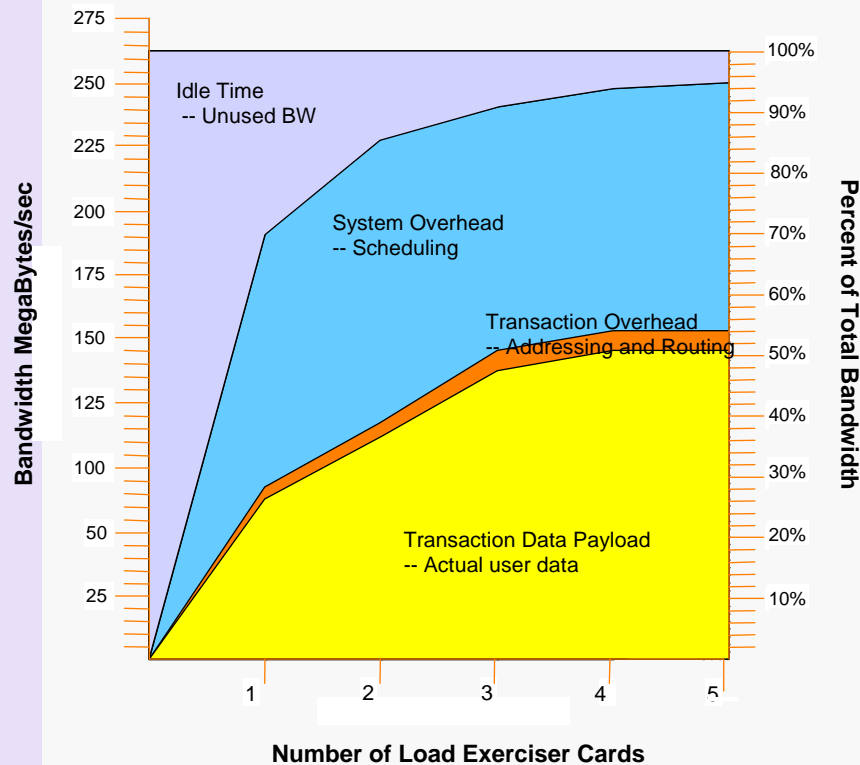
R -- Reserved

Split Transactions

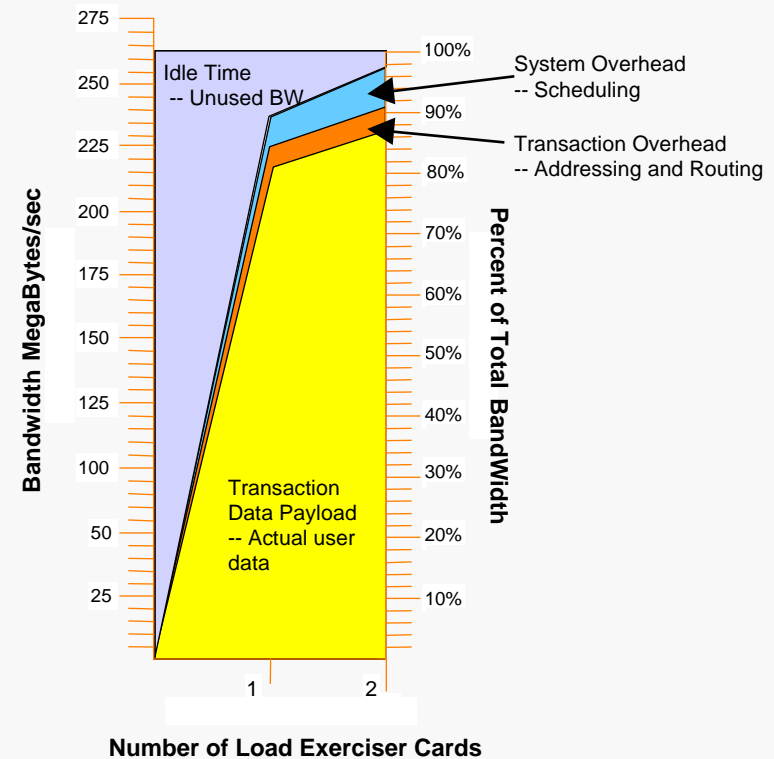
- Bus efficiency of Read almost as good as Write
- Split Completion routed back to requester across bridges using initiator's number and bus number
- Split Transaction components
 - ✓ Step 1. Requester requests bus and arbiter grants bus
 - ✓ Step 2. Requester initiates transaction
 - ✓ Step 3. Target (completer) communicates intent with new target termination, Split Response
 - ✓ Step 4. Completer executes transaction internally
 - ✓ Step 5. Completer requests bus and arbiter grants bus
 - ✓ Step 6. Completer initiates Split Completion

Efficient PCI-X Protocol

Bandwidth Usage with Conventional PCI Protocols



Bandwidth Usage with PCI-X Protocols, included in PCI-X 2.0



The PCI-X protocol is more efficient than traditional PCI.

PCI Express Overview



PCIe Architecture Features

■ PCI Compatibility

- ✓ Configuration and PCI software driver model
- ✓ PCI power management software compatible

■ Performance

- ✓ Scalable frequency (2.5-5GT/s)
- ✓ Scalable width (x1, x4, x8, x16)
- ✓ Low latency and highest utilization (BW/pin)

■ Physical Interface

- ✓ Point-to-point, dual-simplex
- ✓ Differential low voltage signaling
- ✓ Embedded clocking
- ✓ Supports connectors, modules, cables

■ Protocol

- ✓ Fully packetized split-transaction
- ✓ Credit-based flow control
- ✓ Hierarchical topology support
- ✓ Virtual channel mechanism

■ Advanced Capabilities

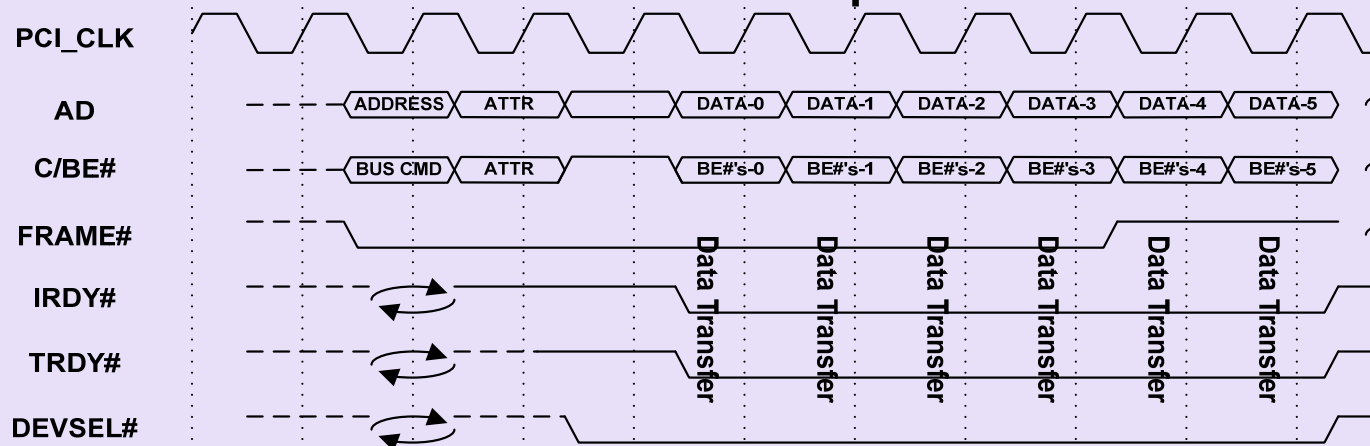
- ✓ CRC-based data integrity, hot plug, error logging

■ Enhanced Configuration Space

- ✓ Extensions and bridges into other architectures

PCIe Protocol Overview

■ PCI-X Address/Attribute phases:

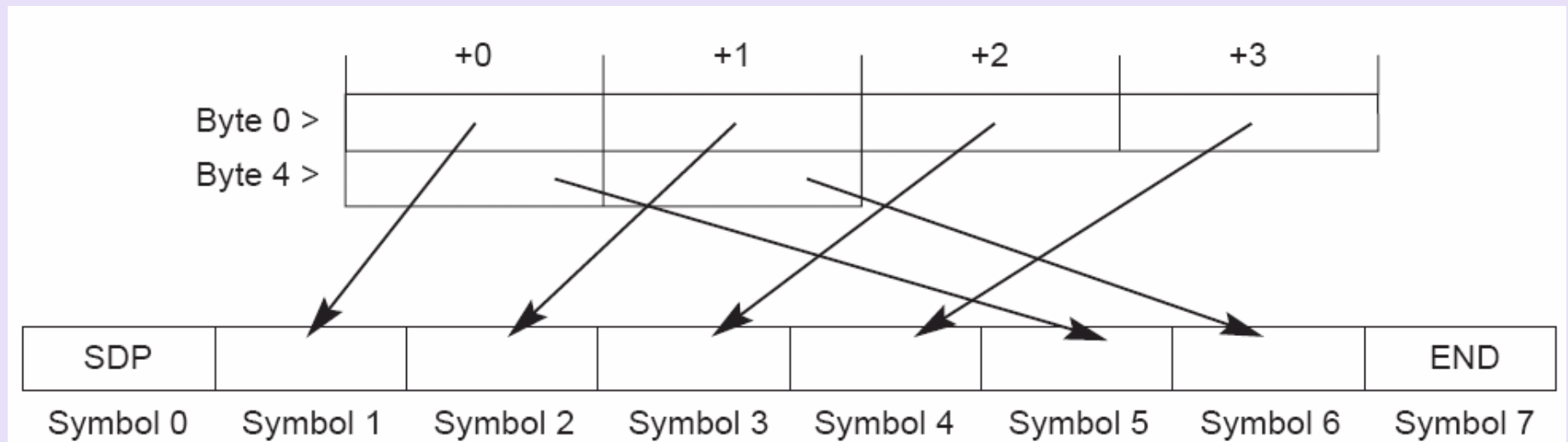


■ Evolved into the PCIe Packet Header:

	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0 >	R	Fmt x 1		Type				R	TC		Reserved				T D	E P	Attr		R	Length												
Byte 4 >	Requester ID																Tag								Last DW BE				1st DW BE			
Byte 8 >	Address[63:32]																															
Byte 12 >	Address[31:2]																														R	

PCIe Protocol Overview

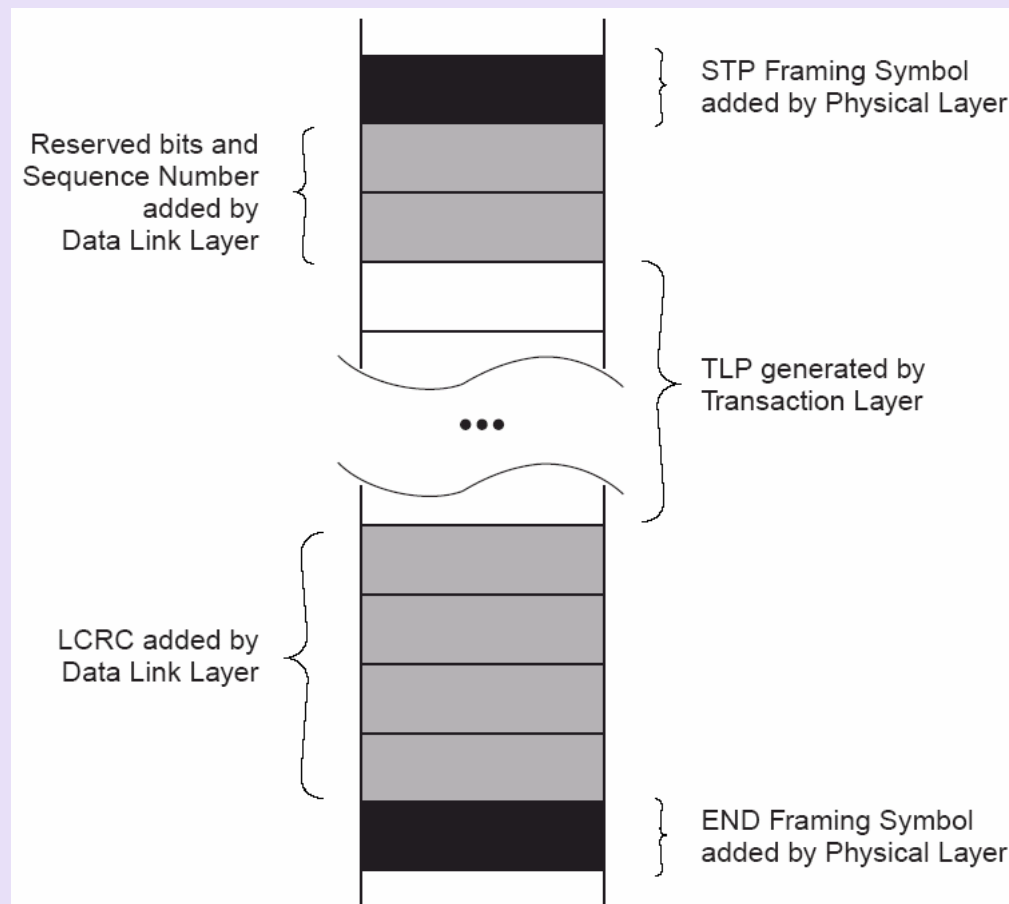
- The packet bytes get converted to 8b/10b and serialized



PCIe Protocol Overview

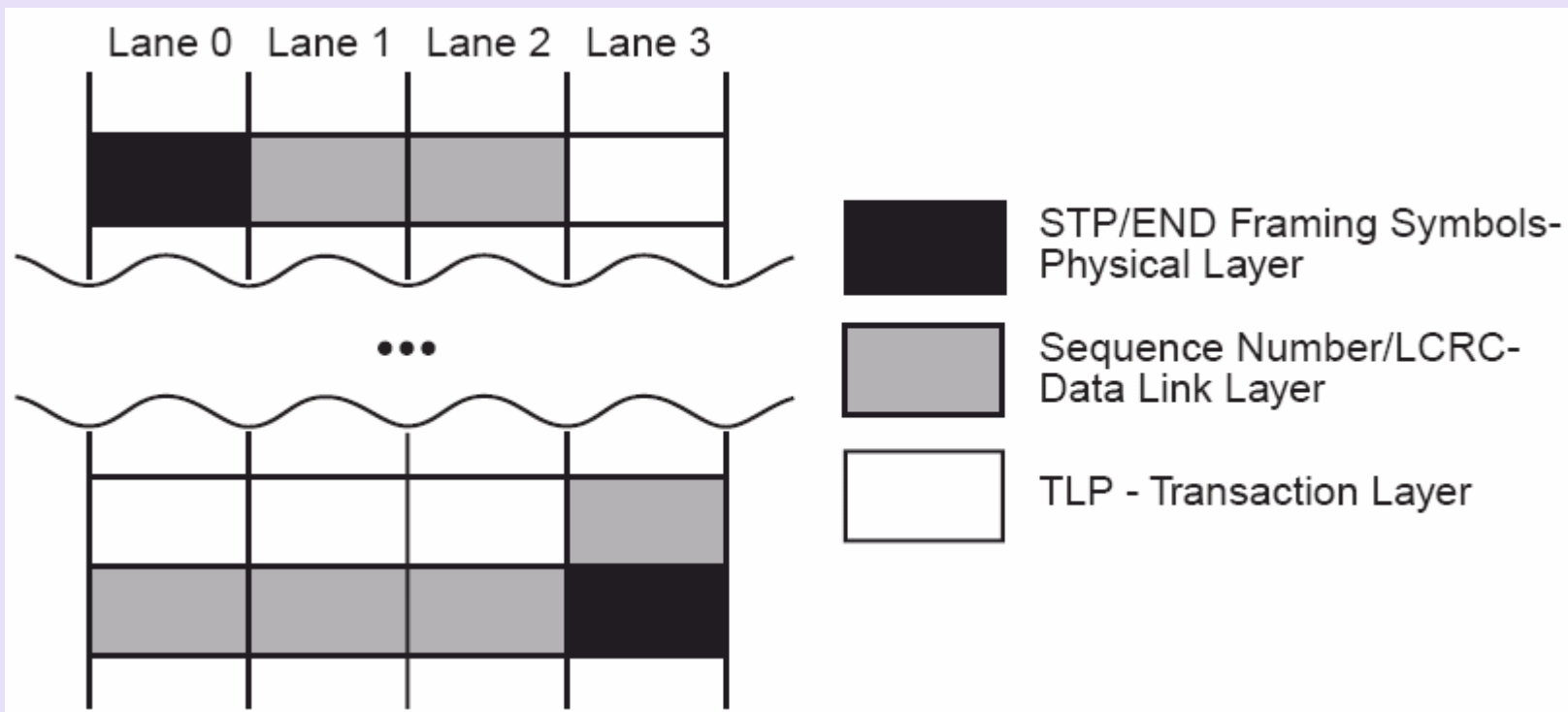
- Framing varies depending on link width

✓ x1

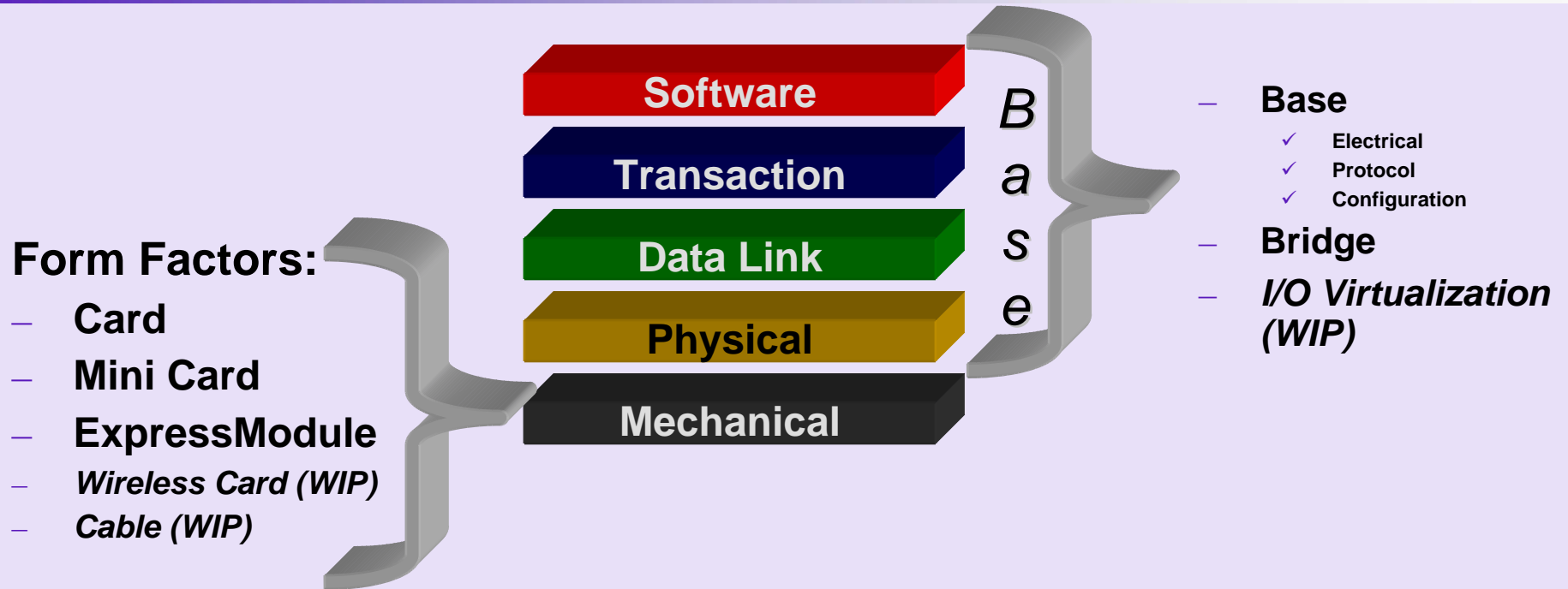


PCIe Protocol Overview

- Framing varies depending on link width
 - ✓ x4



PCIe Architecture Specifications

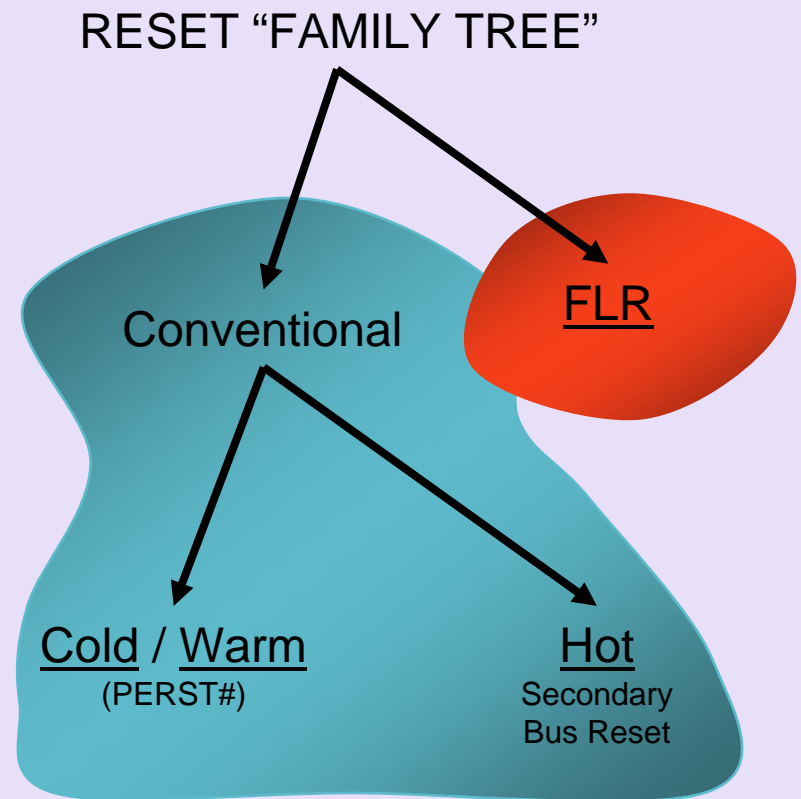


- Layered, scalable architecture
- Performance matched to applications
- Innovative form factors

PCI Express 2.0 Software Update

Function Level Reset (FLR)

- Returns Function specific registers to initialized state
- Existing resets may (but not required to) reset function internals
- Preserved configurations
 - ✓ Clock, Link, Power and Power Management
 - ✓ Sticky bits
- Stops and makes device quiescent
 - ✓ BME, MSI
 - ✓ De-asserts INTx
- Virtualization friendly





Link Speed Control & Bandwidth Notification

- Link Speed Control
 - ✓ By default, hardware automatically trains to highest common speed
 - Software can set upper bound
 - Hardware can always limit speed for link reliability reasons
 - ✓ By default, hardware is permitted to change speed autonomously for other purposes
 - Part of power management
 - Software can disable it
- SW controllable entering/exiting Compliance
- Bandwidth Notification
 - ✓ Notify software speed/width changes
 - Due to hardware autonomous link training
 - Required for >x1 or multiple link speed downstream ports

Access Control Services (ACS)

- Peer-to-peer traffic can be
 - ✓ Disabled
 - ✓ Isolated
- Applicable to switch and multi-function devices
- Configuration should be consistent across fabric
- Error handling
 - ✓ Handling of Completer Abort needs to be enhanced
- ACS implementation is *Optional*

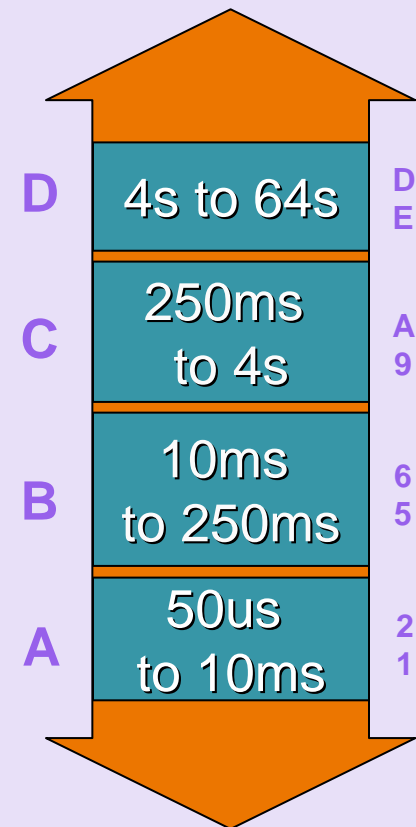


Alternative Routing-ID Interpretation (ARI)

- Eliminates Device ID
- Number of Functions increased from 8 to 256
- Requires ARI enabled downstream ports
 - ✓ Switches and Root ports
- Multi-function devices vs ARI devices
- ARI cap, extended function discovery (link list)
- MFVC arbitration with Function Groups
- ACS P2P egress control + Function Groups
- OS and software requirements
 - ✓ Firmware should not enable ARI (OS may not be ARI aware)
 - ✓ Configuration, PM, error handling, and INTx complications

Completion Timeout

- Required: Architected disable bit
 - ✓ 'Turns off' timeout
 - ✓ Not to be used in normal operation
- Optional: Completion Timeout value programmability
 - ✓ Supported ranges
 - Device Capabilities 2 Register
 - Contiguous selectable ranges
 - A, B
 - AB, BC
 - ABC, BCD
 - ABCD
 - ✓ Two choices within each selectable range
 - Device Control 2 Register





Power Budgeting and 5GT/s Link Controls

- Power budgeting
 - ✓ Optional, via Power Budgeting Capability
 - ✓ 250W, 275W, 300W addition
- Link Controls (Link Control 2 Register)
 - ✓ Selectable De-emphasis
 - Downstream port only
 - 1 -3.5dB
 - 0 -6dB
 - ✓ Compliance features
 - Transmit Margin, Enter Modified Compliance
 - Compliance SOS, Compliance De-emphasis

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PCI-SIG Developers Conference
Europe 2007

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PCI

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SIGTM