The Nuts and Bolts of Integrating PCIe® Into Your Design

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Agenda

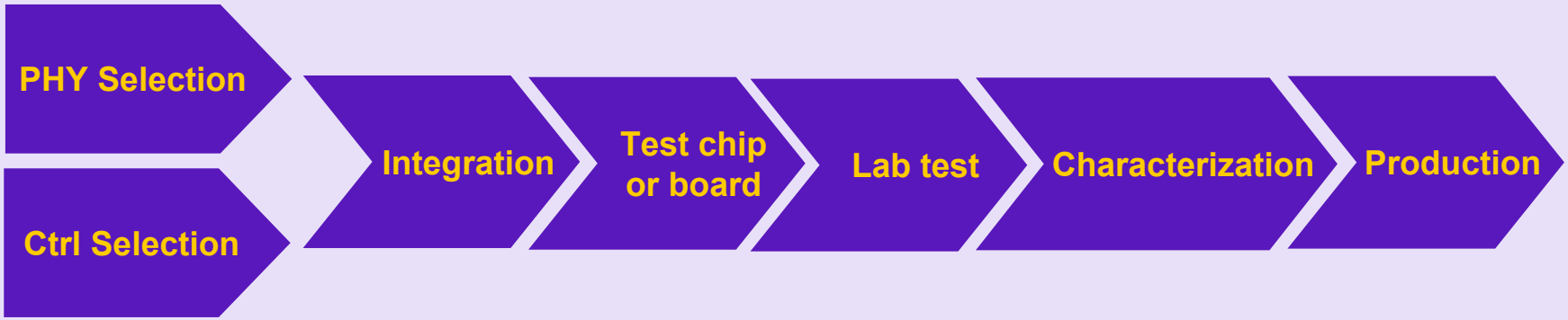
- Types of integration
- IP Selection
- Lab Setup
- Integration timeline
- Future migration of the design
- Summary

Note: all opinions, judgments, recommendations, etc. that are presented are the opinions of the presenter and do not necessarily reflect the opinions of the PCI-SIG®.

Types of Integration

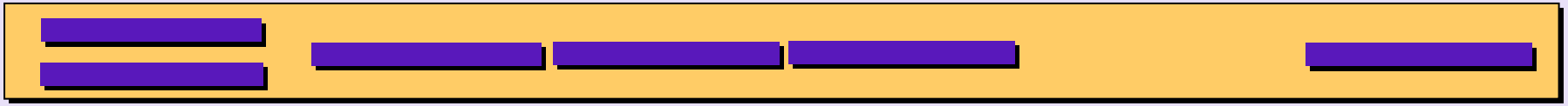
- Low volume designs
  - ✓ Prototype FPGA (+ PHY)
    - – Easy to start, but often a difficult path to volume
- Medium – high volume
  - ✓ Bridge chip (ASSP)
    - – Requires external silicon, no path to integration
  - ✓ Structured ASIC
    - + Custom single chip, fully characterized, readily migrated to standard cell using same PHY IP
- High volume
  - ✓ Standard Cell ASIC
    - + Full integration
    - – Full characterization and long development cycle

The Integration Process

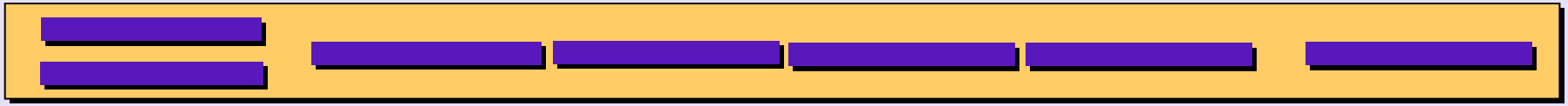


Structured ASIC, ASSP

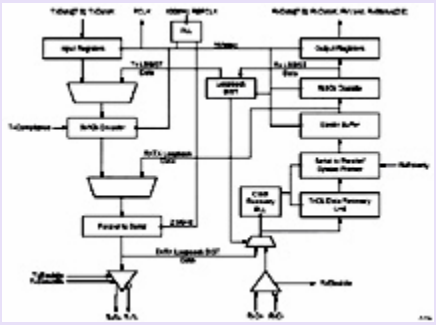
FPGA (+ PHY)



Standard Cell ASIC



PHY IP Selection



- Features
  - ✓ Compliance level
  - ✓ Optional features
  - ✓ Placement restrictions: Power supplies, moats
  - ✓ Pads included? How many metals?
  - ✓ Testability features for lab and production testing
    - BIST
    - Random pattern generation, loop-back
    - Models

Controller IP Selection

- Features
  - ✓ Configuration tools
    - Produce RTL in your chosen configuration
  - ✓ Lane and interface support
    - Must match PHY
  - ✓ Memory organization
    - Ensure required organization matches target technology, and allows for timing closure
  - ✓ Verification tools
    - Consider purchasing a ready-made test bench

Integration in Silicon

- PHY IP on silicon
  - ✓ Establish layout requirements
  - ✓ Ensure that the incoming IP merges with GDS – consider dry run
- Synthesizable Controller IP
  - ✓ Determine requirements, make design using configuration tool
  - ✓ Hook-up controller interface to PHY
  - ✓ Place, route
  - ✓ Close timing
- Build a Test chip
  - ✓ Bring out relevant test signals
  - ✓ Establish features required for bench testing
  - ✓ Package design

Laboratory Requirements

- Depend on the objectives
  - ✓ Structured ASIC, ASSP
    - – Test data eye and loopback
  - ✓ FPGA (+ External PHY)
    - – Add BER testing, more stringent jitter testing
  - ✓ Standard Cell ASIC
    - – Add full characterization
- For PCI-SIG test requirements, refer to PCI-SIG

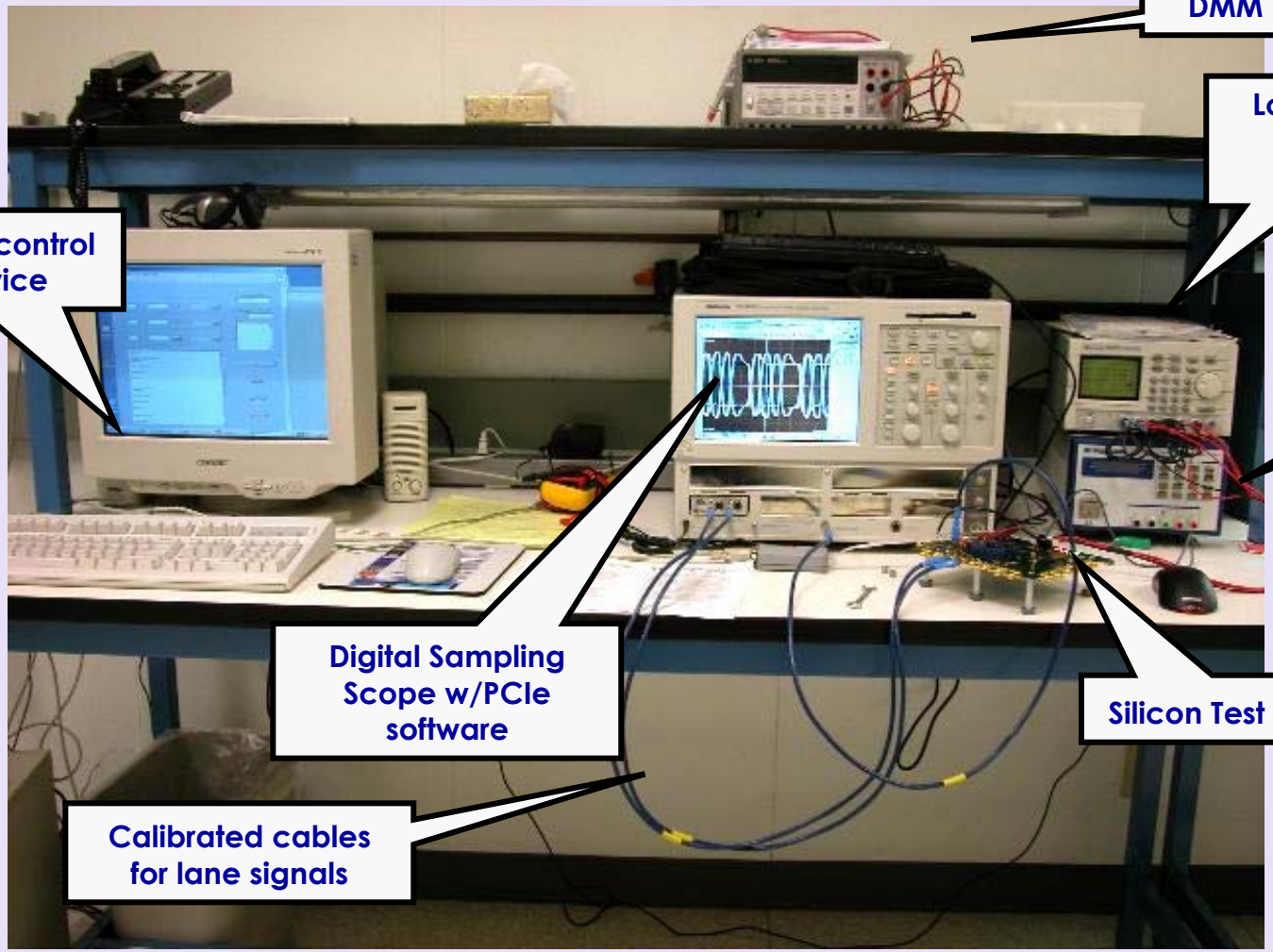
In The Lab

- Equipment requirements
  - ✓ Basic
    - Power supplies
    - High speed digital sampling oscilloscope
    - Calibrated cables
    - Clock source for spread spectrum clocking etc.
  - ✓ Intermediate
    - Serial Bit Error Rate Tester
    - Cable sets
    - Backplane (if required)

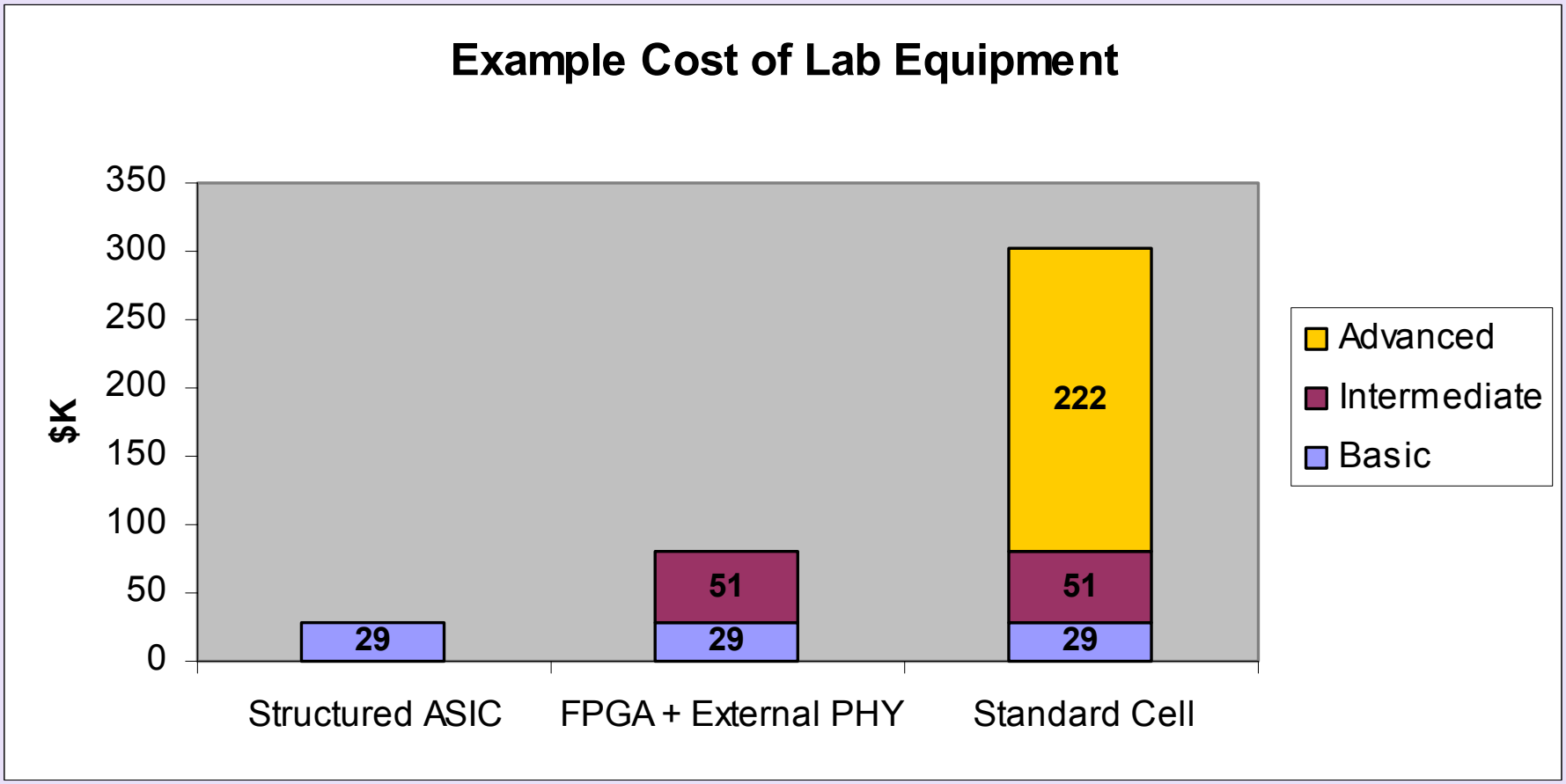
In The Lab (Cont'd)

- ✓ Advanced
  - Random, Sinusoidal, Deterministic jitter sources
  - Data pattern generator
  - Jitter analyzer
  - High-speed realtime oscilloscope
  - Arbitrary function generator
  - RF signal analyzer
  - Spectrum Analyzer
  - Source measurement unit

In The Lab (Basic)



Equipment Costs



Source: equipment quotes to ChipX, 2004-2006

Purchasing Equipment

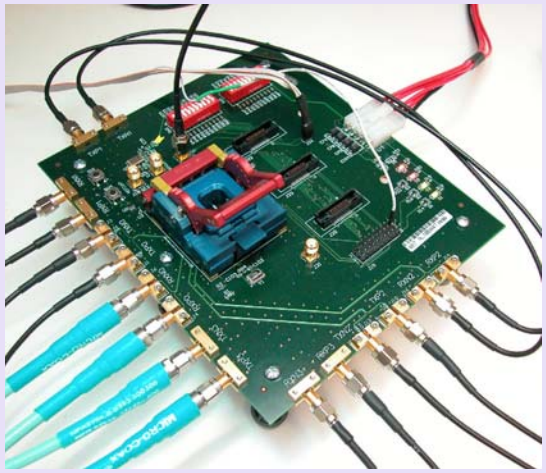
- New
  - ✓ Full warranty, full calibration
- Rent or lease for short term use
  - ✓ Useful when full characterization has been done by supplier
  - ✓ Usually with option to buy
- Refurbished
  - ✓ Ensure equipment is fully calibrated to original specifications
  - ✓ Consider buying the service contract
- Ebay?
  - ✓ Obsolete equipment may not be repairable
  - ✓ Calibration can be problematic
- Your mileage may vary. Not an official PCI-SIG position

In The Lab: People

- Lab Personnel
  - ✓ General lab experience
    - Proper equipment setup and operation
    - Use of reference standards
  - ✓ Knowledge of Gigabit signal integrity
    - Effects of impedance mismatch
    - Attenuation and bandwidth limiting
    - Poor or deteriorating connections
    - Sources of Interference (EMI)
  - ✓ Trained in anti-static procedures
    - Applies to both equipment and components under test

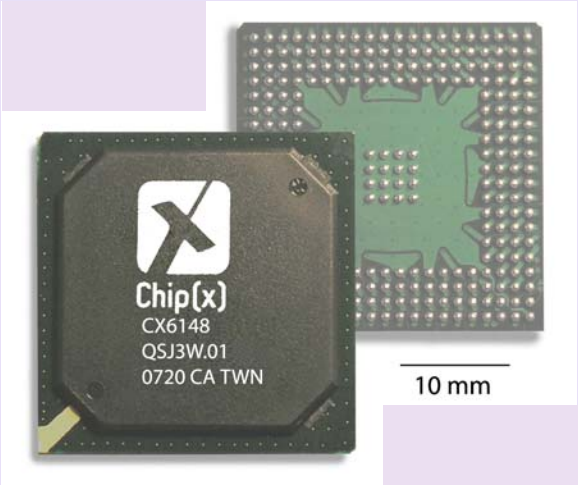
Test Platform

- Test chip + PCB
  - ✓ Test chip
    - – Should be optimized for either
      - PHY electrical characterization
      - Compliance testing
      - Demo and application
    - – One test chip can do it all, but may lead to confusing test results
    - – Avoid placing too many other circuits on the first test chip
  - ✓ PCB
    - – Build well ahead of test chip
      - Allow time for pre-silicon checks and minor rework if needed
    - – Employ best high-speed layout and design practices
    - – Use high quality components, especially sockets and connectors

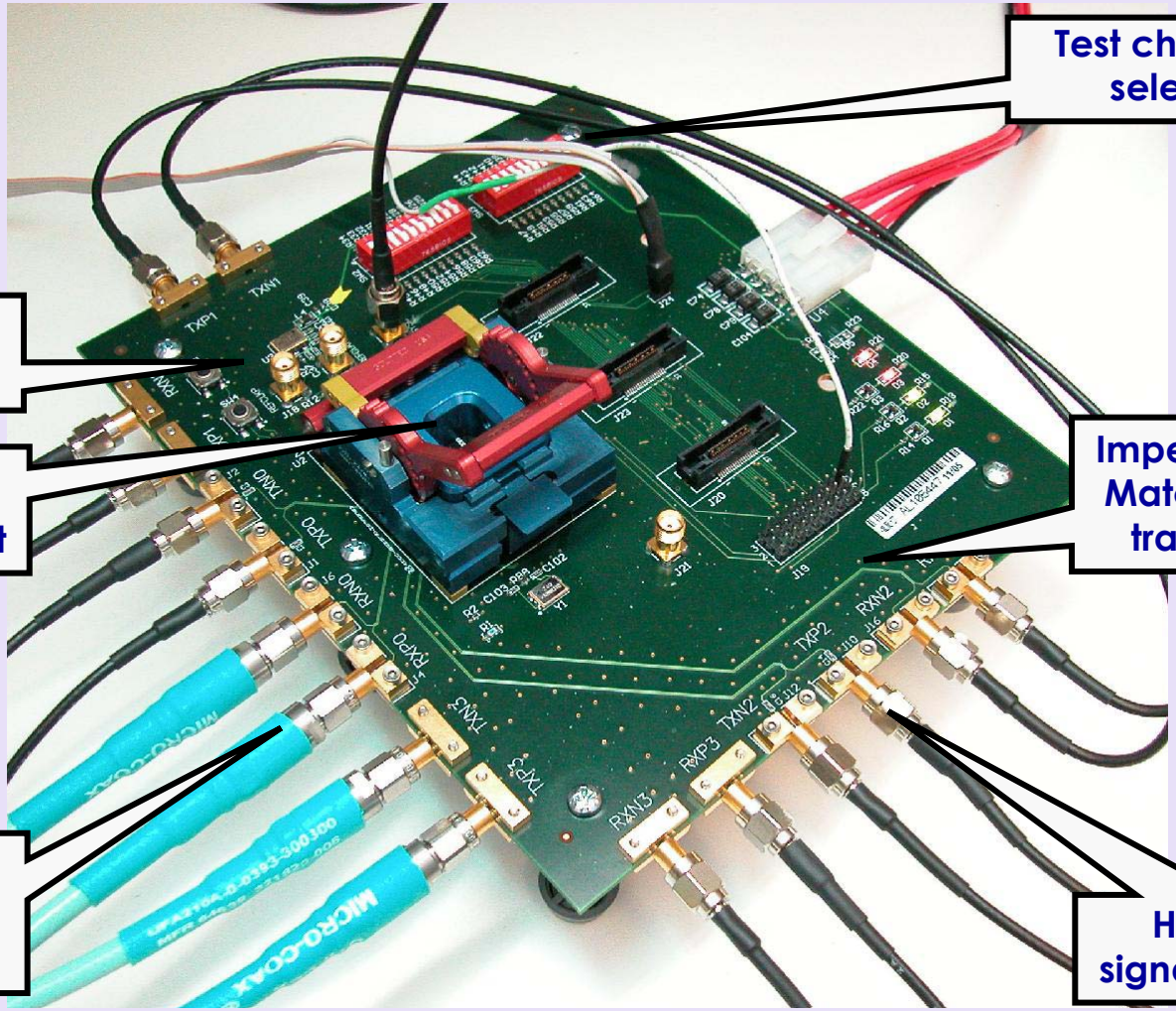


The Test Silicon

- FPGA + PHY
  - ✓ No test chip, but board level integration
  - ✓ Verify timing, jitter
  - ✓ Common issues: board layout or FPGA timing
- Structured ASIC
  - ✓ Fully characterized already
  - ✓ Development platform available
  - ✓ Common issues: typically outside PCIe design (fully integrated)
- Standard Cell ASIC
  - ✓ Requires full Characterization
  - ✓ Common issues typically with PHY performance

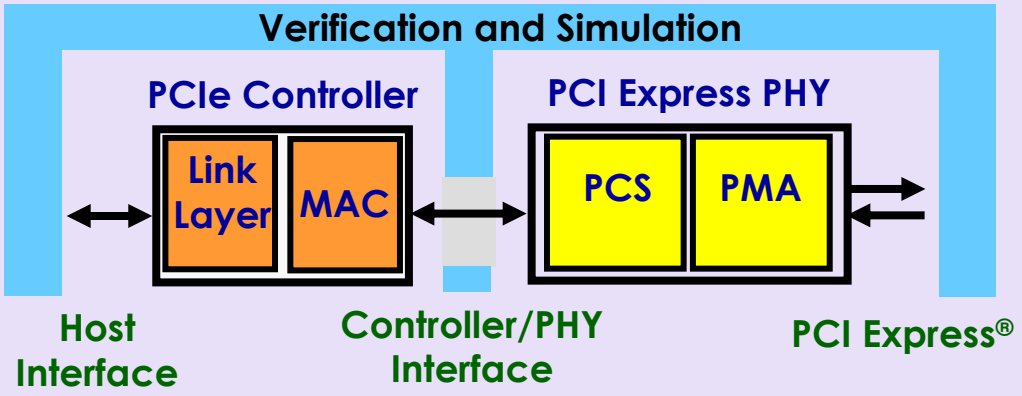


Example Characterization Board



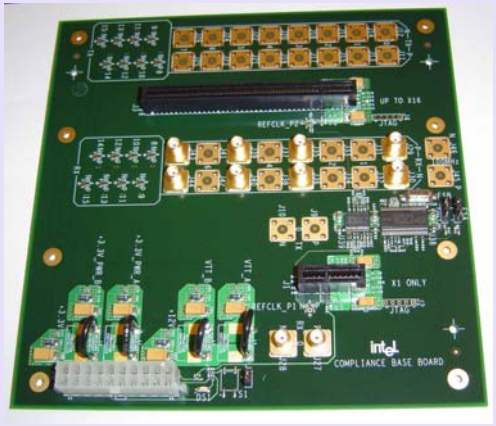
Getting ready for PCI-SIG compliance

- Start the preparations early in the integration cycle
  - ✓ Helps to find areas that need further attention
  - ✓ Greatly simplifies final compliance testing
- Start the verification early
  - ✓ Consider using complete third party ‘compliance’ testbenches to catch problems in the design stage
  - ✓ Note: ‘Compliance’ verification in models does not guarantee PCI-SIG compliance, and is not PCI-SIG endorsed



Getting ready for PCI-SIG Compliance

- In-house compliance dry-run
- Make sure your design is stable!
  - ✓ Hardware, firmware, board revisions etc.
  - ✓ Note your official version # for each portion of your design
- Check out the latest procedures and tools:
  - ✓ http://www.pcisig.com/specifications/pciexpress/technical_library/
- Use the appropriate PCI-SIG test fixture for electrical testing



CBB

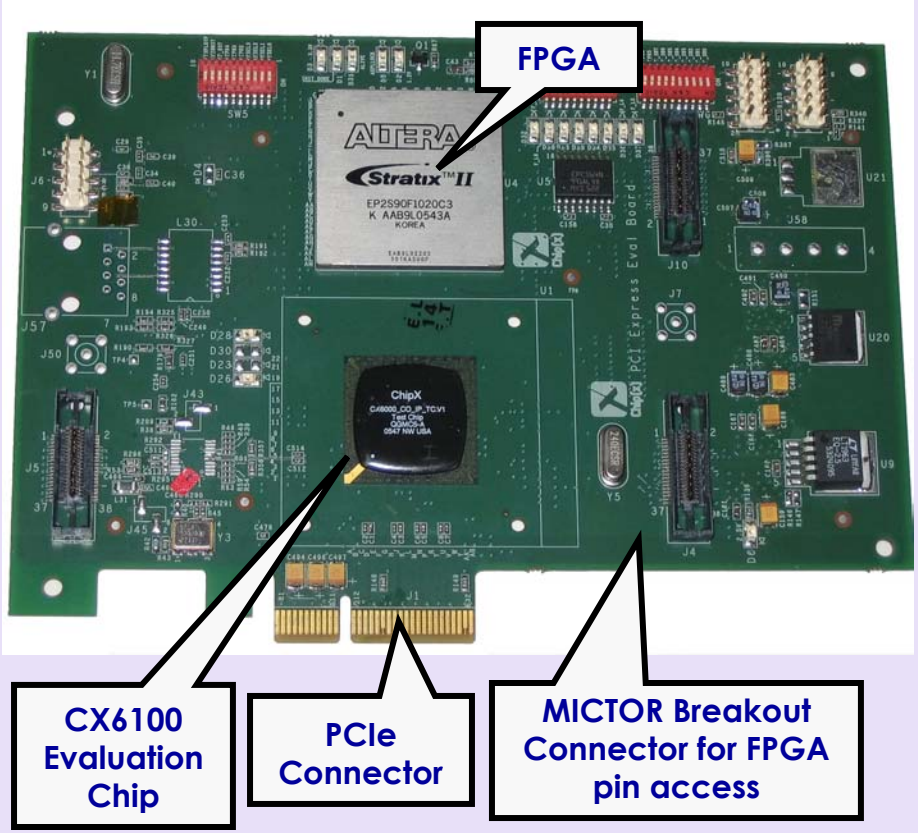
CLB

Compliance Testing Options

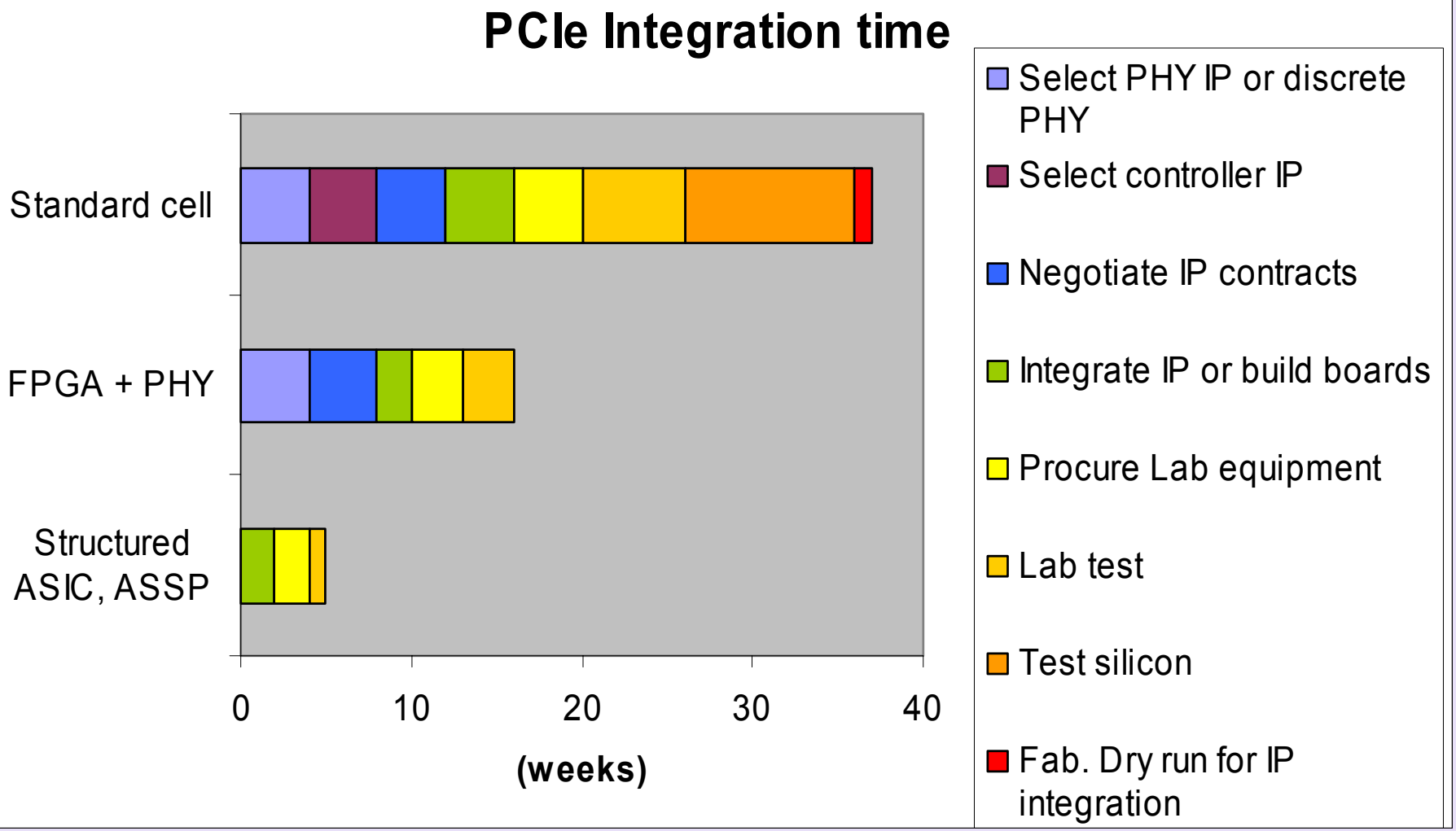
- Take a complete kit, for example:
  - ✓ Final and official version of checklists
  - ✓ Product(s) to be tested. Consider taking a spare
  - ✓ Full documentation, compilation tools, software and firmware source code
  - ✓ Don't forget the basics: soldering iron, re-work tools, static strap etc.
- PCI-SIG Compliance Workshop
  - ✓ Read the rules: http://www.pcisig.com/events/compliance_workshop
  - ✓ Check the schedule carefully. Book on time and be on time
  - ✓ Cost effective
- PCI-SIG approved third party compliance testing
  - ✓ Compliance testing on your own schedule
  - ✓ Typically offer additional services to help with bug-finding

Example Development Board

- 4x PCIe PHY to PIPE Structured ASIC evaluation chip
- Altera Stratix 2 EP2S90 for application development
- Optional ChipX PCIe Controller
- Develop with the PHY you will be using in final silicon
- Concurrent software and hardware design



Example Integration Timeline

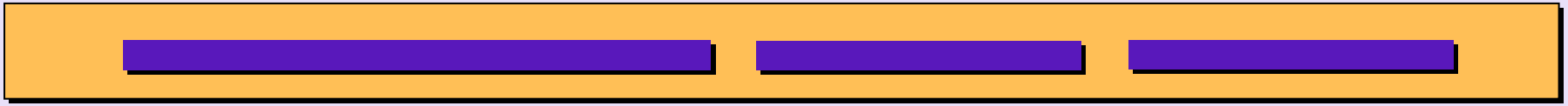


Design Migration

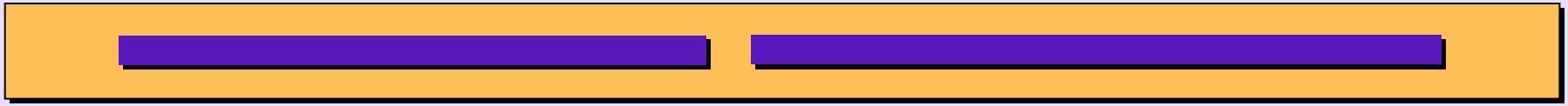
New PHY = new integration cycle

Structured ASIC, ASSP

FPGA (+ PHY)



Standard Cell ASIC



Build a PCIe Solution

- Structured ASIC
  - ✓ Pre-integrated, pre-validated IP
  - ✓ Concurrent hardware/software design using kit
  - ✓ Same PHY from development to high volume production
- FPGA (+ PHY)
  - ✓ Great prototyping tool
  - ✓ Often lacks migration path, tricky economics
- Standard Cell
  - ✓ Top choice for guaranteed high volume
  - ✓ High risk, slow to market

Thank you for attending the
PCI-SIG Developers Conference 2006.

For more information please go to
www.pcisig.com

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