
# PCI Express® 1.1 PHY Design Considerations

Milpitas, CA  Dec 5, 2005

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# Agenda

- Logical Physical Layer
- Electrical Physical Layer
- Link Training and Initialization (LTSSM)
- Layout Considerations

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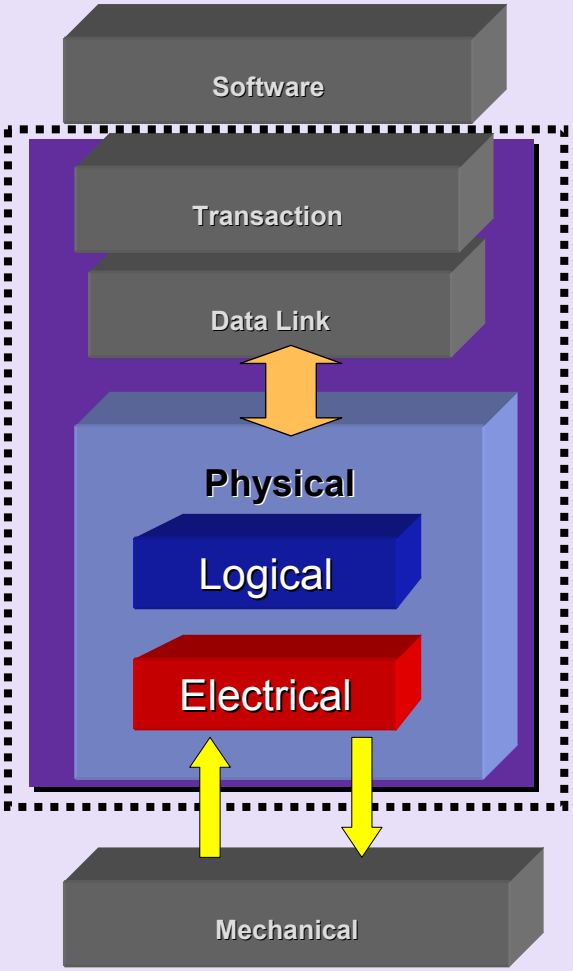
# PCI Express Physical Layer

- **PCI – PHY is digital in nature**
  - ✓ Parallel multi-drop bus
  - ✓ Bits, a clock, setup and hold times…
    - – Jitter essentially ignored
- **PCI Express – PHY is analog in nature**
  - ✓ Based on serial technology
  - ✓ Techniques developed by the communication industry
- **A transition for microprocessor based systems**
  - ✓ Microwave theory/physics challenges dominate
  - ✓ Two PLLs communicating directly

# PHY Layer Design Basics

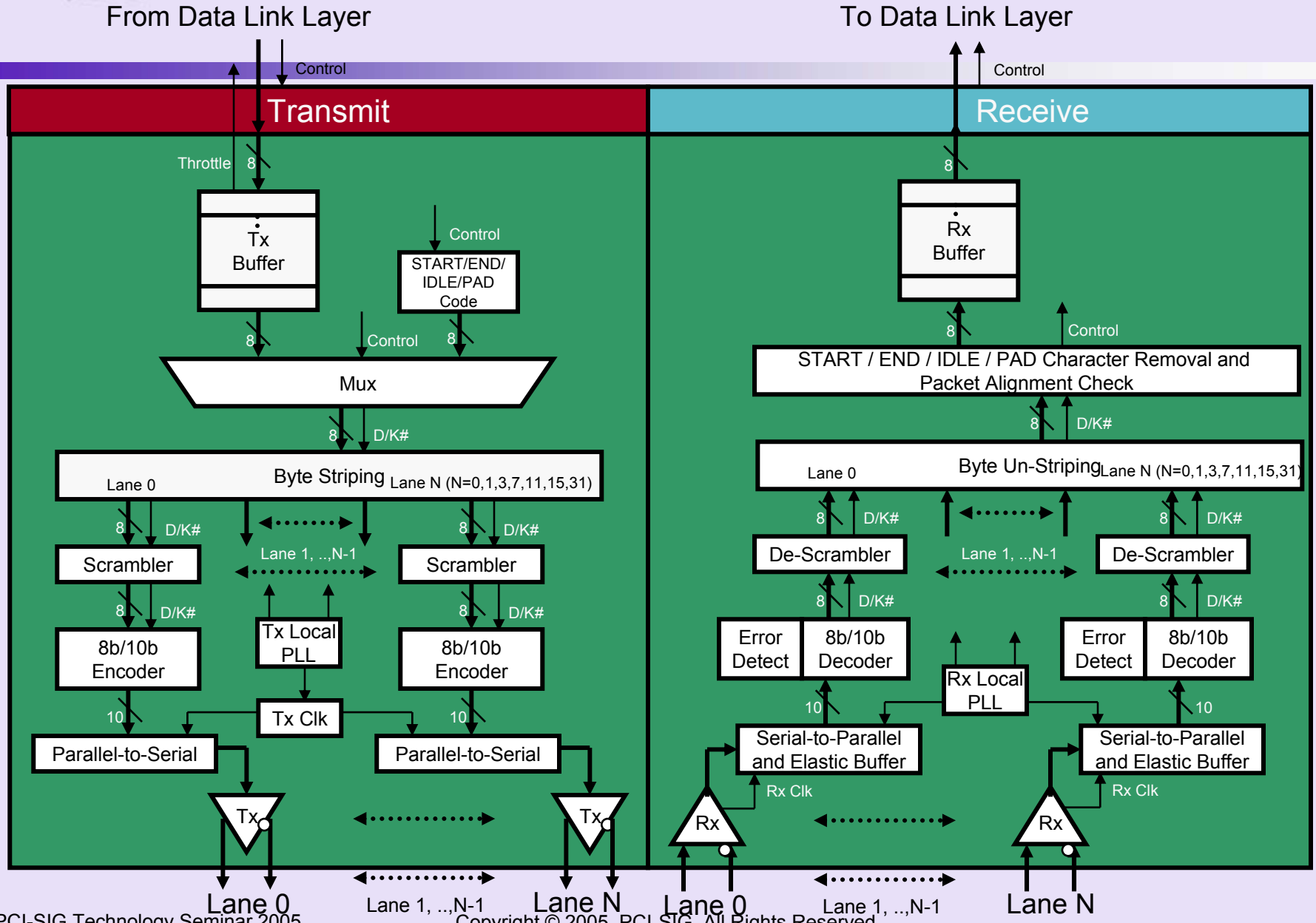



- **Logical Functions**
  - ✓ Encoding/decoding/scrambling
  - ✓ Reset, initialization, de-skew
  - ✓ Built in test modes
  - ✓ Configuration:
    - Speed, link width, lane mapping, Polarity
  - ✓ Link power management

- **Electrical Functions**
  - ✓ Transmitter/receiver
  - ✓ Clocks/PLLs
  - ✓ Clock/data recovery

**PHY layer upgrades do NOT impact upper layers**

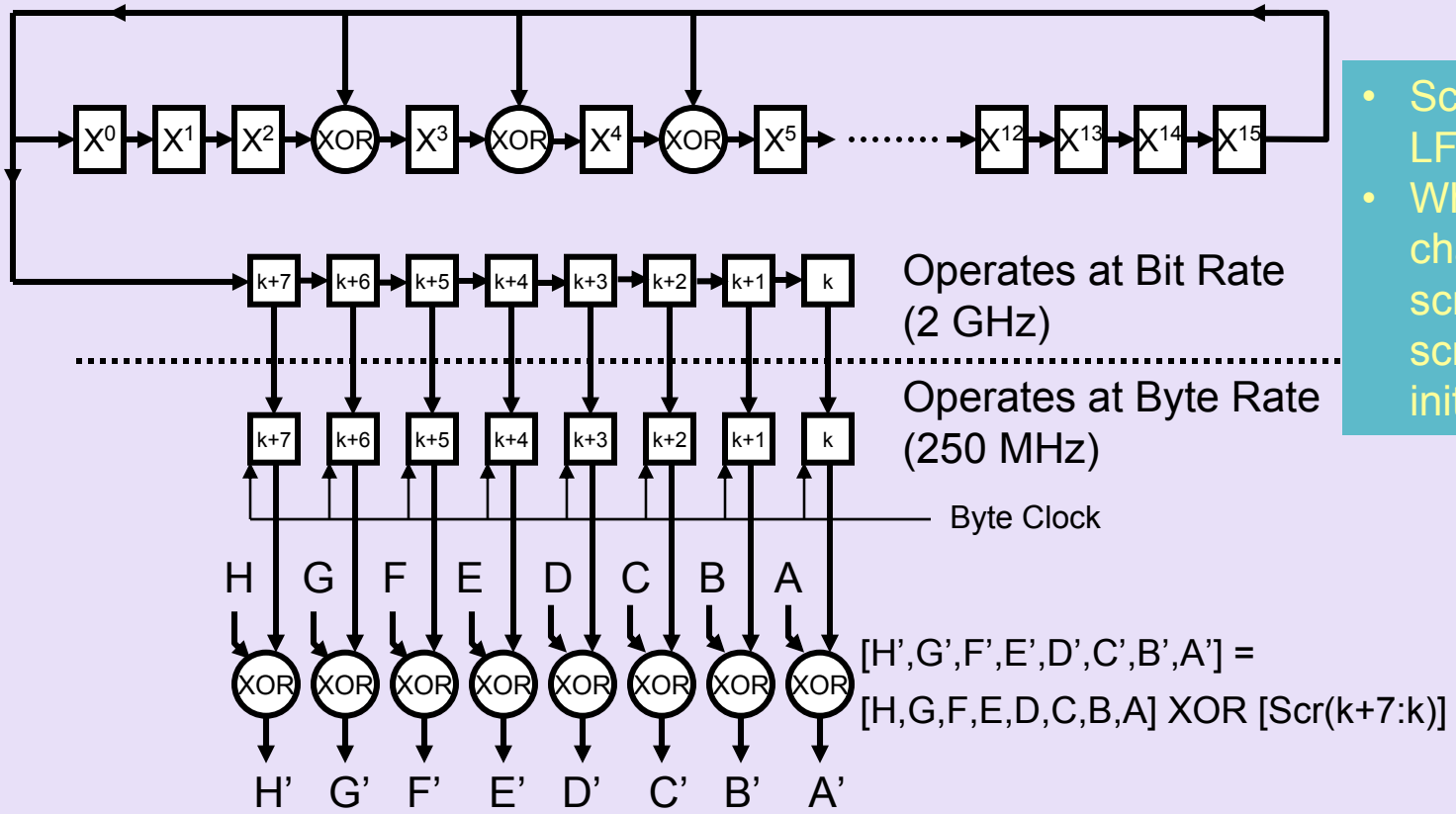
# Logical Physical Layer



# Scrambler Operation

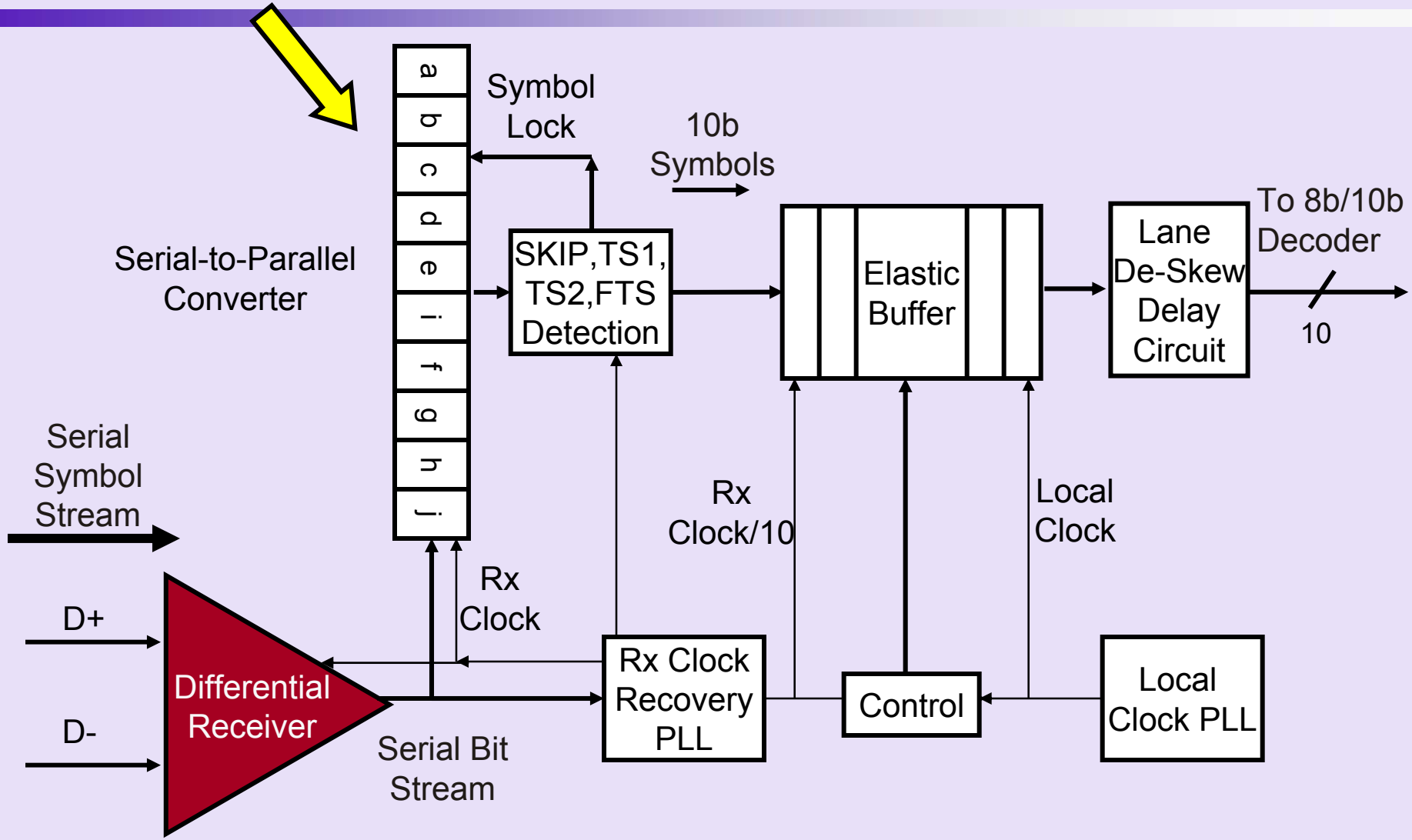
- Scrambling polynomial:

$$G(x) = X^{16}+X^5+X^4+X^3+1$$

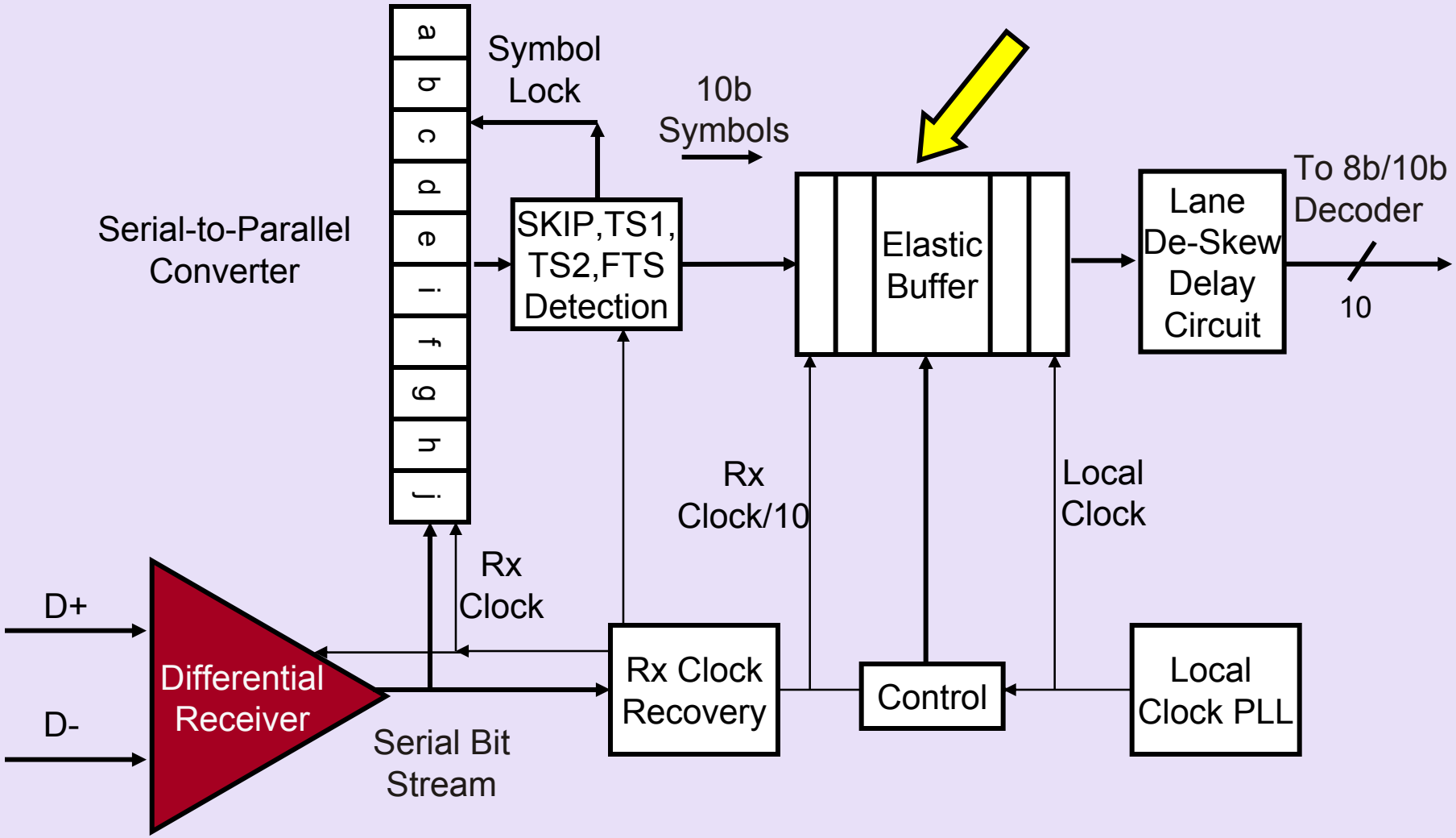



- Scrambler uses LFSR
- Whenever COM character exits scrambler, scramble is initialized

# Serial-to-Parallel Converter



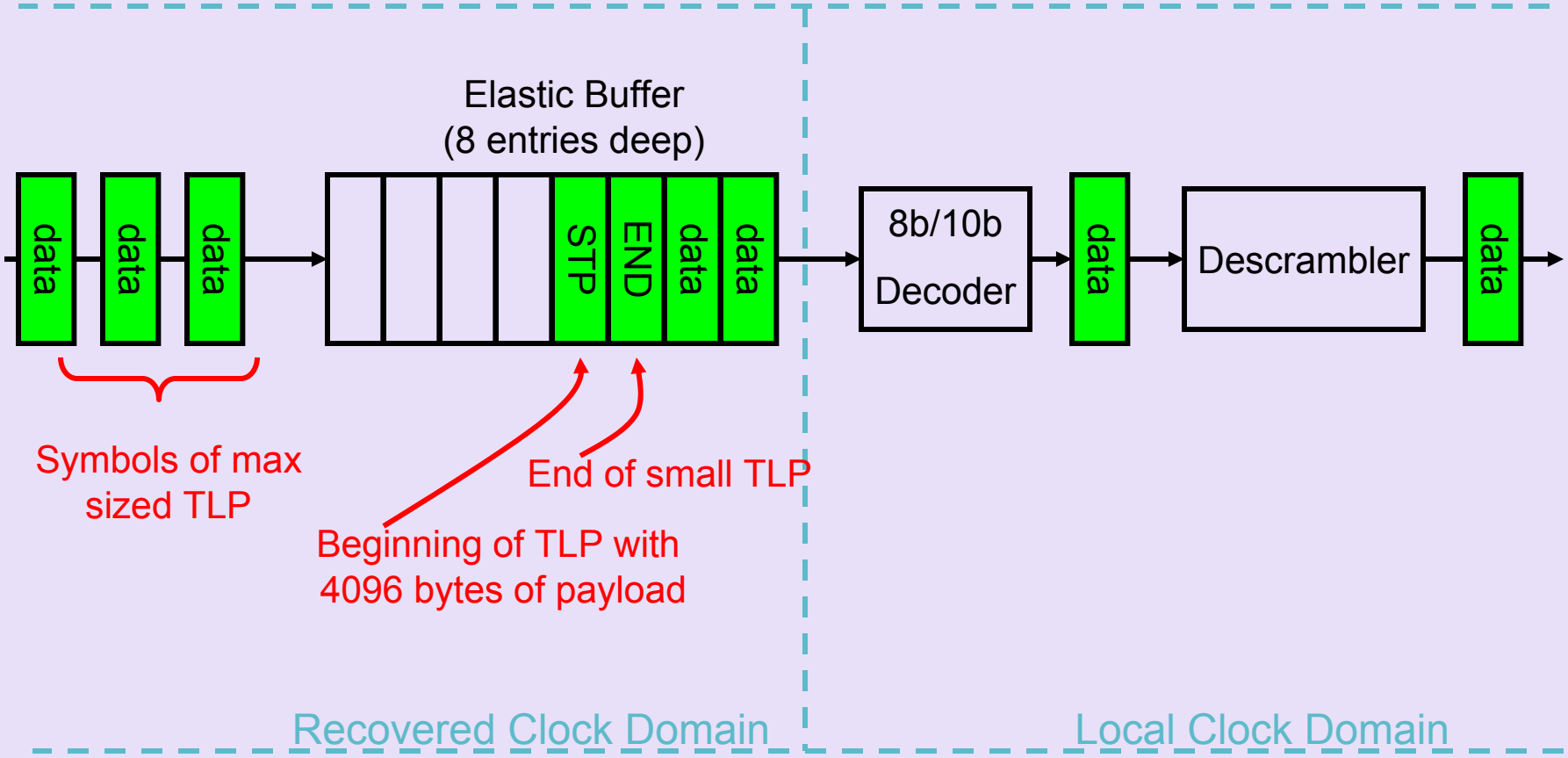
# Elastic Buffer



# Clock Tolerance Compensation

- Skip ordered-set used to compensate for differences in frequency of bit rate a packet is transmitted with, and the receiver clock frequency
- Frequency difference no greater than 600 ppm
- Skip ordered-set scheduled to be inserted every 1180 to 1538 symbol times and transmitted on a packet boundary.

# Elastic Buffer Option 1, Example 1: Local Clock Faster than Recovered Clock



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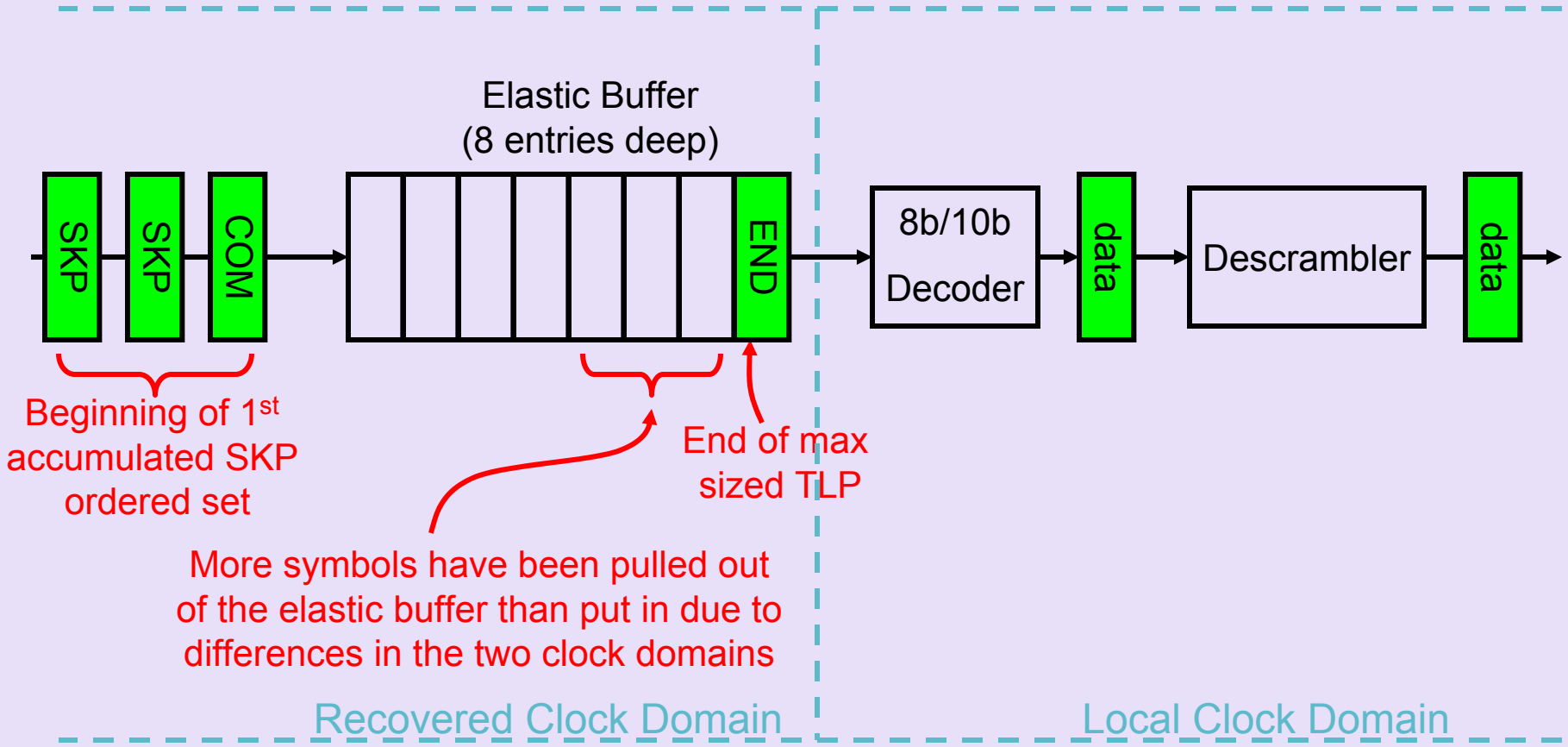

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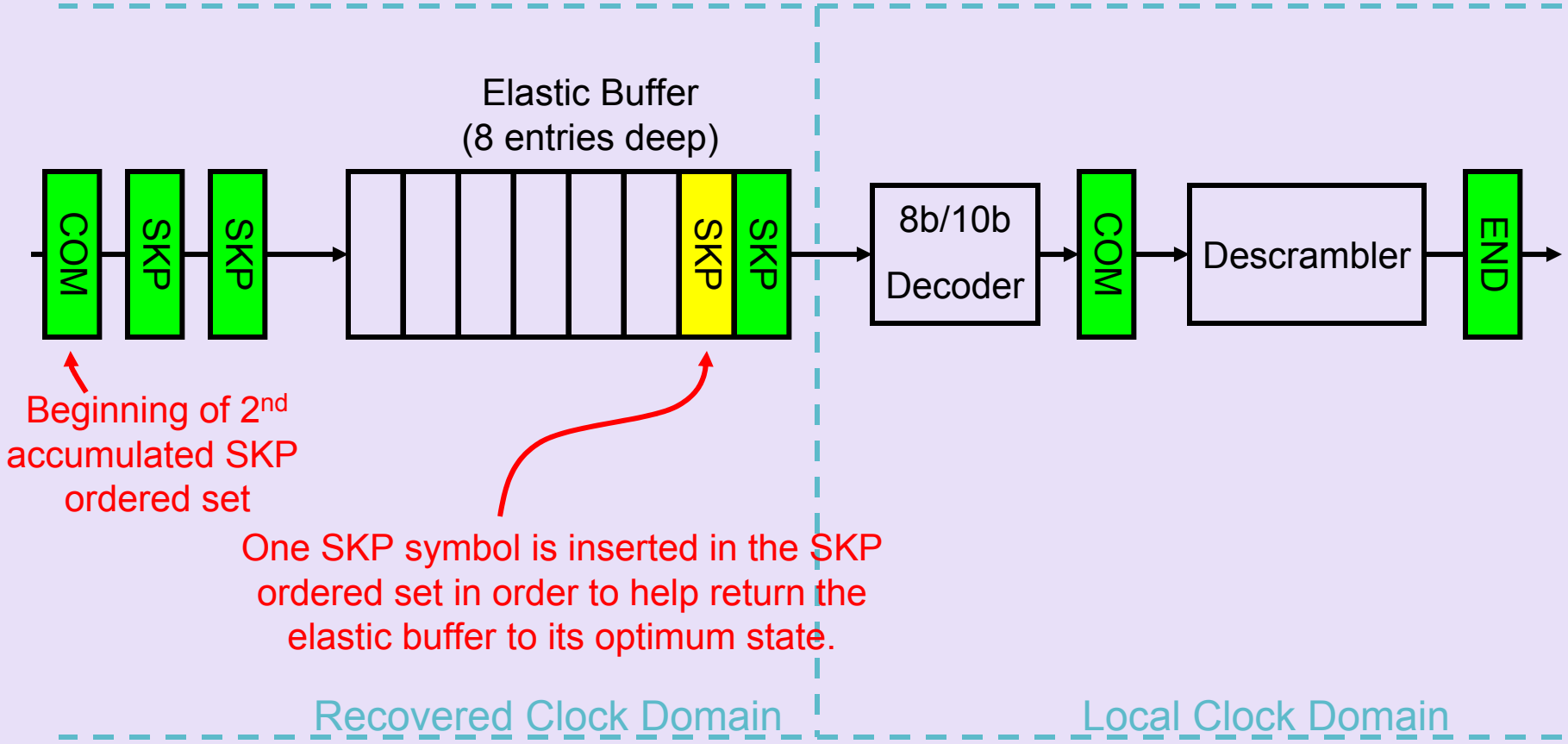

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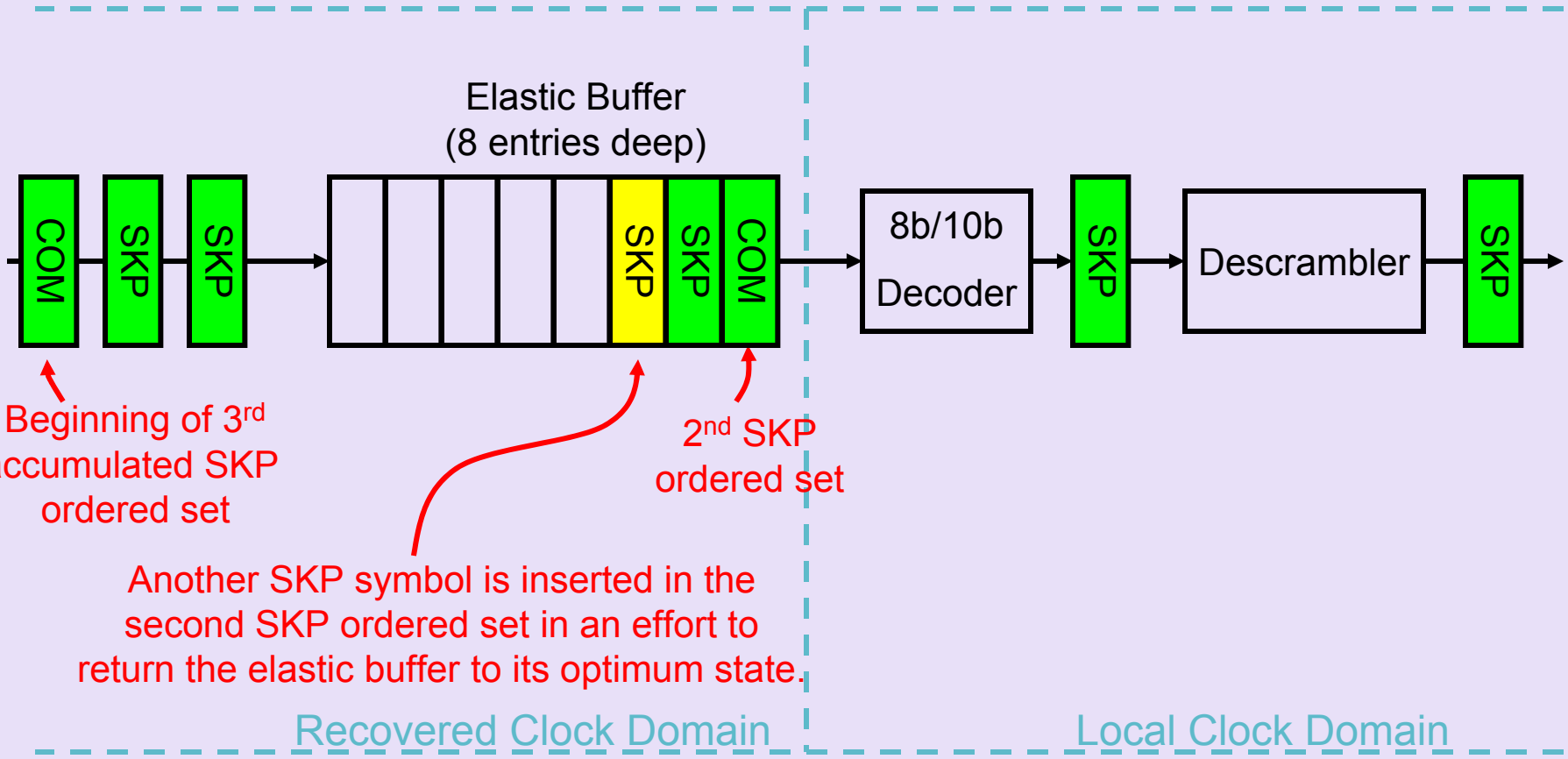

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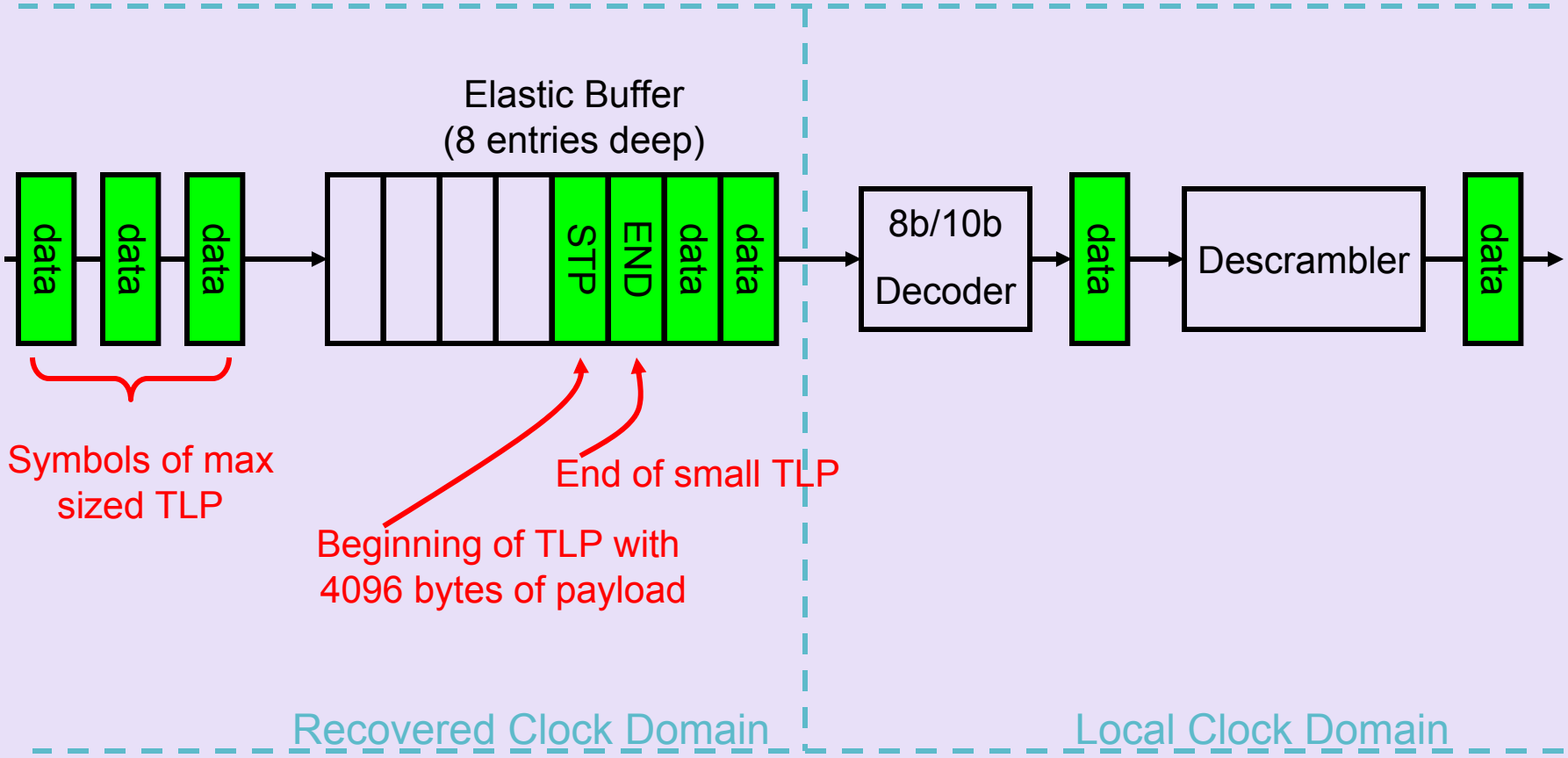

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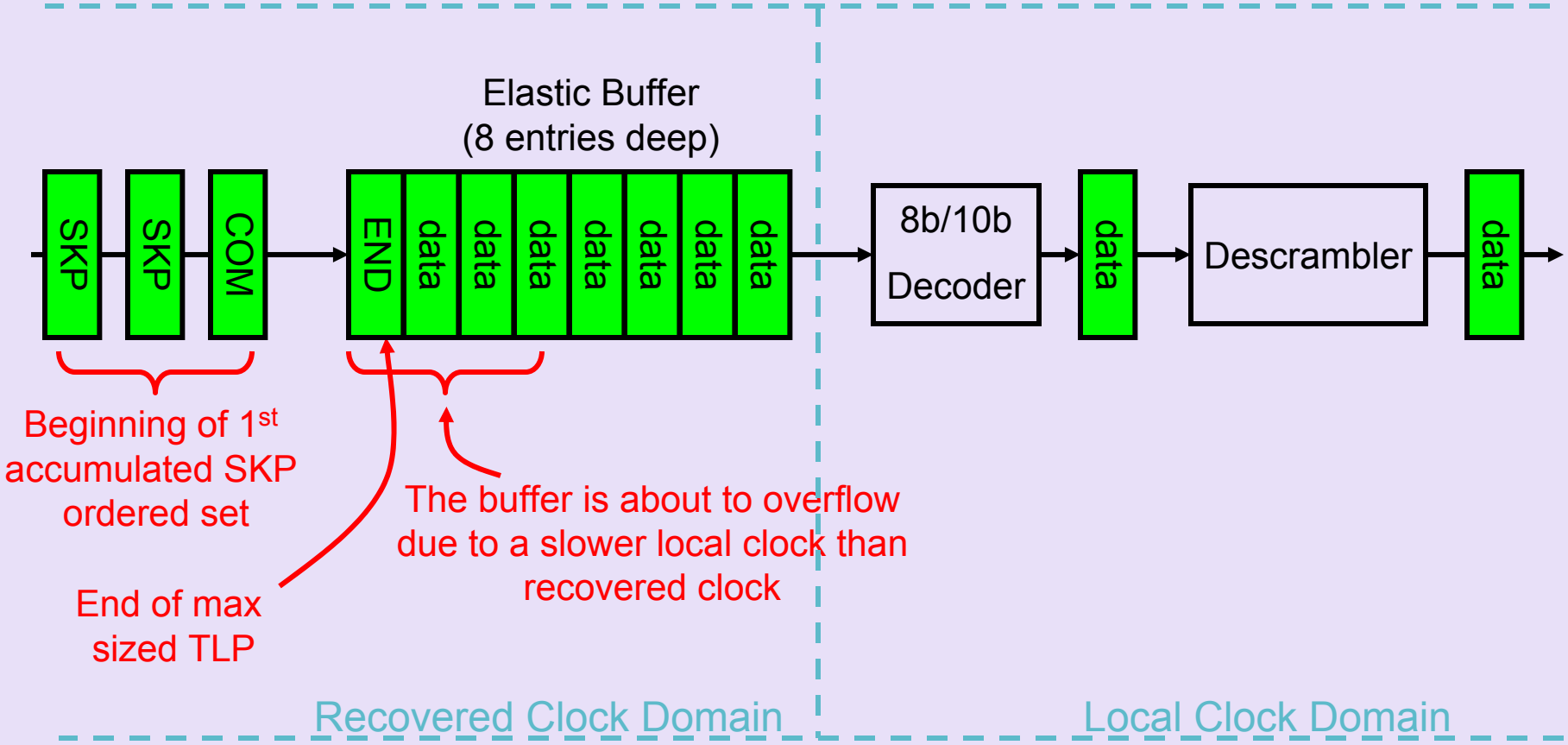

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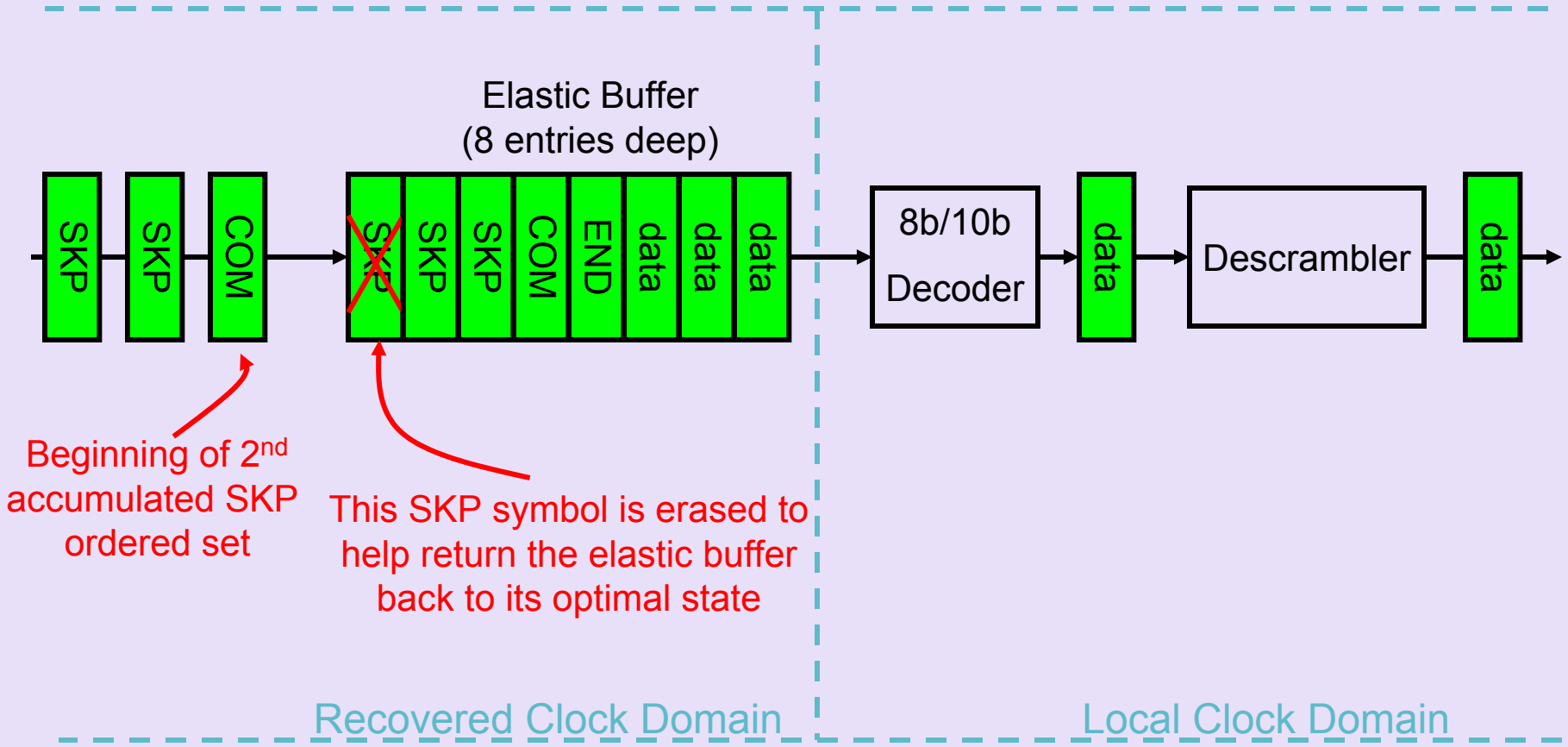

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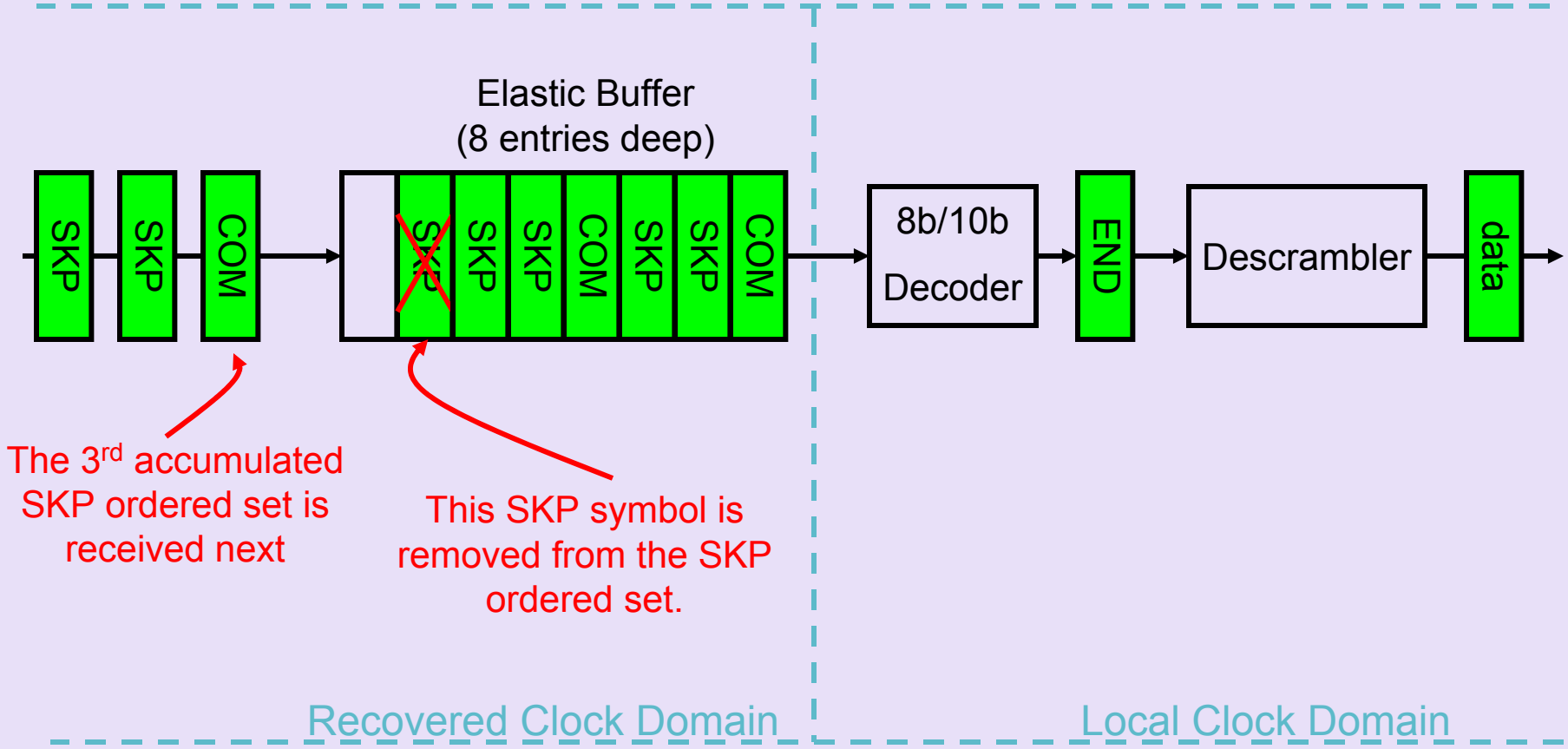

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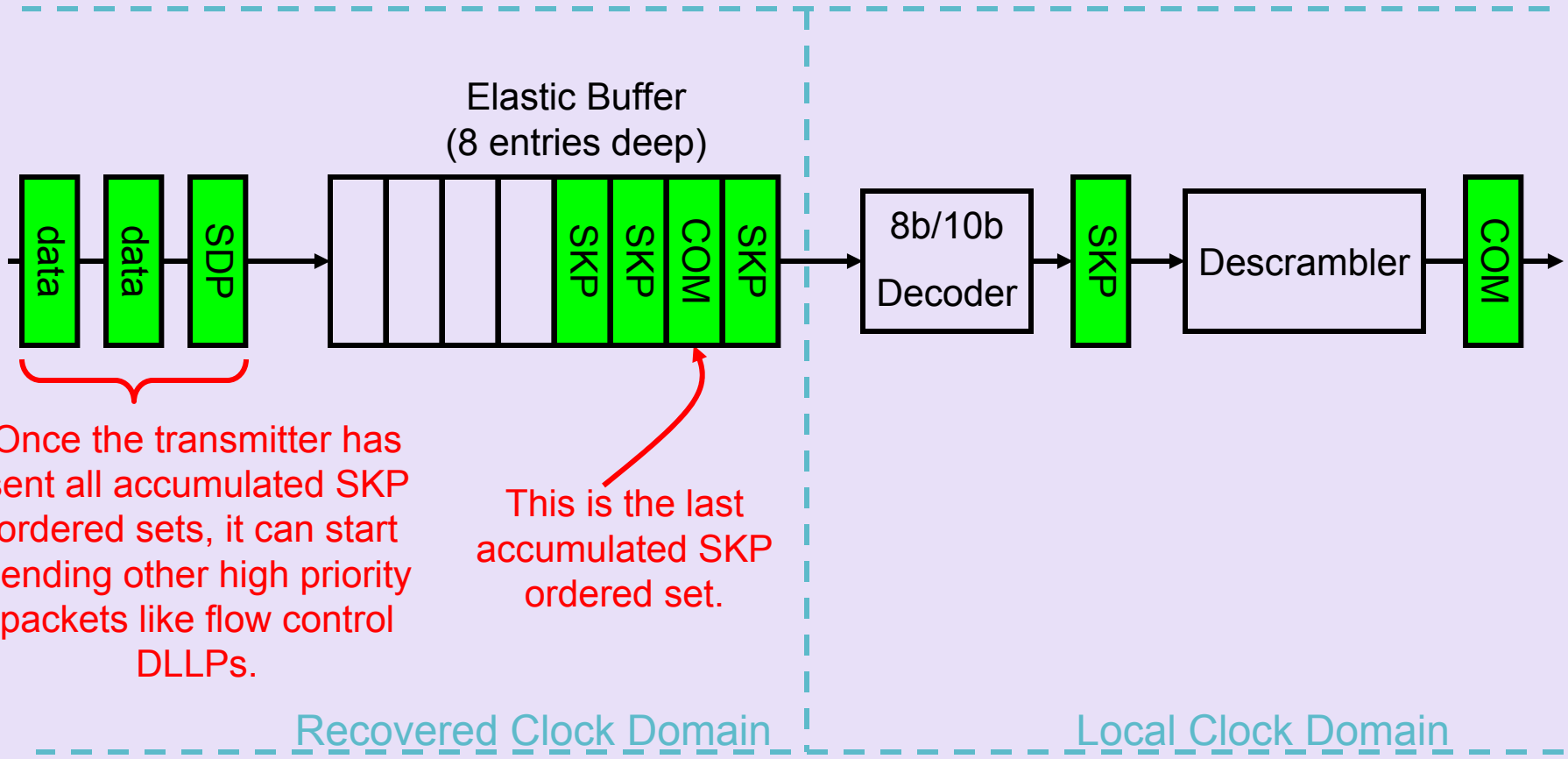
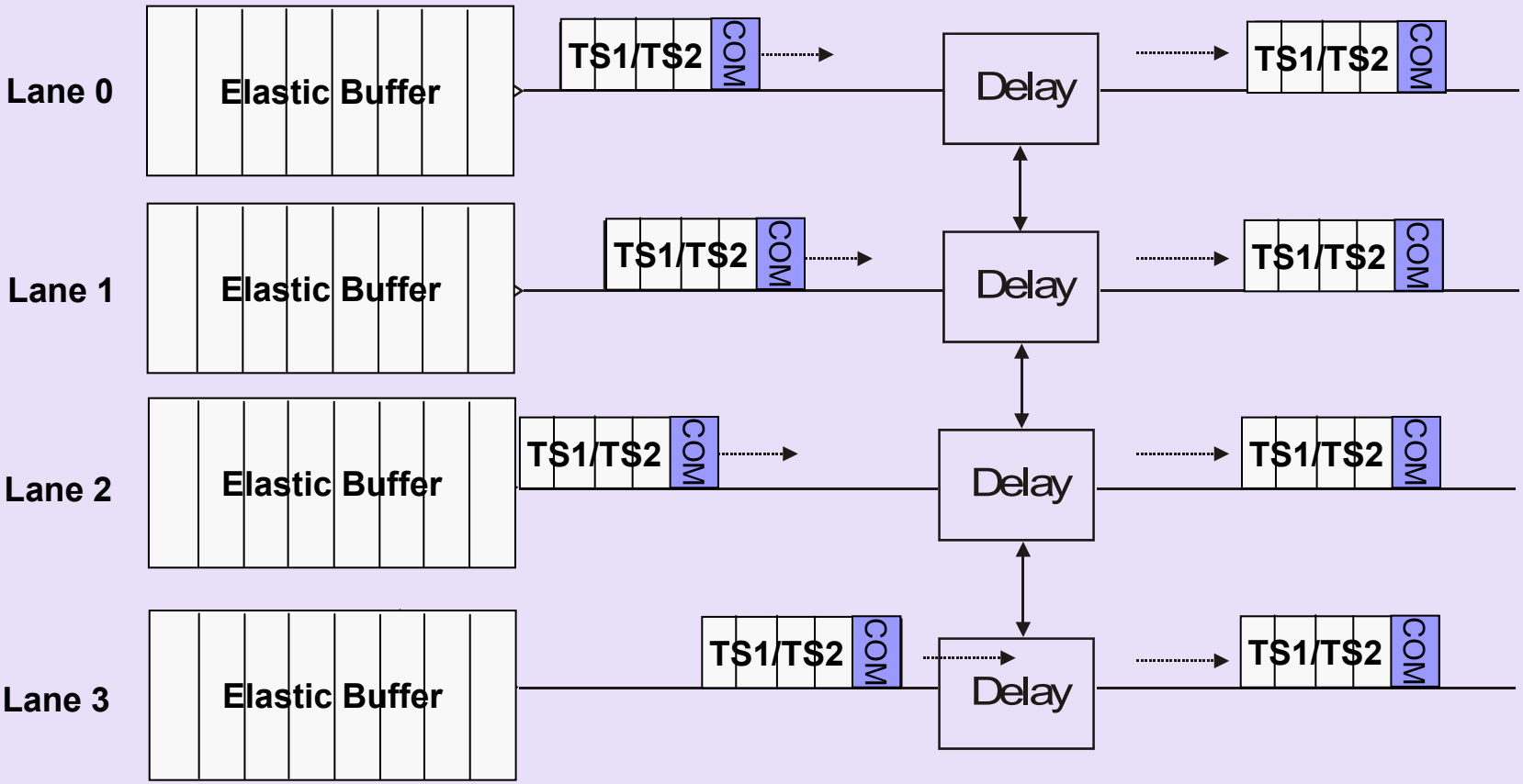


# Receiver Link De-Skew



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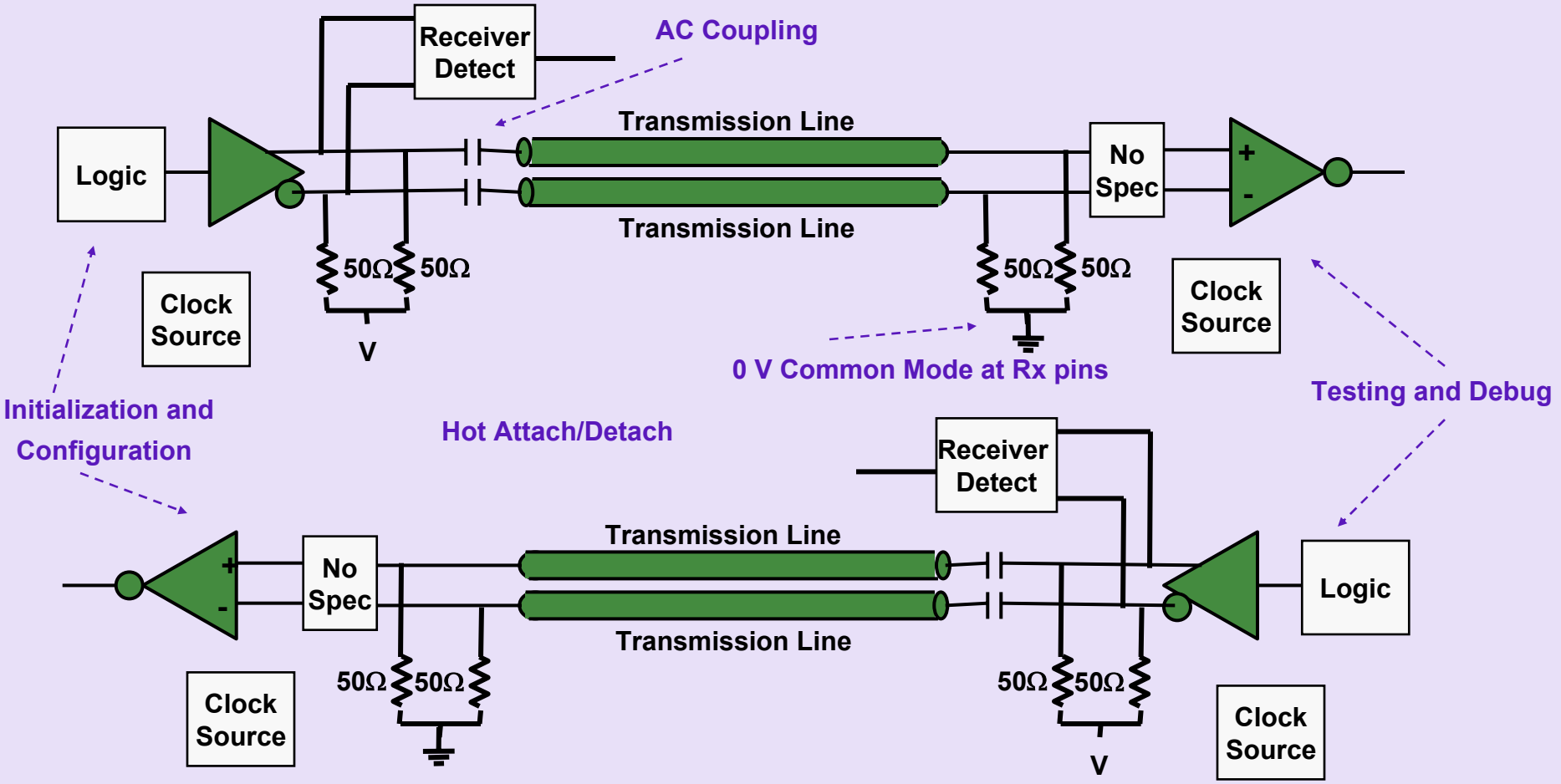
- Logical Physical Layer
- Electrical Physical Layer
- Link Training and Initialization (LTSSM)
- Layout Considerations

# Pictorial Summary

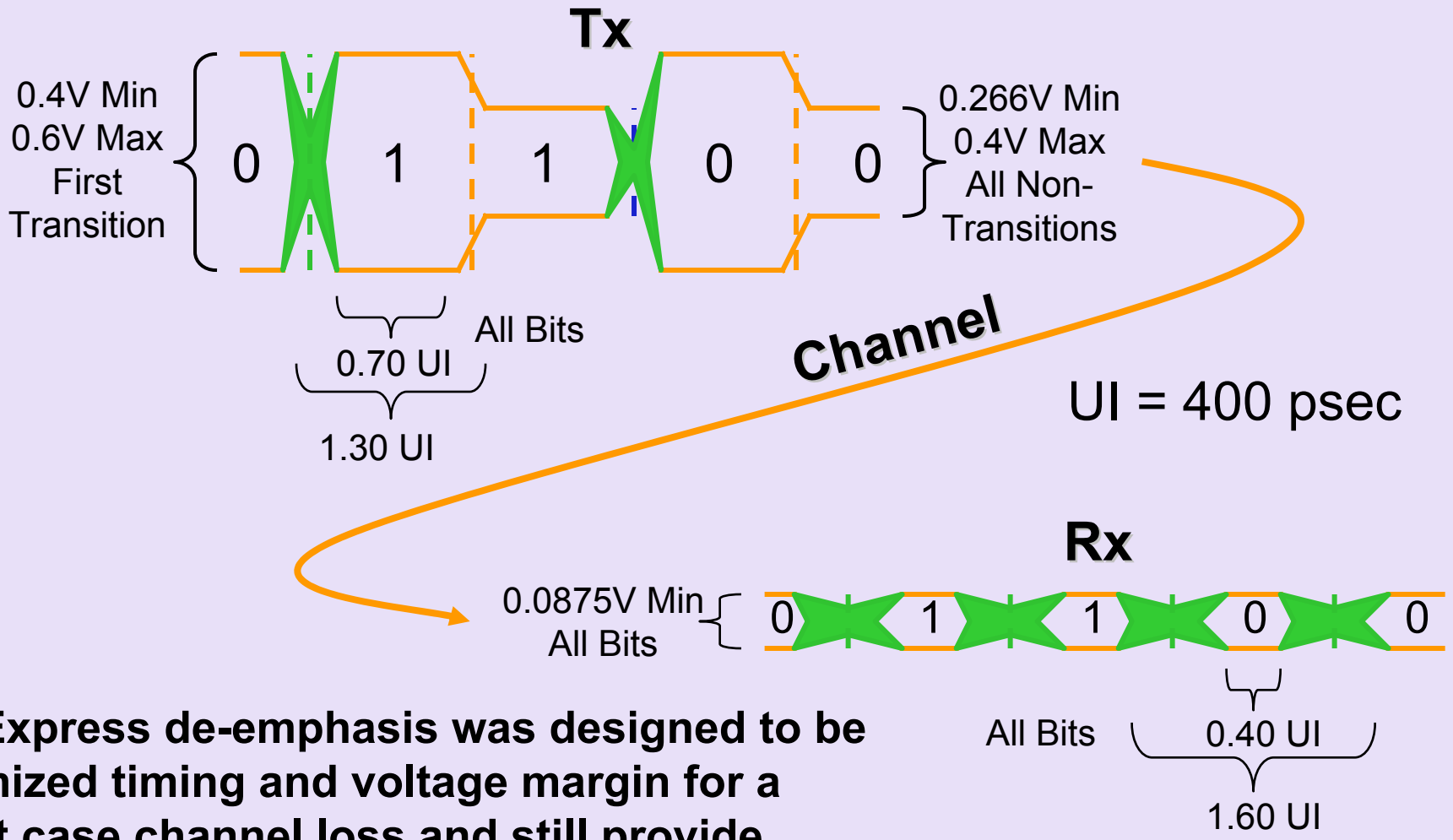



Emphasis on Low Power

ESD, EMI, Noise Suppression

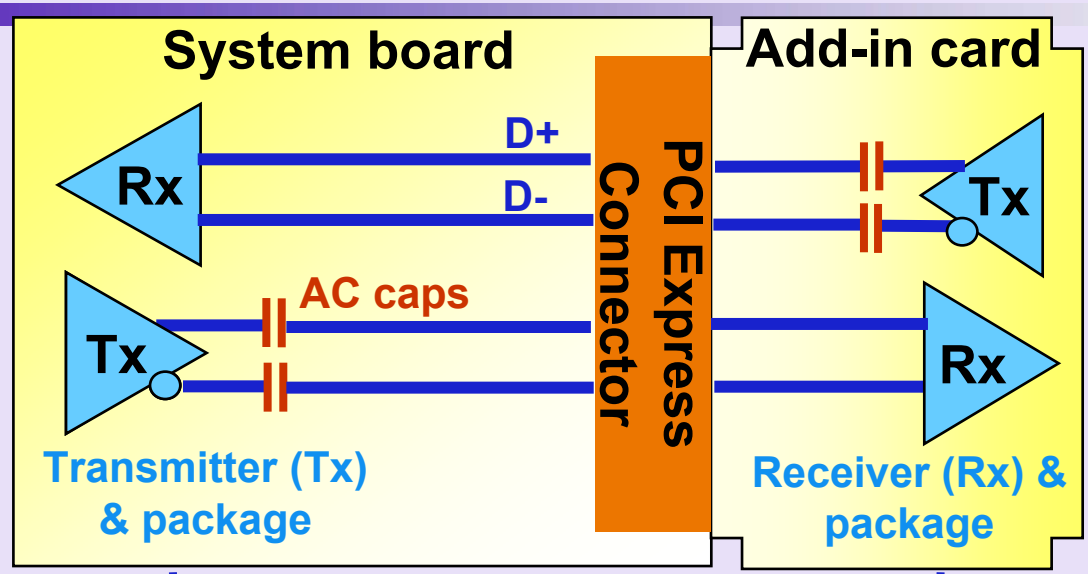
Error Behavior/Recovery

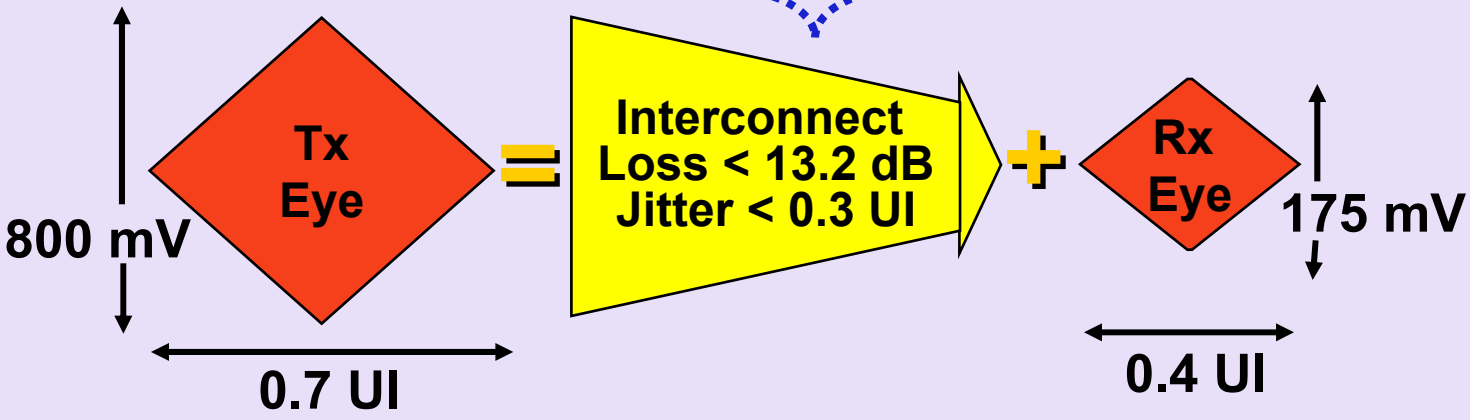
# Electrical Specifications




**PCI Express de-emphasis was designed to be optimized timing and voltage margin for a worst case channel loss and still provide adequate margin for the best case channel loss**

# System Budget



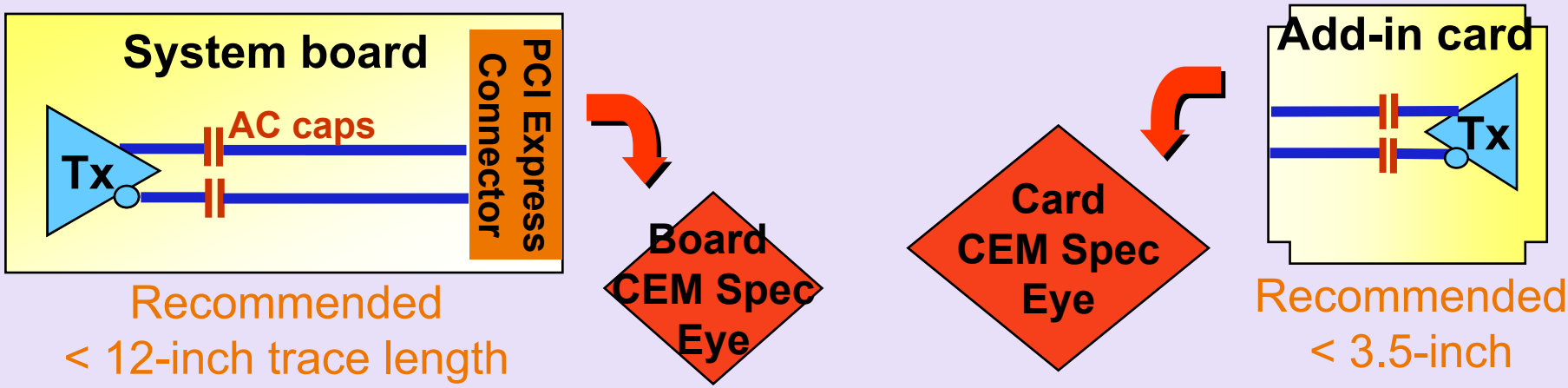




- ✓ Differential pairs
- ✓ AC coupled
- ✓ Lane-to-lane de-skew
- ✓ Polarity inversion
- ✓ On-chip equalization
- ✓ On-chip terminations

*UI = Unit Interval as defined in the PCI Express Base 1.0a Specification*

# Card Electromechanical Interconnect Budget

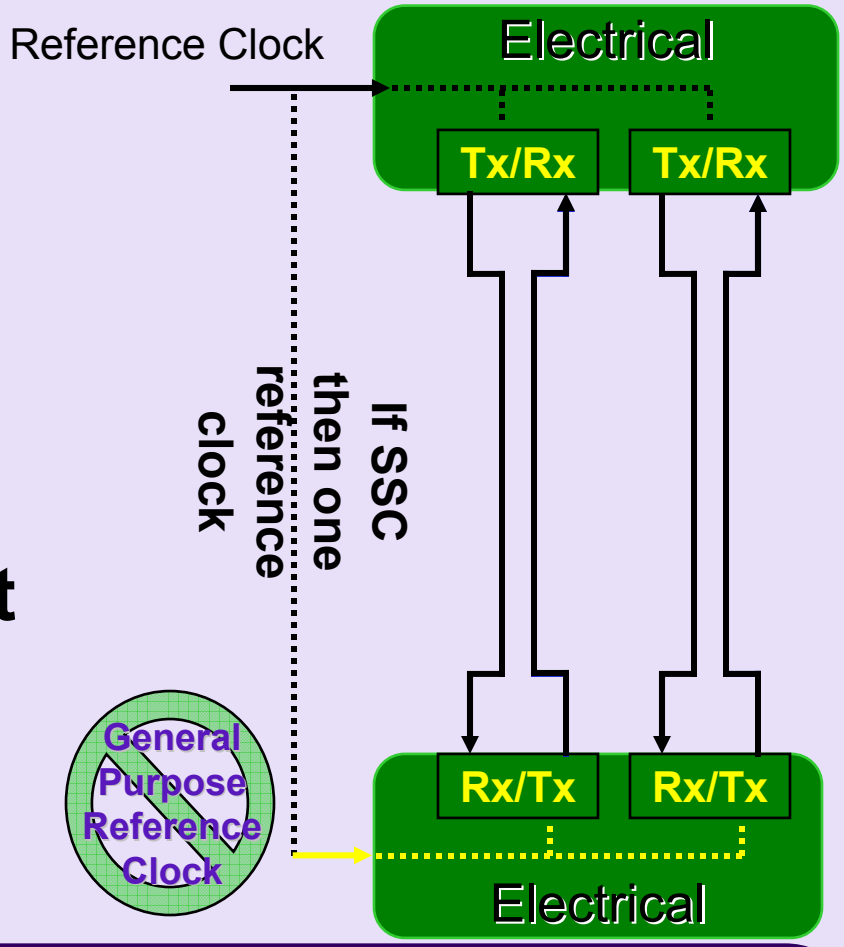
- **Card Electromechanical (CEM) 1.0a specification defines budget allocation**
  - ✓ *Loss* and *jitter* are key parameters
  - ✓ Target impedance not as critical
  - ✓ Maintain differential pair symmetry
  - ✓ Design tradeoffs: loss vs. trace length, etc.




**Manage loss & jitter to meet budget**

# Clocking Options

- **All lanes within a port must transmit data using one frequency**
- **The ports at each end of a link may transmit data at slightly different frequencies**
  - ✓ Tolerance = ±300 ppm each

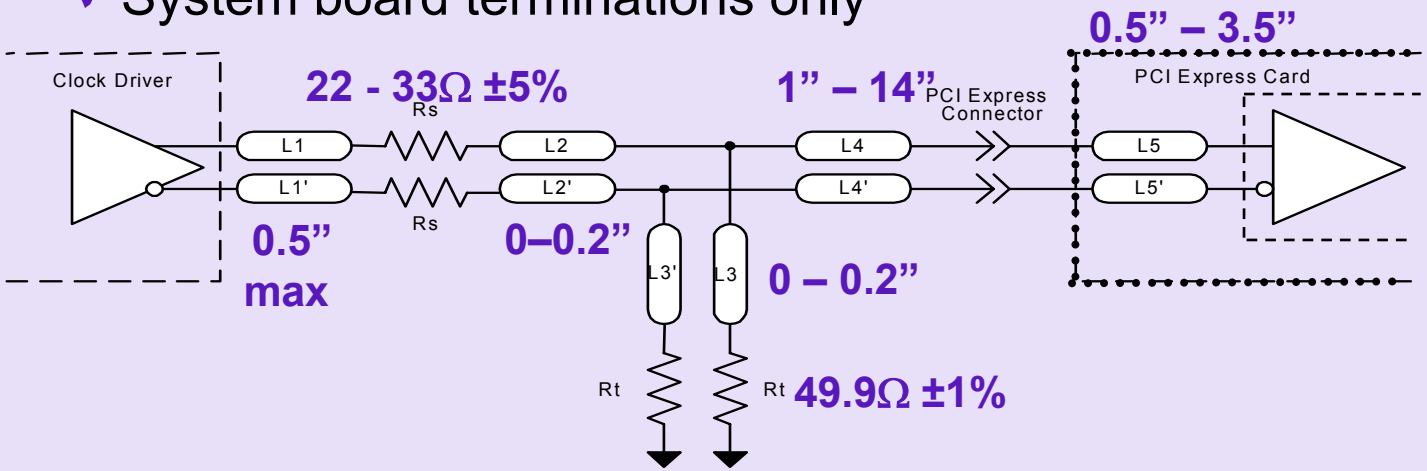



**If SSC used to modulate data rate, then both ports must use same modulated clock source**

# Reference Clock Routing

- **Differential clock routing to each device and connector**
  - ✓ Use the same differential trace geometries
  - ✓ Length matching to different devices *NOT* required!

- **Clock driver requirements**
  - ✓ 100MHz with SSC support (e.g. CK410)
  - ✓ Choose low jitter components
  - ✓ System board terminations only



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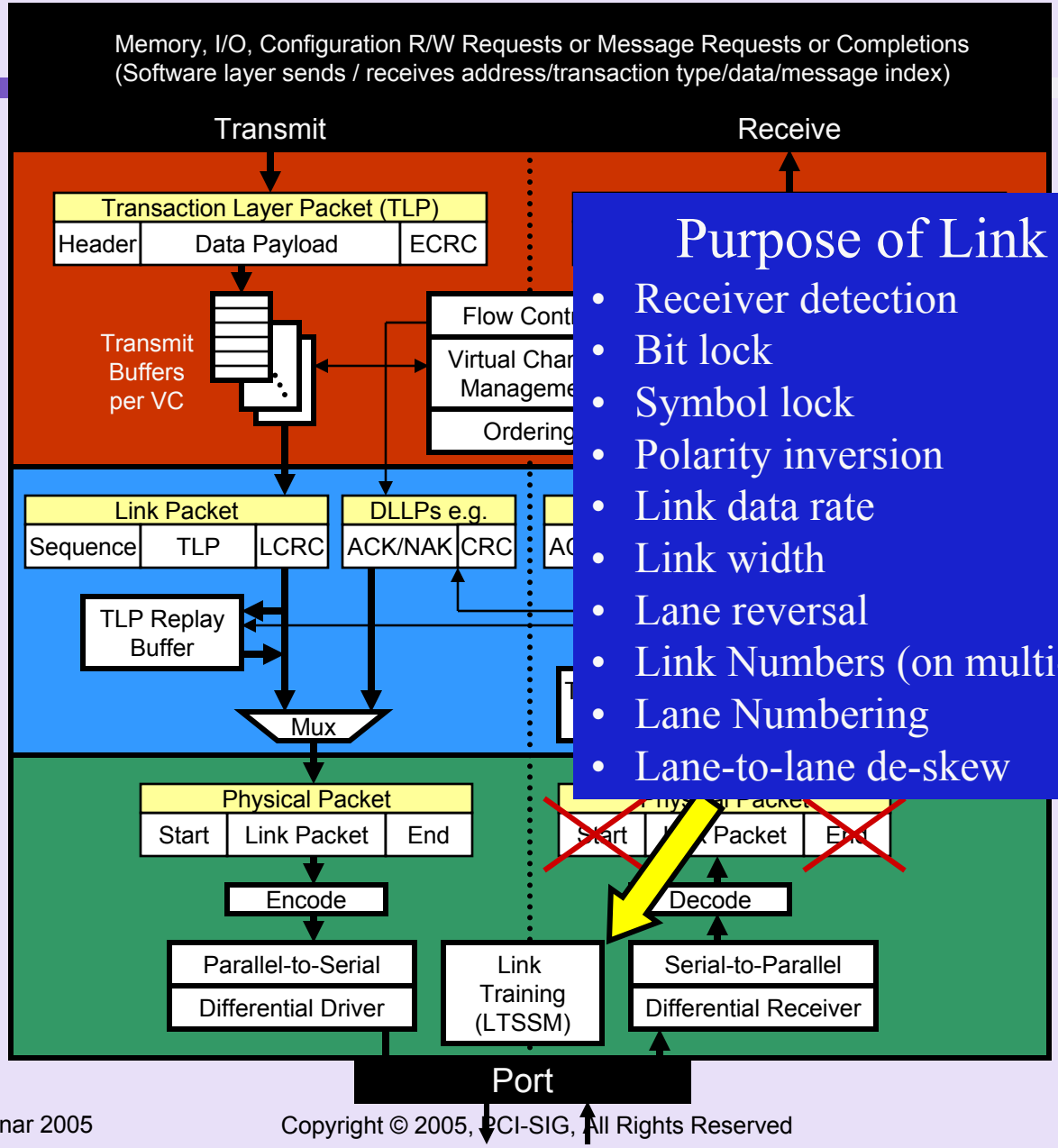
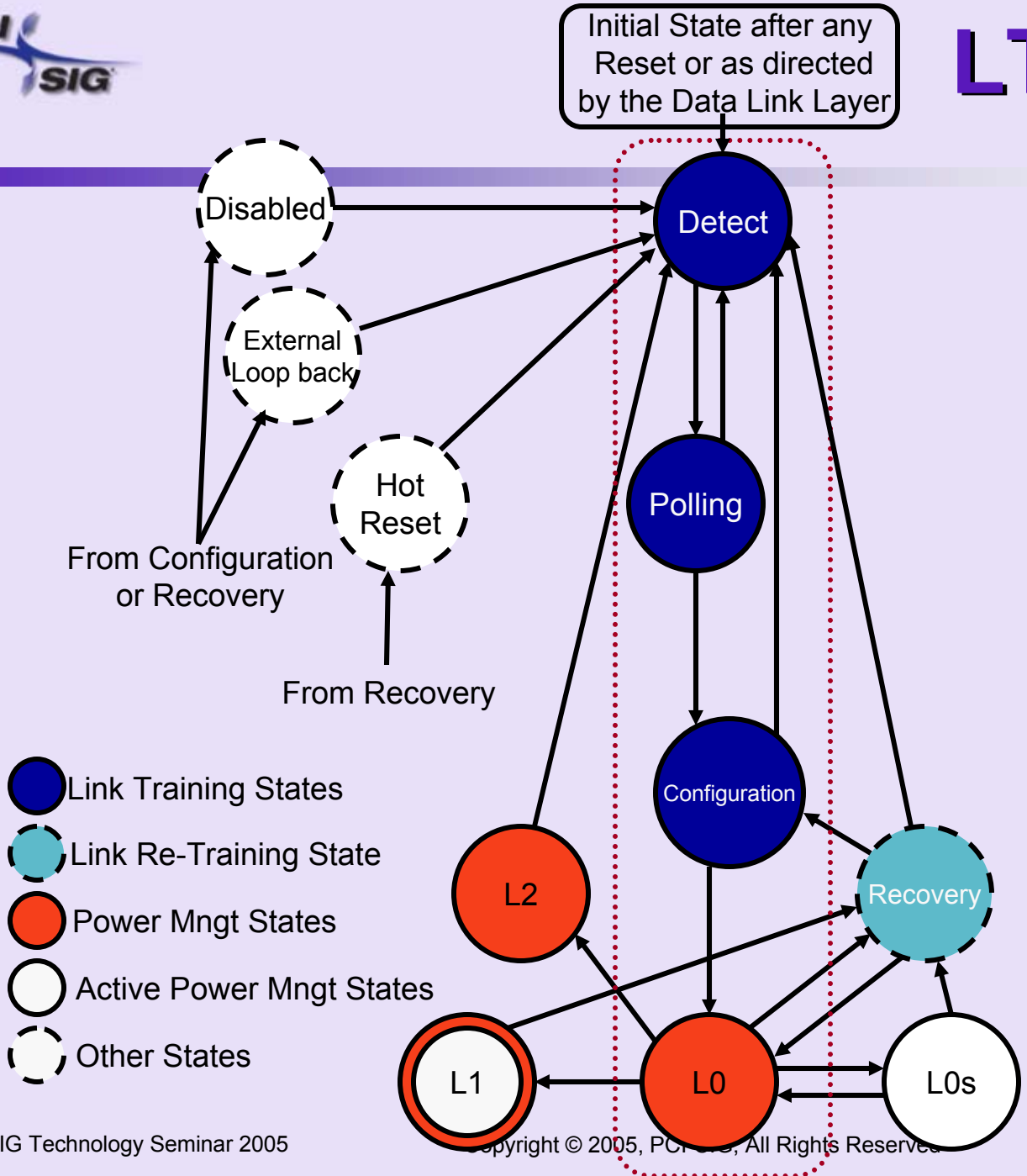
# Link Initialization and Training




## Purpose of Link Training

- Receiver detection
- Bit lock
- Symbol lock
- Polarity inversion
- Link data rate
- Link width
- Lane reversal
- Link Numbers (on multi-Link device)
- Lane Numbering
- Lane-to-lane de-skew

# LTSSM



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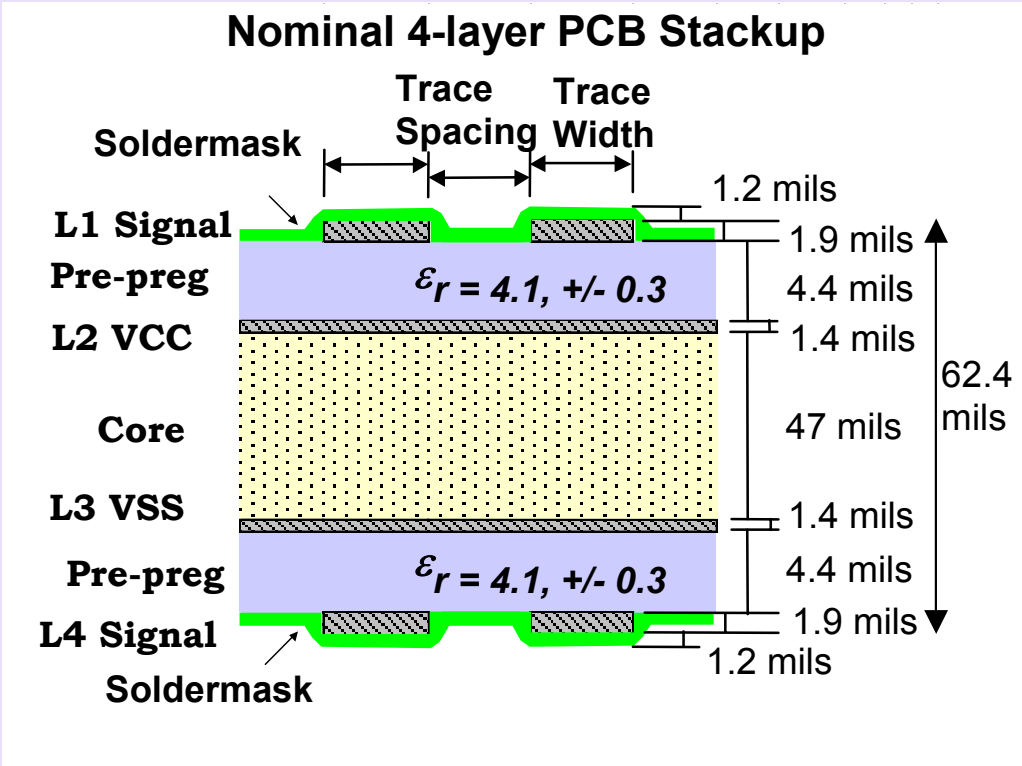
# Stackup design

- No new PCB technology required
- Standard 4-layer stackup 0.062” thick PCB
- Microstrip ½ oz Cu plated Ok
- Stripline 1 oz Cu (6+ layers) Better



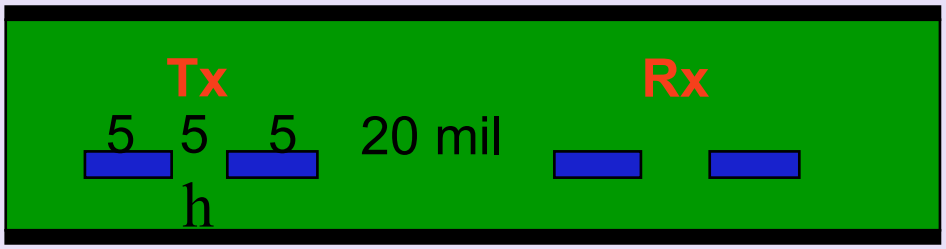

**Follow simple layout rules & design tradeoffs**

# Trace Geometry & Impedance

- Use wider trace width ⇒ Minimize loss
- Use wider traces for long routes
- More pair-to-pair spacing ⇒ Minimize crosstalk
- Target differential $Z_o$ of 100 Ω ±20%


Microstrip

Non-interleaved Topology example

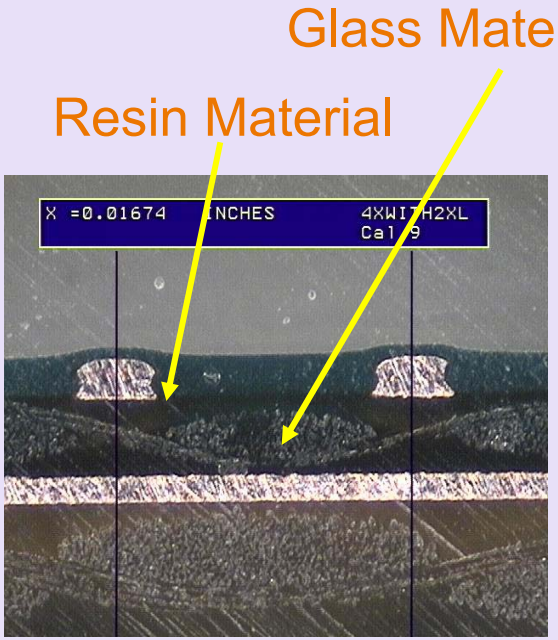



Stripline

Interleaved Topology example

# PCB material dominates loss

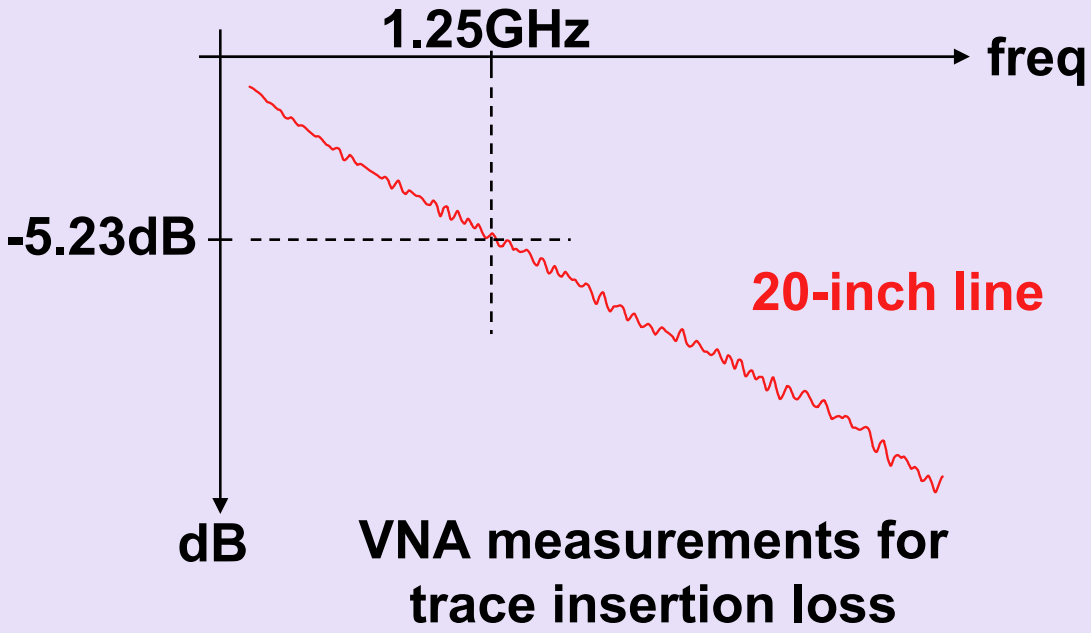
- Stackup FR4 material
  - ✓Copper roughness ⇒ loss ↑
  - ✓Thinner dielectrics ⇒ loss ↑
- Non-homogeneous dielectric
  - ✓Localized Zo variation due to material weave ⇒ loss ↑
- Wide differential Impedance variation on μstrip
  - ✓Etching and Plating process ⇒ loss ↑




FR4 cross-section

# Trace length

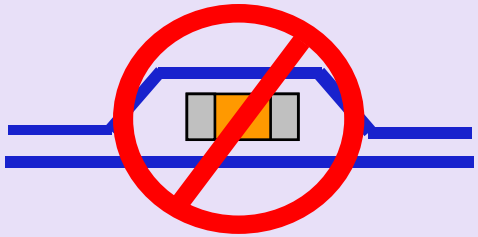
- Longer trace length ⇒ loss ↑
- 0.25 to 0.35 dB inherent loss per inch for FR4 microstrip traces
- Limit motherboard trace to < 12 inches and add-in card trace to < 3 inches

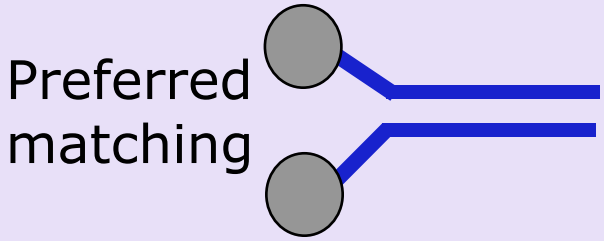


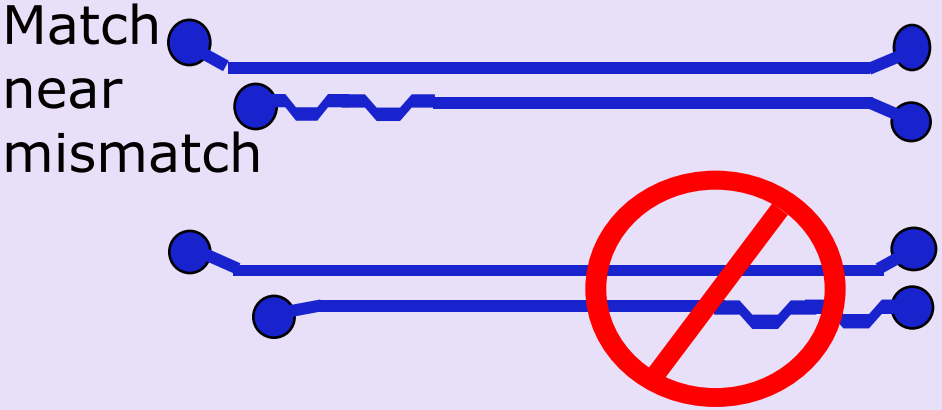

**Spec allows a loss of 13.2**

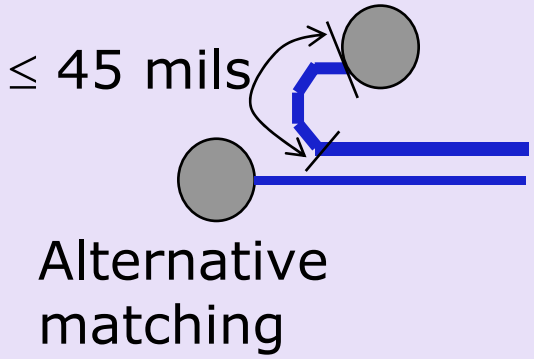
# Trace Symmetry & Matching

- Match each differential pair per segment
  - ✓ Match overall length ≤ 5 mils
  - ✓ Symmetric routing for each pair



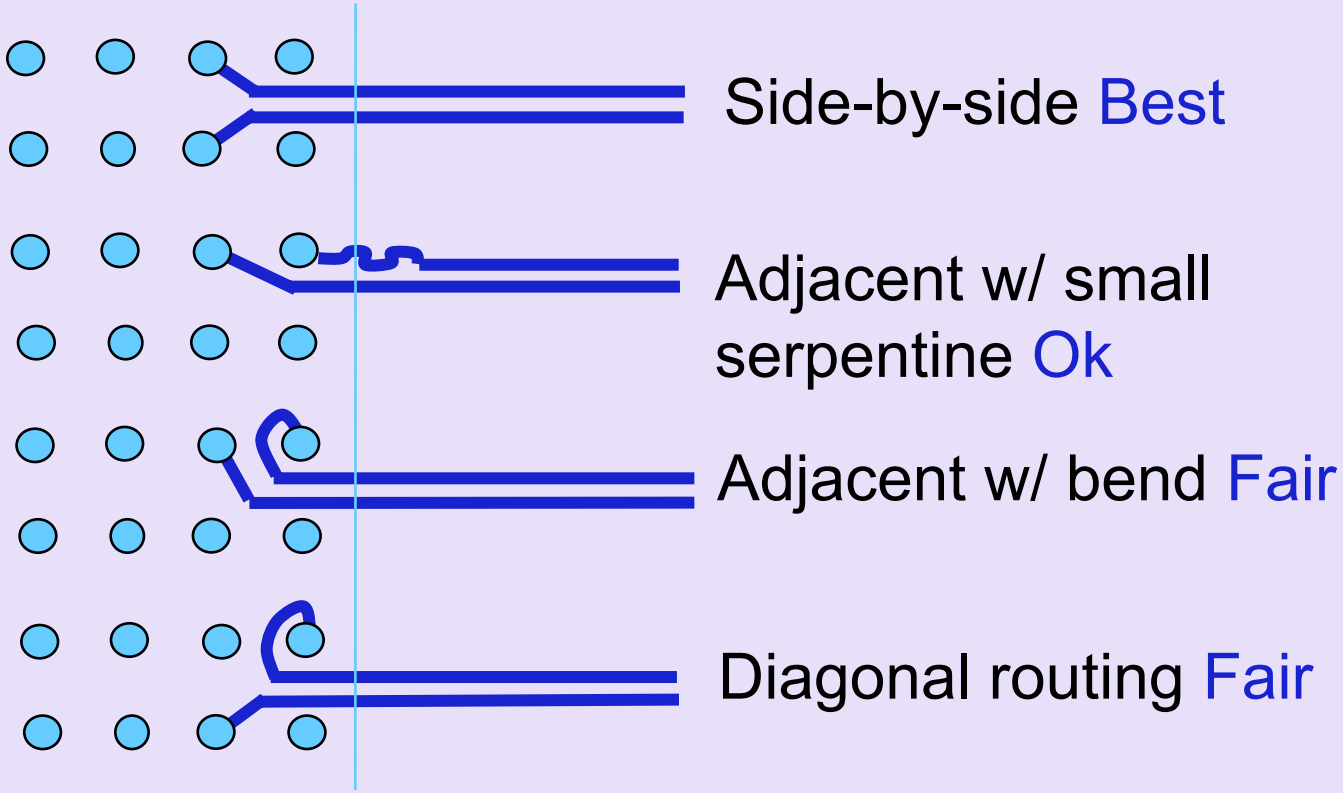


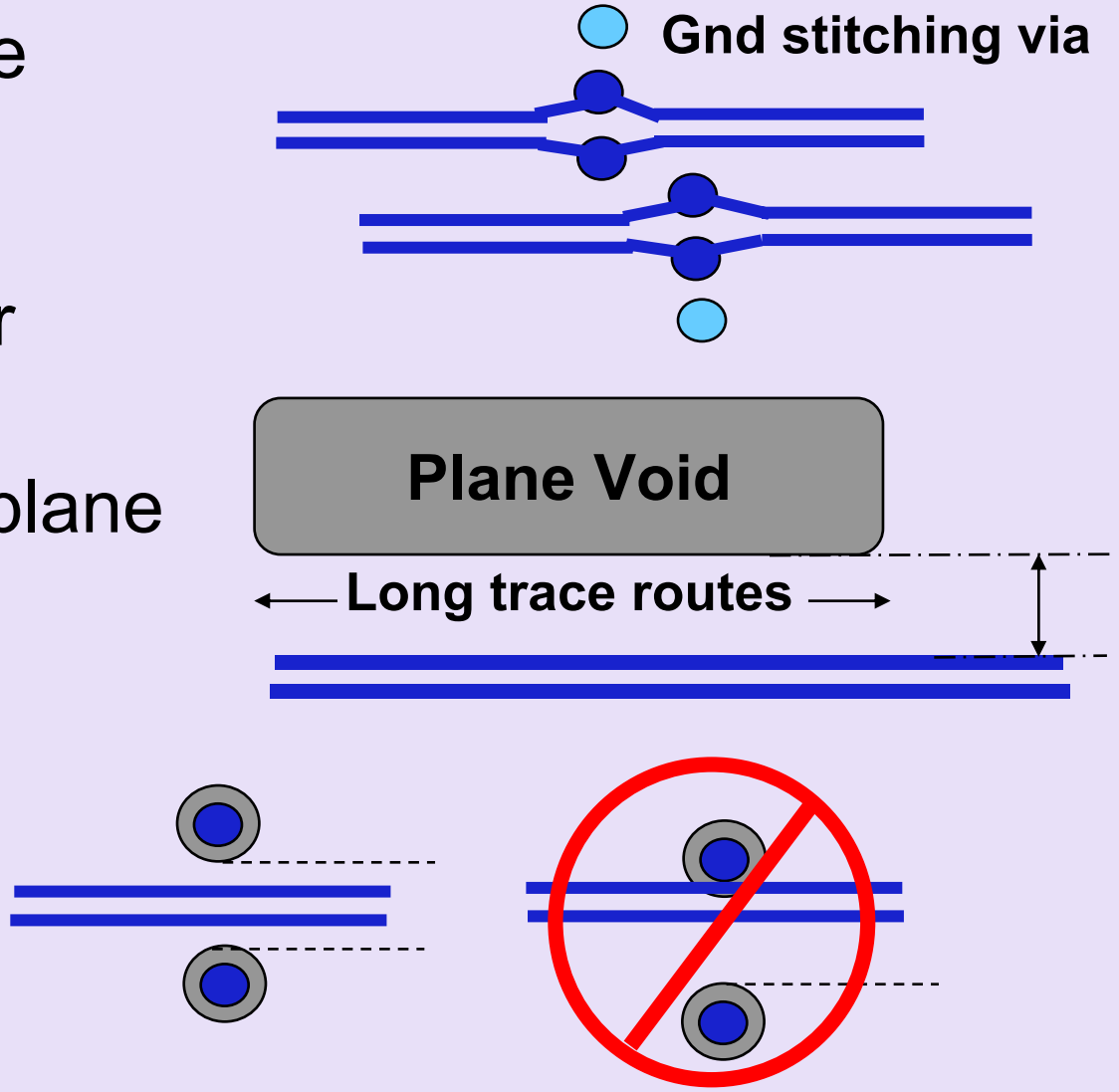
# Pin field breakout

- Use side-by-side breakout for package to maintain symmetry
- Avoid tight bends



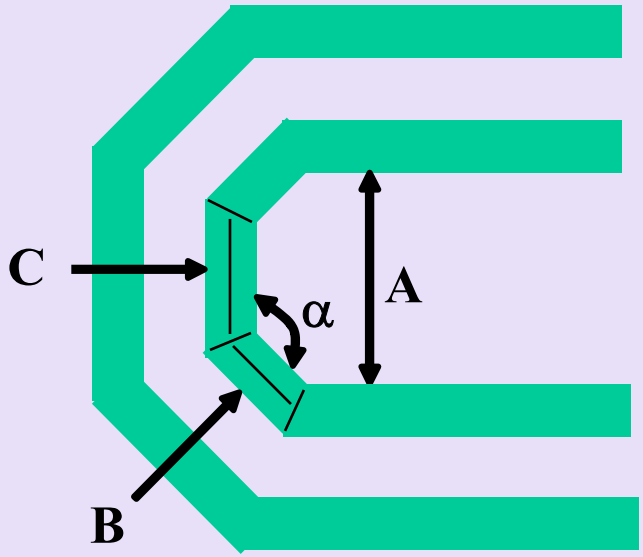
# Reference plane

- Full ground plane reference
- Stitching vias required for layer transition
- Clearance near plane void
- Avoid trace over anti-pad



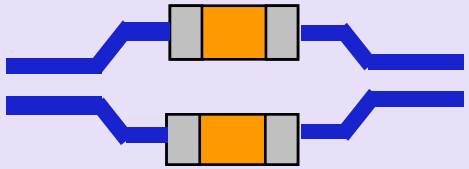
# Bend Guidelines

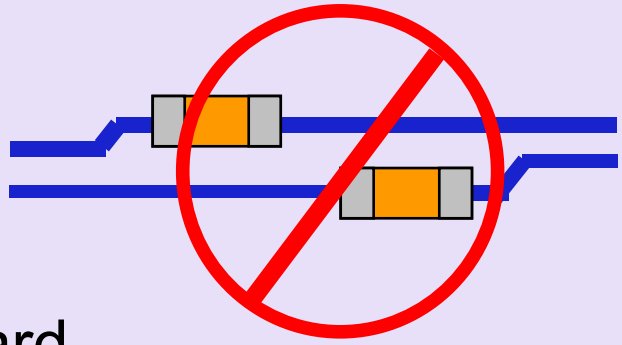
- Avoid tight bends
  - ✓ No 90° bends; impact to loss and jitter budgets
- Keep angles >= 135° (α)
- Keep minimum air gap
  - ✓ A >= 3x the trace width
- Length of B and C >= 1.5x the width of the trace



# AC coupling caps

- Size: 0402 best, 0603 ok
- No 0805 size or C-packs
- Symmetric placement

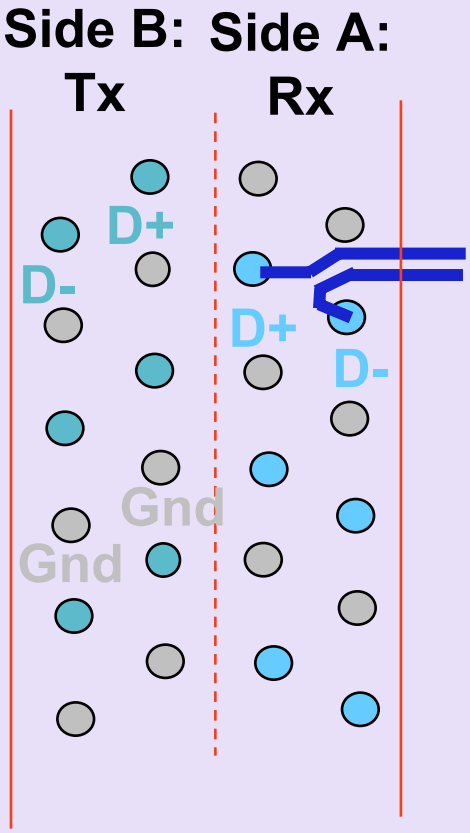




- Cap Size: 0.1uF best
- Cap location:
  - ✓ Along Tx pairs on Motherboard
  - ✓ Along Tx pairs on Add-in card

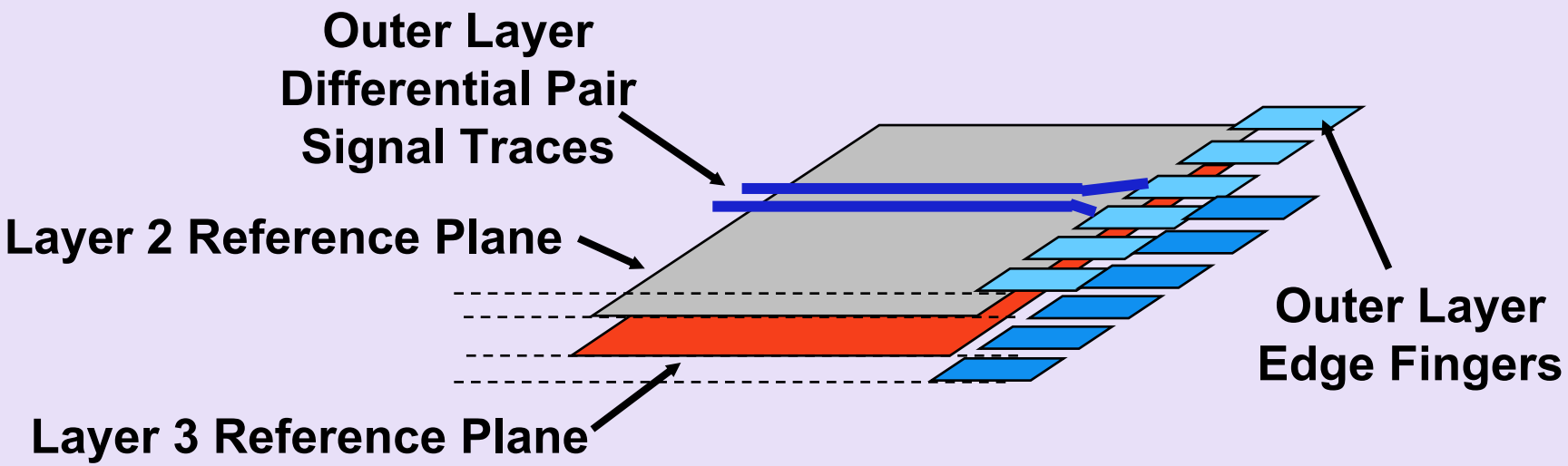
# Connectors

- New connector with standard PTH
- Pinout optimized for differential routing
- Loss & crosstalk part of baseboard budget
- Connector sizes: x1, x4, x8, x16



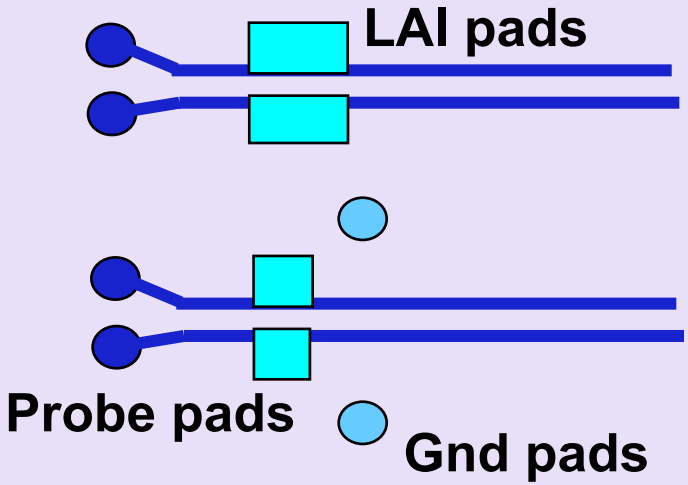
# Card edge fingers

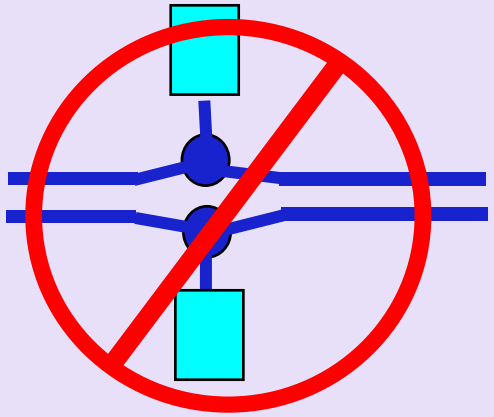
- Remove ref plane under edge fingers pads
  - ✓ For better impedance/loss performance



# Test points & Vias

- Minimize Vias usage
  - ✓ Up to 0.25 dB loss per via
  - ✓ Via pad size ≤ 25 mil, hole size ≤ 14 mil
- Put test points or LAI pads in series
  - ✓ No stubs
  - ✓ Provide Gnd pads for single-ended probing



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