PCI Express™ Cabling

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Session Outline

- PCI Express External Cabling
  - ✓Why and who?
  - ✓Usage Models
    - Examples
  - ✓Preliminary definition
    - Targeted link widths and distances
    - Auxiliary signals
    - Keying Requirement
  - ✓Call To Action

Why PCI Express Cabling?

- PCI-SIG members were surveyed in April 2003
  - ✓Responses representing several market segments indicated that cabling was required
    - Extend PCI Express protocol / functionality across arbitrary distances and packaging
      - Need cannot be met using existing backplane connectivity
- The Cabling Working Group was formed in August 2003
  - ✓Charter is to create a specification that focuses on
    - Standard cable connectors
    - Copper cabling attributes and electrical characteristics
      - Acknowledging that optical cabling will be addressed later!
    - Connector retention
    - Identification/labeling
  - ✓This is **NOT** a replacement for cabling to USB or 1394 peripherals!

Who's Involved In the PCI Express Cabling Working Group?

- 16 Member companies and 11 Observer companies
  - ✓Members have voting rights
- The WG includes:
  - ✓Several OEMs
    - Covering mobile through server segments
    - Covering equipment manufacturers
  - ✓Several PCI Express Silicon Providers
    - Covering host-side silicon and device-side silicon
  - ✓Several Cable and Connector Vendors
    - Providing experience with existing high-speed interface solutions
  - ✓Several peripheral/equipment manufacturers
- Simulation Working Group
  - ✓Subset of the Cabling WG
  - ✓Focusing on the simulation of PCI Express across copper cables

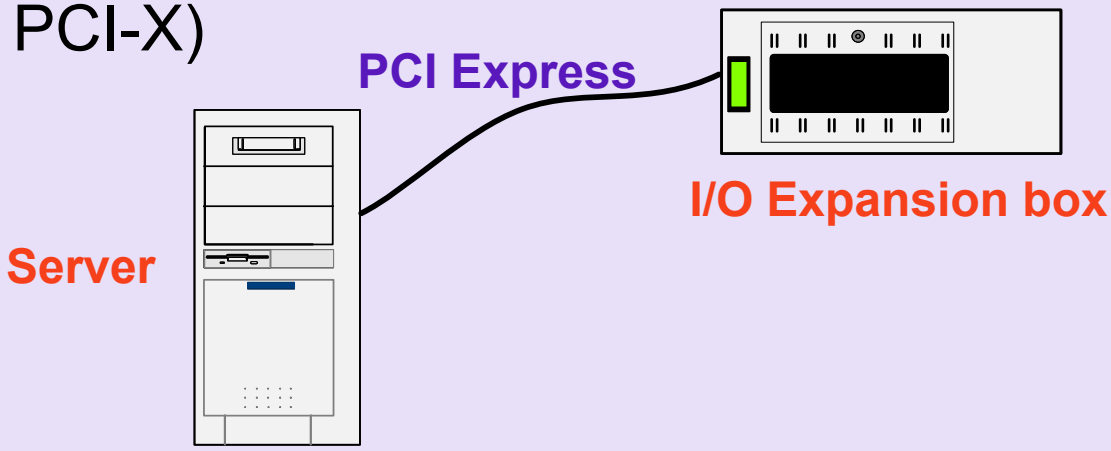
PCI Express External Cabling Usage Models

PCI Express Cabling Usage Models

- Expansion I/O
- Split-system (disaggregate) desktop
- Tethered docking for mobile platforms
- External graphics controllers
- Communication equipment
- Printers and other office equipment
- Test and measurement equipment

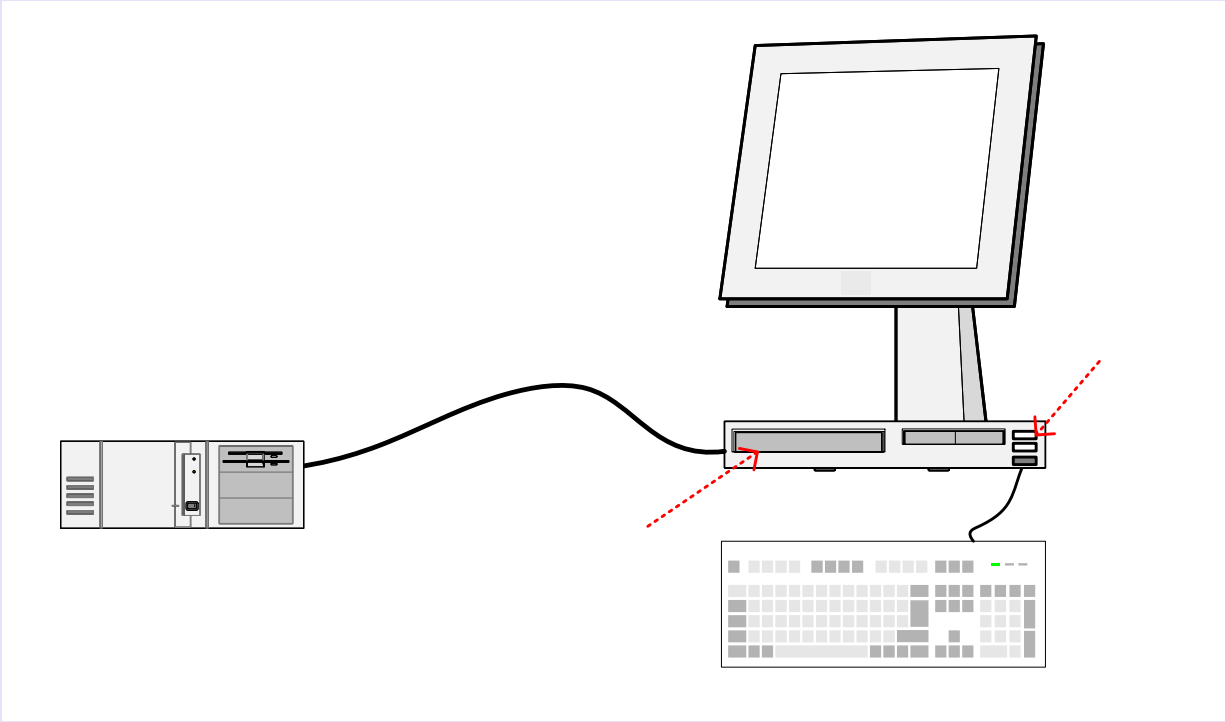
Expansion I/O Example

- Provide additional or different slot types beyond what is available in the base system. For example:
  - ✓Provide additional I/O add-in card capacity (e.g. PCI Express CEM)
  - ✓Provide support for new add-in card interface technologies (e.g. SIOM)
  - ✓Provide “legacy” I/O slots for customers who reuse add-in cards (e.g. PCI-X)



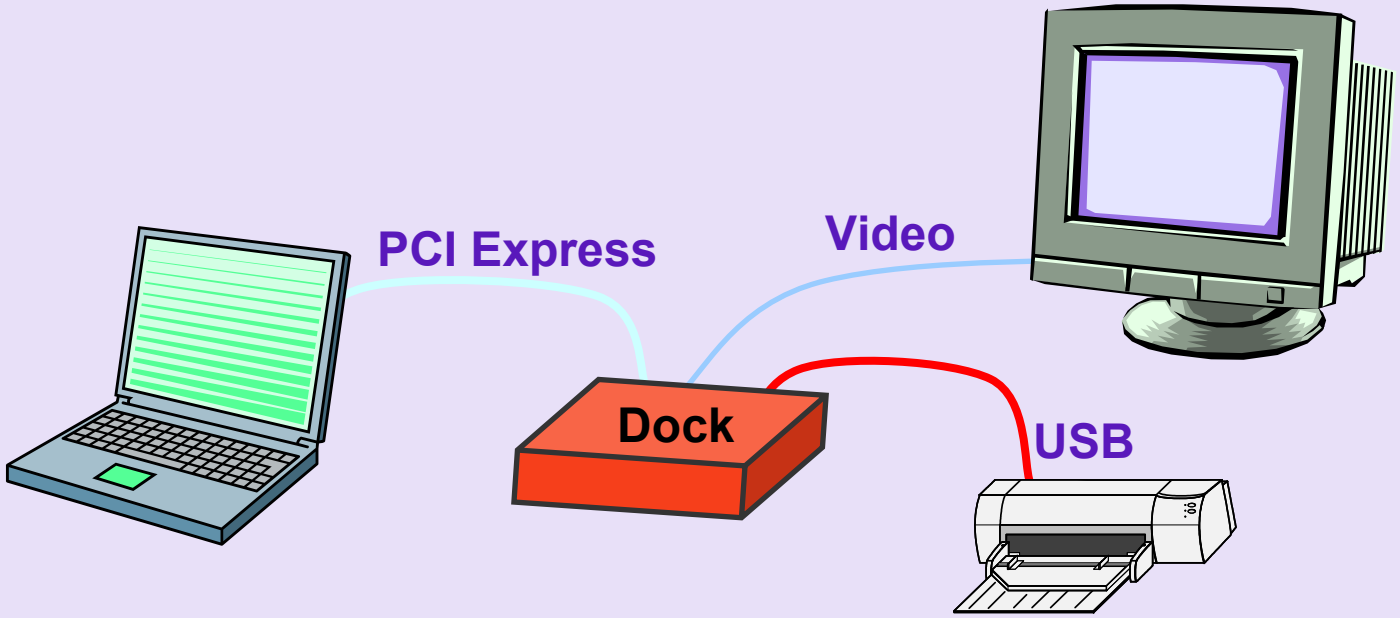
Split-system (disaggregate) Desktop Example

- Move the user-accessible components (e.g. optical drive bay and USB ports) closer to the user
- Move the “static” and “noisy” components (e.g. CPU, hard drive) further away from the user



Tethered Docking for Mobile Platforms Example

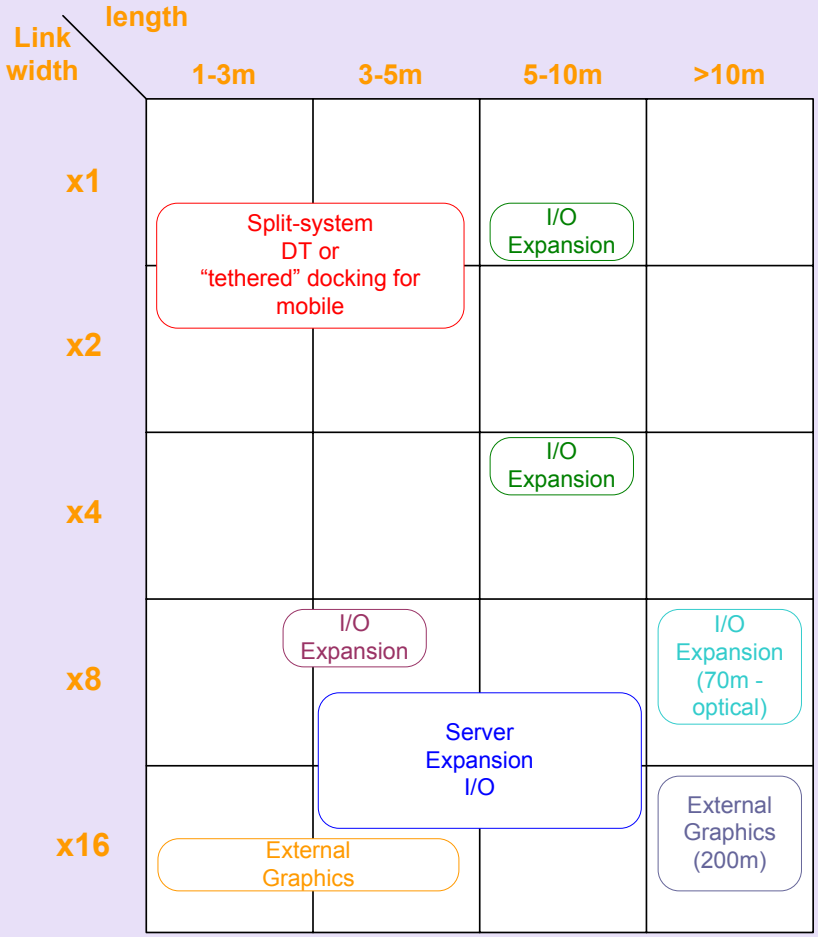
- Replace “rigid” docking station or port replicator with a tethered solution
  - ✓Flexibility in placement of the laptop and docking station
  - ✓Decouple laptop and docking station life-cycle



PCI Express External Cabling Preliminary Definition

Targeted Link Widths and Distances

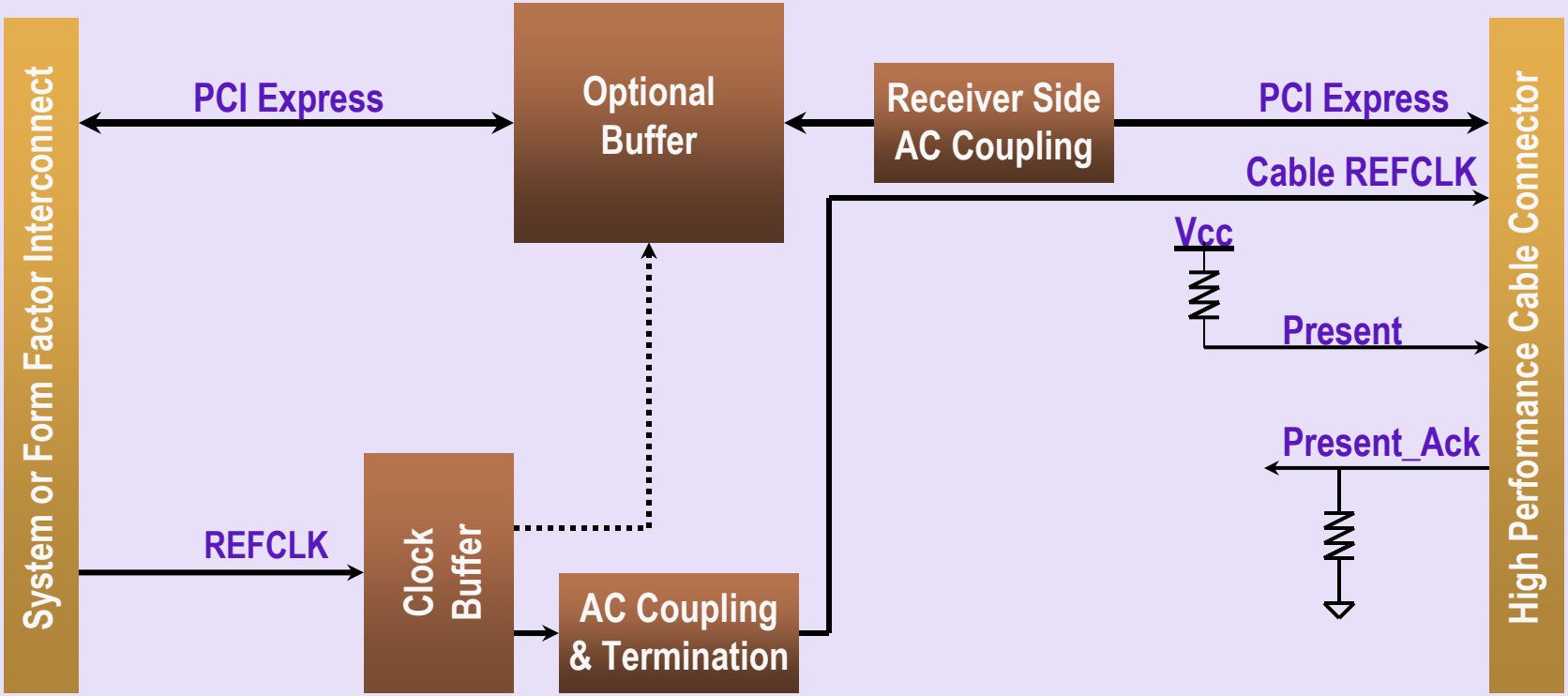
- The follow chart illustrates target applications and required link widths and distances.



Current Specification Status

- Working to define connectors supporting various market segments
  - ✓x1, x4, x8 and x16 Link widths
    - – x2 Link supported as subset of the x4 connector definition
  - ✓Anticipate and support Gen2 signaling
  - ✓Sideband signals for compatibility with existing silicon and OS
    - – Presence Detect and Reference Clock
  - ✓Optional power for active signal conditioning within cable assembly
- Cable length
  - ✓Simulations assume PCI Express signaling without additional equalization
    - – 7 meters (without additional equalization or repeaters) seems feasible at the current 2.5Gbps; active components (e.g. repeaters) will enable greater lengths
  - ✓Approximately 10dB of 13.2dB budget, at 1.25GHz, reserved for cable assy.
    - – Includes cable loss, crosstalk, intra-pair skew, mated connectors, etc.
  - ✓Impact of Gen2 signaling currently unknown and not likely to be included with first release of the cable specification

Upstream Block Diagram



Auxiliary Signals

- Additional signals are required in order to provide a functional and reliable link between two units.
- The specific implementation is intended for maintaining compatibility with OS and silicon functionality.
- To date, the following signals have been identified:
  - ✓Reference Clock
  - ✓Presence Detect
  - ✓Active component power provision
  - ✓Wake (under consideration)

Reference Clock

- Why distribute the 100MHz reference clock?
  - ✓Required for some silicon solutions to meet the 600ppm data rate matching requirement
  - ✓Support of Spread Spectrum Clocking (SSC)
  - ✓Certain data recovery mechanisms might require a common-clock
  - ✓Provides a baseline for timing control at a downstream slave device
- Implementation
  - ✓AC-Coupled differential signal
    - Requires conversion to PC standard HCSL signaling
  - ✓Specifies signal requirements
    - Minimum signal swing, rise/fall time, etc.
    - Source and load termination
  - ✓Does not dictate a specific logic family

Presence Detect

- Why implement a Presence Detect mechanism?
  - ✓Enable power management
  - ✓Compatible Hot Plug notification
  - ✓Power sequencing between subsystems
  - ✓Additional timing control of boot sequence
  - ✓Prevent component damage
  - ✓End-user diagnostics
- Implementation
  - ✓A roundtrip mechanism to preserve power domain isolation
  - ✓Detect if downstream subsystem is powered and cable installed
    - Enable the cabled reference clock if true
    - Signal a Hot Plug event if such occurred
  - ✓Detect if upstream subsystem is powered and cable installed
    - Automatic power-up of downstream subsystem
    - Enable reset timing state-machine

Active Component Power Provision

- Why provide power?
  - ✓Implement active components within the connector housing
    - Extend achievable cable length through additional equalization
    - Potentially implement optical transceivers as part of cable assembly
- Implementation
  - ✓Power provisioning is optional
    - Keying will be provided
  - ✓For use within the connector assembly only!
    - Power will not be provided via cable wiring!
  - ✓Dedicated power and ground pins are allocated
  - ✓Actual voltage is yet to be defined

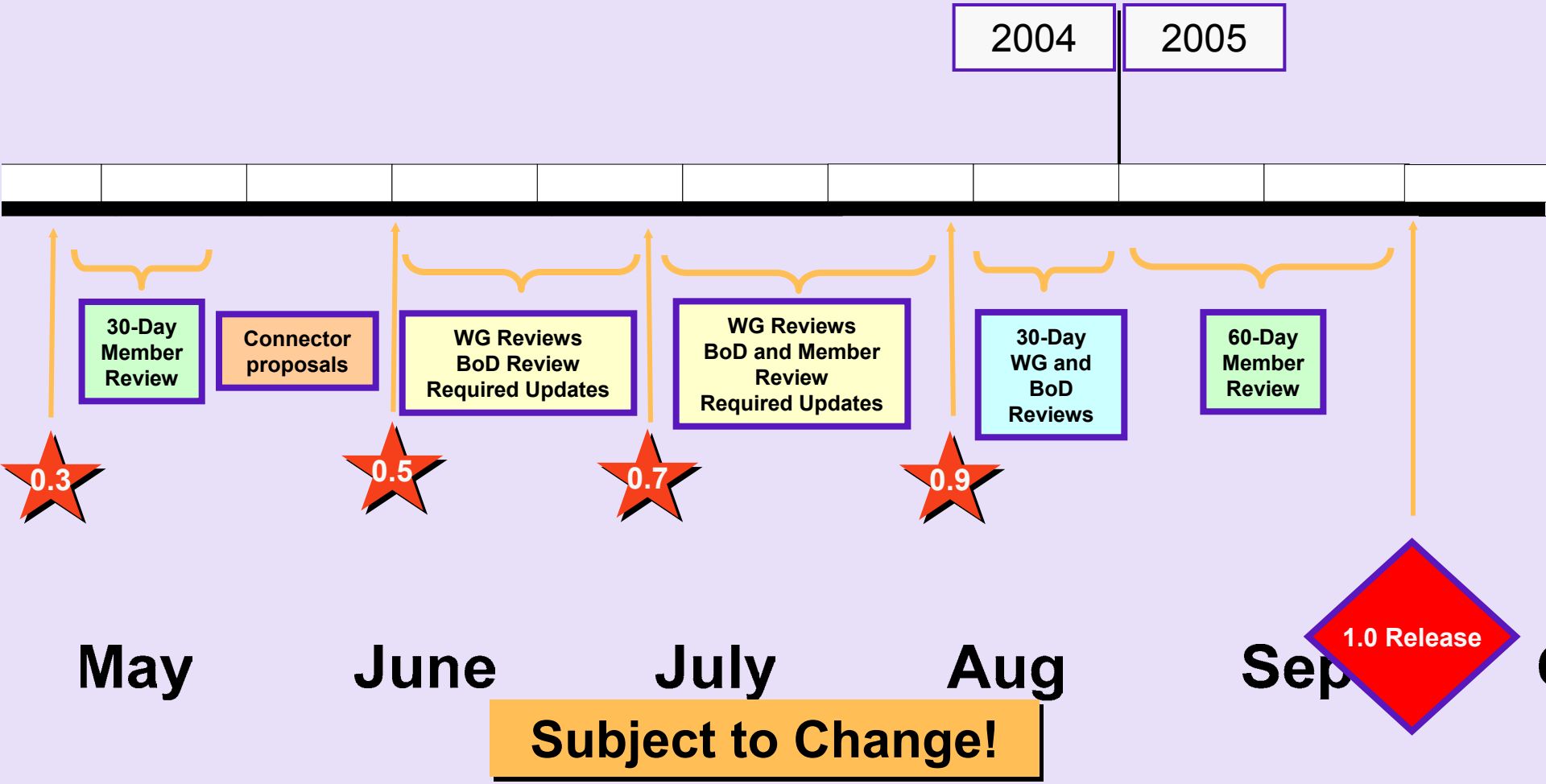
Wake (Under Consideration)

- Why support the out-of-band wake mechanism?
  - ✓PCI Express silicon is not required to support the in-band beacon mechanism
  - ✓ Some PCI Express form factors (e.g. CEM) require support for wake

Keying Requirement

- Why implement keying?
  - ✓Insure the right match between cable assemblies and subsystems
  - ✓Power Provision Key
    - Key prevents a cable assembly that requires power from being inserted into a subsystem connector that doesn't provide such power
  - ✓Signaling Generation Key
    - PCI Express Generation 2 (Gen2) signaling could require more interconnect restrictions than Gen1
    - Key prevents a Gen1-only cable from being inserted into a Gen2-capable receptacle
- Implementations are being proposed within the WG at this time

Proposed PCI Express Cabling Schedule



Call To Action

- PCI-SIG members should review the draft specifications when made available and provide your feedback!
- Develop your market requirements for PCI Express cabling and provide input to connector and cable suppliers

Question & Answers

Thank you for attending the
PCI-SIG Developers Conference 2004.

For more information please go to
www.pcisig.com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