Techniques for Efficient Verification of PCIe® to PCI Bridge

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Agenda

- Introduction
- Typical PCIe Bridge Test Bench
- Requirements for Environment Components
- Test Suite Development Strategy
- Test Suite Execution Strategy
- Critical Areas for Verification
- Reusability of Verification Environment
- Summary

1. Introduction

- Tell any design engineer that he/she is coding bugs along with the design !!
  - ✓ Every one is going to get offended !
- But, that's the reality.
- Therefore there is a need of robust verification environment to uncover these bugs and to ensure first time working silicon.

- This presentation talks of verification of a Forward PCIe Bridge.

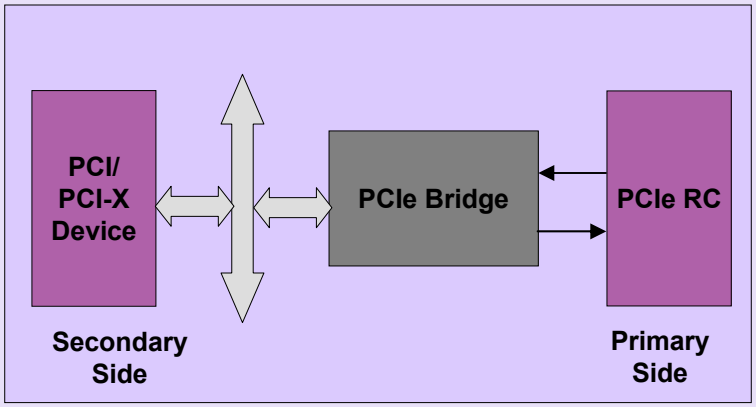
What is a Bridge

- A connection path between two independent buses.
- Interface between existing Technology and the new Technology.
- Mechanism to have more devices.

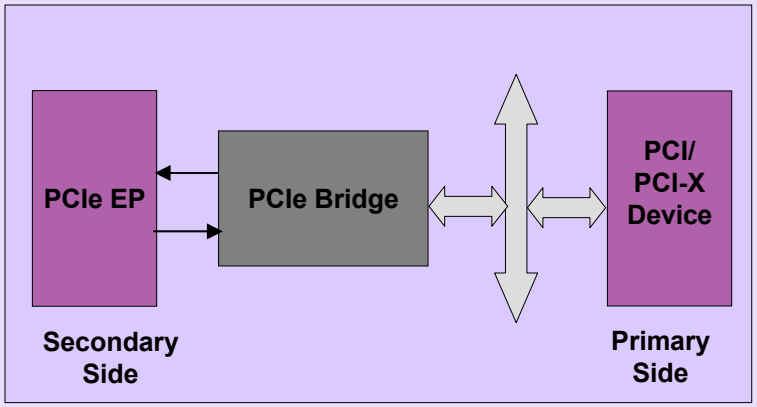
- PCIe Bridge is a connection path between PCIe and PCI/PCI-X® buses.

Types of PCIe Bridges

- Depending on the Primary Interface
  - ✓ Forward Bridges
    - A bridge from PCIe primary to PCI/PCI-X secondary Interface.
  - ✓ Reverse Bridges
    - A bridge from PCI/PCI-X primary to PCIe secondary Interface.



Forward Bridge



Reverse Bridge

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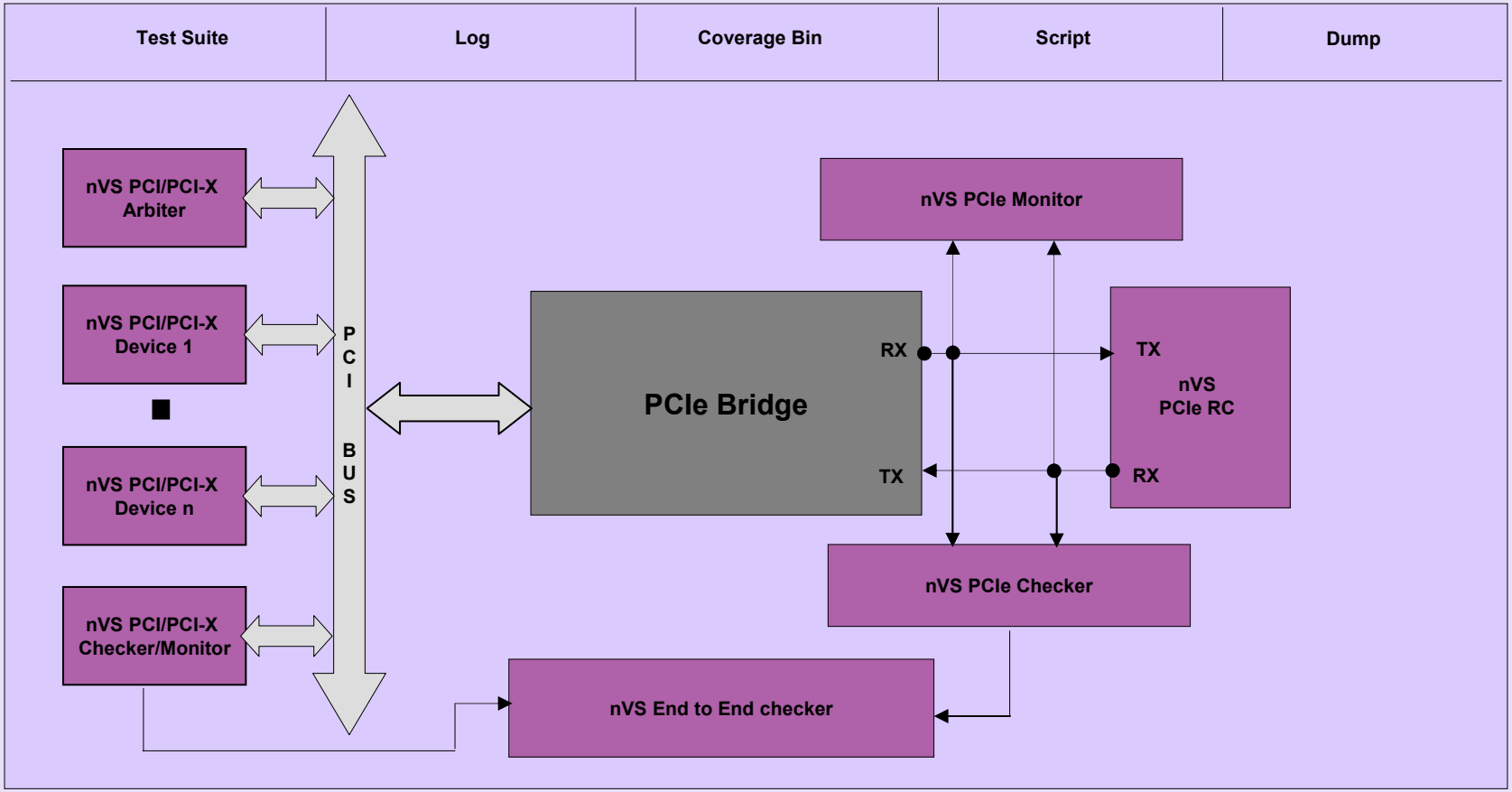
2. Typical PCIe Bridge Test Bench

- Environment Block Diagram



Description of Block Diagram

- Typical PCIe Bridge Environment must consist
  - ✓ PCIe Drivers
  - ✓ PCIe Monitor/Checker
  - ✓ PCI/PCI-X Master/Initiator and Slave/Target
  - ✓ PCI/PCI-X Arbiter
  - ✓ PCI/PCI-X Monitor/Checker
  - ✓ End to End Checker (E2E Checker)
  - ✓ Scripts & Test Suite
  - ✓ Log & Dump Generation
  - ✓ Coverage Bin

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3. Requirements for Environment Components

- The section will cover
  - ✓ Rich features required of the different Drivers.
  - ✓ Features to speed up debugging and verification.
  - ✓ E2E Checker concept.
  - ✓ E2E Checker Modeling Techniques.
  - ✓ Development and execution of Test Suite.
  - ✓ Requirement of Scripts.

Drivers: PCIe BFM

- PCIe BFM must emulate Root Complex or Down Port Switch functionality.
- Rich Feature Set
  - ✓ Supporting x1 to x32.
  - ✓ Ability to insert erroneous TLP, DLLP and PL Packet.
  - ✓ Ability to stop flow control and start as per test requirements.
  - ✓ Ability to configure RCB size.
  - ✓ Ability to configure completion status.
  - ✓ Exhaustive Event generation.
  - ✓ Call Backs.

Drivers: PCI-X BFMs

- PCI-X BFM must emulate functionality of PCI-X Initiator and Target.
- Rich Feature Set
  - ✓ Configurable termination type and data phase of termination.
  - ✓ Split Completion in one go or chunks.
  - ✓ Configurable subsequent Split Completion Status.
  - ✓ Parity error insertion.
  - ✓ Exhaustive Event generation.
  - ✓ Call Backs.

Drivers: PCI BFMs

- PCI BFM must emulate functionality of PCI Master and Slave.
- Rich Feature Set
  - ✓ Configurable termination type and data phase of termination.
  - ✓ Fast back to back.
  - ✓ Parity Error insertion.
  - ✓ Configurable maximum retry count.
  - ✓ Exhaustive Event generation.
  - ✓ Call Backs.

Drivers: PCI/PCI-X Arbiter

- PCI/PCI-X Arbiter must emulate arbiter functionality.
- Rich Feature Set
  - ✓ Configurable Grant assertion logic.
  - ✓ Configurable number of clocks Grant to be asserted.
  - ✓ Ability of set high priority of any agent.
  - ✓ Ability to change the Grant assertion logic in run time.

Monitors

- Monitor captures the Bus/Link information and prints the information in the ASCII format.
- Feature to speed up debugging
  - ✓ Configurable to print only the required information.
  - ✓ Option to print the information in specified file, output or both.
  - ✓ Ability to configure time frame to start the printing.
  - ✓ PCIe Monitor must have the capability to print Packet and Symbol information in separate files.

Protocol Checkers

- Protocol checker keeps an eye on adherence of protocols on each interface.
- Advance Feature to ease debugging
  - ✓ Error messages must specify the Specification Section.
  - ✓ Option to switch OFF/ON any rule.
  - ✓ Coverage bin for each rule.
  - ✓ Exhaustive Event generation.
  - ✓ Call Backs.

```
Error      TSx ordered set must have same value of Scramble bit on all lanes.Sec.#
4.2.4.
```

End to End Checker (E2E)

- Tracks Transaction level activity from one interface to the other interface.
- Behavioral Bridge.

- Why it is required ?
  - ✓ Protocol checkers only polices the protocol violation on the each interface.
  - ✓ Therefore, a component is required to verify the transaction flow from one interface to the other interface.

End to End Checker (E2E)

- Effective Modeling Techniques
  - ✓ Extract information from Protocol Checkers and drivers Must be developed incrementally.
  - ✓ Reusable.
- Key features
  - ✓ Coverage Bin.
  - ✓ Data checking.
  - ✓ Log file generation
    - – Print the transaction level information of each interface.

Scripts & Test Suite

- Environment must be supported by scripts
  - ✓ To have the common top level for PCI & PCI-X secondary operations and different lane count.
  - ✓ To automate the test case running.
  - ✓ To merge the log files.
  - ✓ Regression execution.

- PCIe Bridge has complexity of PCIe, PCI and PCI-X, therefore test suite development and execution is very complex. Looking at the complexity, the presentation have a dedicated section on the same.

Logs and Dump Generation

- All environment components must have sufficient message reporting to help debugging
- Ability to print the information in user define files or IO.
- All messages must be grouped into levels.
- Ability to configure the message level during run time for each component.

- Ability to configure level of Dump generation.

Coverage bin

- A coverage bin has group of counters incremented on the define conditions.
- Coverage goals to be define during design phase.
- All critical conditions to be covered.
- Option to merge the multiple simulation run report.
- On the fly coverage counter value accessible to Test Suite.

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4. Test Suite Development Strategy

- Traceability Matrix.
- Proposed Traceability Matrix.
- Test Suite Classification.
- Guidelines for coding test cases.

Traceability Matrix

- Traceability Matrix created with Design Phase.
- Track information of test suite, test case for each feature.
- Recommended to cover PCI, PCI-X and PCIe specifications.

Feature Section #	Description	Test Suite	Test Case File	Test Case #	Bridge Bug
2.12 PCIe Bridge Specification	Must advertise Finite FC credits for Completion Header and CO				
. . .					
. . .					

Test Suite Classification

- Test Suite can be classified as following.
  - ✓ Basic
  - ✓ Random & Constraint Random
  - ✓ Directed
  - ✓ Error
  - ✓ Compliance
  - ✓ Corner
  - ✓ Regression

Test Suite Classification…

- Basic Test Suite
  - ✓ Ensures grass-root functionality verification.
  - ✓ Sub Divided
    - Only Transaction from one interface to other.
    - Transaction from both the interfaces.
- Random Test Suite
  - ✓ Generates heavy traffic and guarantees bridge stability.
  - ✓ Sub Divided
    - Random 1: Correct Packet.
    - Random 2: Random 1 + Error Packet.
    - Random 3: Random 2 with Loop based.

Test Suite Classification…

- Directed Test Suite
  - ✓ Rigorously verifies a dedicated feature.
  - ✓ Sub Divided
    - Configuration
      - Initial Value Test.
      - Type Test.
    - PCI
      - Non posted transaction flushing.
    - PCI-X
      - Split Completions.
    - PCIe
      - Replay.
    - Bridge
      - Time Out.

Test Suite Classification…

- Compliance Test Suite
  - ✓ Check List point execution.
  - ✓ Sub Divided
    - PCI.
    - PCI-X.
    - PCIe (Refer PCIe EP Checklist).
- Error Test Suite
  - ✓ Verifies the Error handling.
  - ✓ Sub Divided
    - PCI/PCI-X.
    - PCIe.

Test Suite Classification…

- Corner Test Suite
  - ✓ To improve coverage count.
- Regression
  - ✓ Ensure the bridge stability and guarantees bug fixing is a really bug fixing, not coding bug.
  - ✓ Sub Divided
    - Debug: Test failing recently.
    - Short: Test started passing recently.
    - Long: Test passing for more that n weeks.

Guidelines of Test case development

- Self checking Test Cases.
- Randomness in even in the directed test to generate a newer test pattern in every run.
- Task for common BFM configurations.
- Module approach for each test case.
- Exhaustive print information.
- Error coverage bin.

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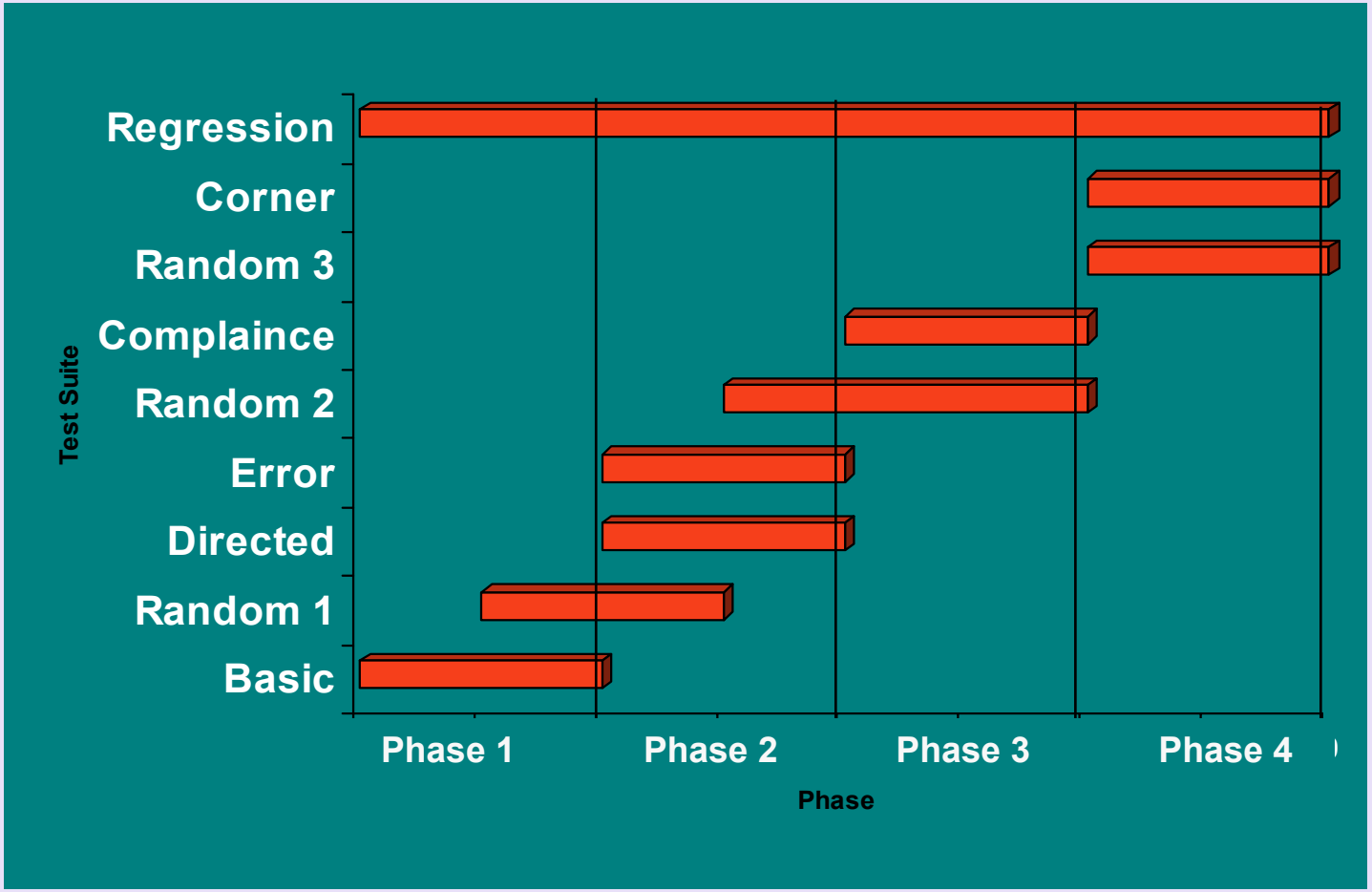
5. Test Suite Execution Strategy



Test Suite Execution Strategy …

- Phase 1
  - ✓ Starts with Code Drop.
  - ✓ Ensures that bridge is ready for the regress verification.
- Phase 2
  - ✓ Ensures that all bridge features are verified.
  - ✓ Ensures missing logic and features are there in code.

Test Suite Execution Strategy …

- Phase 3
  - ✓ Time for the code coverage.
  - ✓ Revisiting the Test Plan.
- Phase 4
  - ✓ Preparing for confidence that Bridge is bug free.
  - ✓ Bridge ready for Tape out.

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6. Critical Areas for Verification

- General
  - ✓ Flushing of Transaction on time out.
  - ✓ Buffer Allocation.
  - ✓ Error handling and Error reporting.
- PCIe to PCI-X
  - ✓ Tag allocated on cycle ownership.
  - ✓ For RCB 64 merges the cycle and generate ADB boundary cycle.

Critical Areas for Verification …

- PCIe to PCI
  - ✓ Correct Cycle conversion for memory read.
  - ✓ Transaction Ordering.
- PCI-X to PCIe
  - ✓ Breaking Cycle according to Byte Enables.
  - ✓ Breaks 4K crossing cycle.
- PCI to PCIe
  - ✓ Read Data Prefetching.
  - ✓ Breaking Cycle according to Byte Enables.

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7. Reusability of Verification Environment

- Concept of the Verification Environment discussed, is re-use for the verification of any DUT.
- Reuse able components
  - ✓ Scripts
  - ✓ Template of Traceability Matrix
  - ✓ Log and Dump Generation
  - ✓ Concept of the E2E Checker
  - ✓ Test Suite classification
  - ✓ Test Suite execution Strategy

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8. Summary

- Robust environment is must for bug free tape out.
- Verification IP must have rich feature set.
- Environment component must have feature to speed up the verification.
- Scripts plays a critical role in verification
- Traceability Matrix is key requirement for Test Plan.
- Test Suite execution strategy must be planned.
- Re-Use of Verification Environment

Thank you for attending the
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