PCI Express® – A Forward Looking Protocol

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Agenda

- Evolution of PCI Express
- Transitioning to PCI Express
- Fundamentals of PCI Express Technology
- PCI-SIG® Compliance Workshop
- Q & A

Evolution of PCI Express

- What drives the future:
  - ✓ Challenge and Competition to stay at the top
  - ✓ Customer Requirement
    - Multiplying Date Bandwidth Requirement
    - Return On Investment (ROI) Justification
    - Backward Compatibility to Previous Generation

Evolution of PCI Express

- Revolutionary Technologies:
  - ✓ Ethernet
  - ✓ Fibre Channel
  - ✓ FB-DIMM
- Evolutionary Technologies:
  - ✓ SCSI to SAS
  - ✓ ATA to SATA
  - ✓ PCI to PCI Express

Transitioning to PCI Express

- **Bandwidth Advantage**

	Clock (MHz)	# of Data Wires	Total Bandwidth (GBPS)	Notes (Bus#2, Device, Fn)
PCI-32/33	33	32	1.056	B2,Dx, Fx
PCI-64/66	66	64	4.224	B2,Dx, Fx
PCI-X 64/133	133	64	8.448	B2,Dx, Fx
PCI-X 64/266	133 (DDR)	64	16.896	B2,Dx, Fx
PCIe x1	100	4	4	B2,D0, Fx
PCIe x4	100	16	16	B2,D0, Fx
PCIe x8	100	32	32	B2,D0, Fx
PCIe x16	100	64	64	B2,D0, Fx

Transitioning to PCI Express

- **Real Estate Advantage**
  - ✓ Smaller Form Factor Boards
  - ✓ Phasing out of PCI and Emergence of PCIe® 1.x and 2.0 will drive smaller size systems.
- **Scalability Advantage**
  - ✓ x1 upto x32
  - ✓ Transitioning from PCIe 1.x to 2.0
- **Quality Of Service**
  - ✓ Traffic Class, Virtual Channel
  - ✓ Isochronous Traffic Support

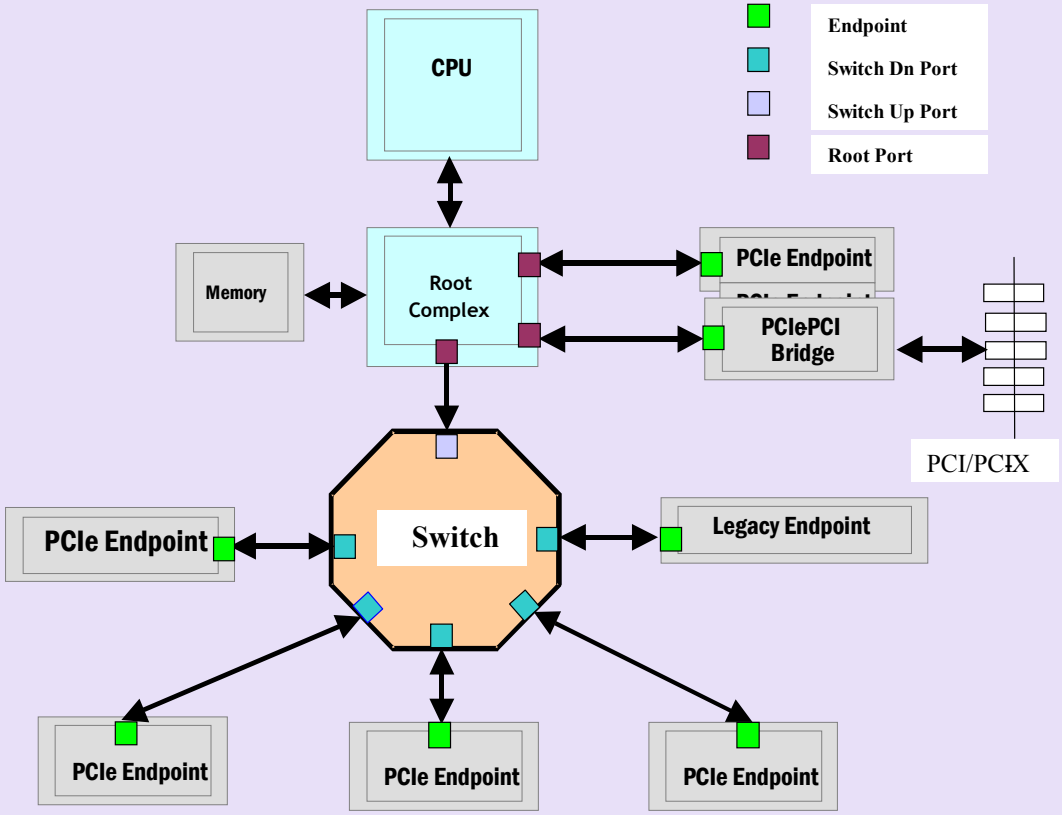
Fabric Topology

- PCI:
  - ✓ Simple Building Blocks – Master/Slave
  - ✓ Host Bus Adapter and Bridge
  - ✓ Multiple Devices exist on one Bus (Bx,Dx,Fx)
- PCI Express:
  - ✓ Multiple Building Blocks – Endpoint/Root/Switch
  - ✓ Endpoint (PCI-like application)
  - ✓ Root Complex (Southbridge/Northbridge-like application)
  - ✓ Switch
  - ✓ Multi-Mode Device : Endpoint or Root or Switch
    - Configures at power-up
    - Application/Usage of this powerful feature is emerging.
  - ✓ Point-to-Point Protocol (Bx,D0,Fx)

Features of PCI Express

- Link-up:
  - ✓ Root initiates the Link-up with Endpoint/Switch Upstream
- Flow Control:
  - ✓ Differentiated for Write/Read/Completion
  - ✓ Differentiated for Header/Data
- Quality of Service:
  - ✓ Virtual Channel and Traffic Class
- Power Management:
- Tons of Optional Features
  - ✓ End-to-End CRC (ECRC) in addition to Link-to-Link CRC (LCRC)
  - ✓ Advanced Error Reporting

A Typical PCI Express Topology



Example PCI Express Topology

Stress Areas for PCI Express

- Link-up
  - ✓ Power-up Link Up
  - ✓ Link Recovery
  - ✓ Hot Reset
  - ✓ Hot Swap

Stress Areas for PCI Express

- Flow Control
  - ✓ Memory Write - Posted
    - Header
    - Data
  - ✓ Memory Read – Non-posted
    - Header
    - Data
  - ✓ Completion
    - Header
    - Data
  - ✓ Message
    - Legacy Interrupt Message
    - Vendor Message
    - Power Management

Stress Areas for PCI Express

- Power Management
  - ✓ D-State for Device (from PCI)
  - ✓ L-State for Link (for PCIe CORE)
  - ✓ P-State for Phy (for PCIe PHY)
- Effective Power Management is Critical
  - ✓ Legacy Power Management (D-state)
  - ✓ ASPM (L-state)
    - Active State Power Management – by Hardware
    - L0s and L1 states are used

Stress Areas for PCI Express

- Power Management – D-states to L-states

Downstream Component D-State	Upstream Component D-State	Permissible L-state
D0	D0	L0, L0s, or L1
D1	D0-D1	L1
D2	D0-D2	L1
D3hot	D0-D3hot	L1
D3cold	D0-D3cold	L2 or L3

Stress Areas for PCI Express

- Power Management – L-states to P-states to D-states

L-states	P-states	D-states
L0	P0	D0
L0s	P0s	D0
L1	P1	D1, D2, or D3hot
L2	P2	D3cold

PCI-SIG Compliance Workshop

- Why should you attend…..
  - ✓ Test your product – PCI Express Interface
    - Two Parts
      - Compliance Testing
      - Interoperability Testing
  - ✓ Good excuse to your boss to have some time off from work and still get paid

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PCI-SIG Compliance Testing

- Popularly known as “Gold Suite” Testing
- Configuration Testing
  - ✓ Configuration Space Test
  - ✓ Link Stress Test
- Link Testing
  - ✓ Error Scenarios Testing related to Phy /Datalink /Transaction Layers
- Electrical Testing
  - ✓ Electrical properties of the PHY and the BOARD

PCI-SIG Compliance Testing

- Configuration Testing
  - ✓ Test all controllable optional features of the Configuration Space.
  - ✓ Optional Features usually controlled by EEPROM/Embedded CPU/Bootstrap
  - ✓ Can test in-house before the PCI-SIG Compliance Workshop
    - Download PCIECV Software from PCI-SIG Website
  - ✓ **CONTACT PCI-SIG IF YOU DO NOT UNDERSTAND ANY FAILURE**

PCI-SIG Compliance Testing

- Link Testing
  - ✓ Tests the exception conditions like NAK, CRC Error, Duplicate Sequence Number etc.
  - ✓ Can test in-house before the PCI-SIG Compliance Workshop
    - – You can get the Test Card from Agilent

PCI-SIG Interoperability Testing

- This is why I go to PCI-SIG Plugfest
  - ✓ New/Emerging Protocol
  - ✓ New Chipsets
    - Northbridge/Southbridge-like chipsets
    - Switch
  - ✓ OS
    - Windows 2000/XP etc.
    - Linux
    - Solaris
  - ✓ Networking

PCI-SIG Interoperability Testing

- How should you prepare….
  - ✓ Bring your driver software
  - ✓ Bring your diagnostic software
    - To stress the chip
  - ✓ Thumb drives are pretty neat to carry the software
  - ✓ Extremely friendly atmosphere to discuss specific issues.
  - ✓ An Excellent Forum to discuss and conclude on specific issues.

PCI-SIG Interoperability Testing

- What to expect….
  - ✓ An opportunity to stress your component
    - With Almost ALL Chipsets in the industry
    - With Almost ALL Switch Vendors in the industry
    - With Multiple OS – Windows, Linux, Solaris
  - ✓ Validation Steps:
    - Link-up
    - Flow Control
    - Enumeration
    - Memory Write/Read
    - Message Processing from Host
    - Message to Host

PCI-SIG Interoperability Testing

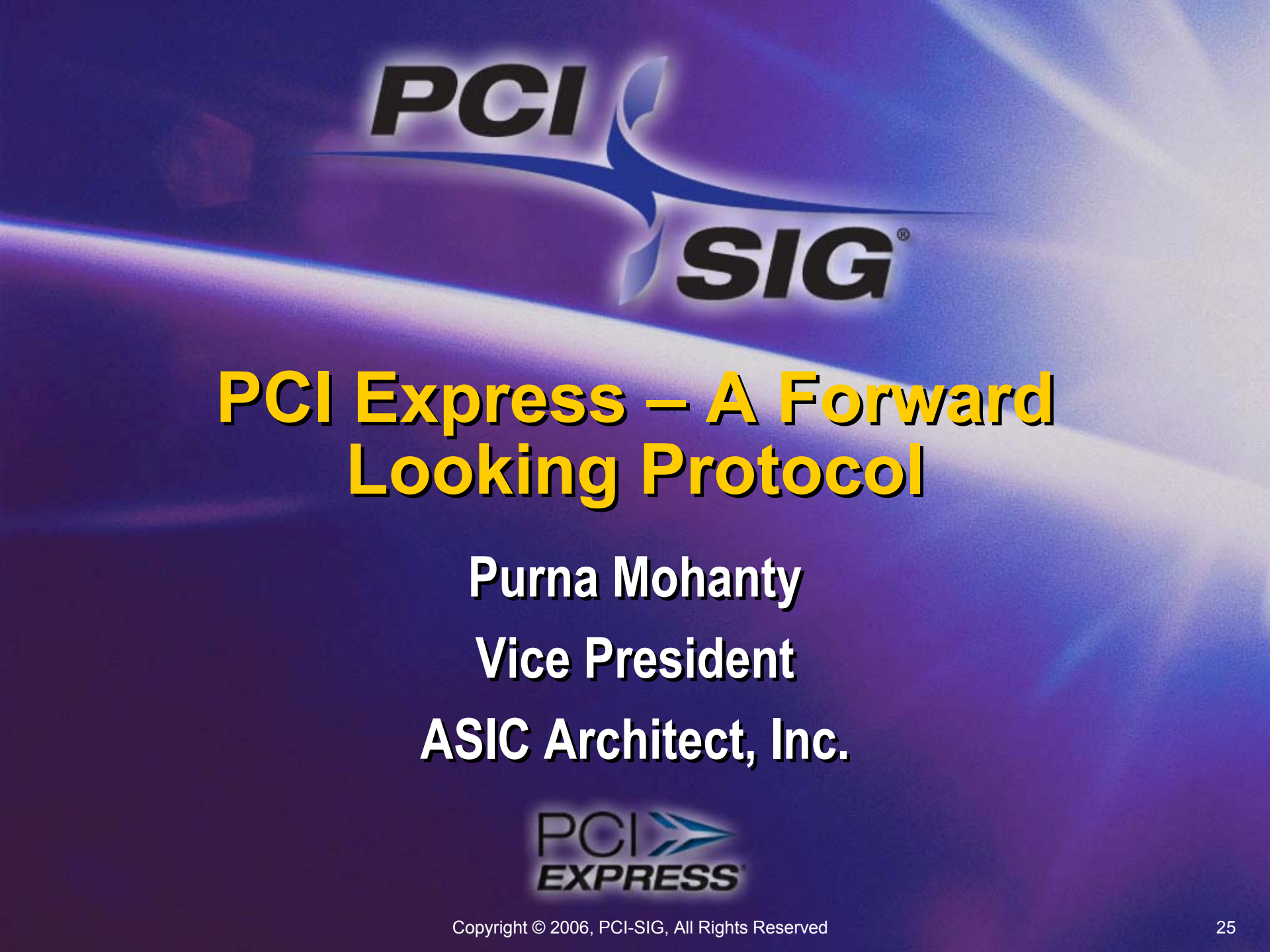
- What if the Systems Hangs ….Crashes ….Reboots..
  - ✓ This is quite possible…
  - ✓ Example:
    - If your application does not respond to certain Vendor Specific Message coming from Host with Credit Updates etc.
- What can you do…
  - ✓ Carry an ANALYZER CARD for PCIe with you.
  - ✓ Carry a 2nd PC/Laptop with Analyzer Software installed.
  - ✓ Helps you to analyze and capture the problem areas immediately within your time slot

PCI Express – A Forward Looking Protocol

- Great Technology to the Future
  - ✓ More amenable to out-of-box applications
  - ✓ Will proliferate into areas PCI did not
  - ✓ So Embrace the Technology and Move ON.
- PCI-SIG Compliance and Interoperability Testing
  - ✓ An Excellent Platform for Testing
  - ✓ A must-attend for PCIe Card/System Vendors

Thank you for attending the PCI-SIG Developers Conference 2006.

For more information please go to www.pcisig.com



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