
PCI
SIG®

Throughput Evaluation of PCIe™ Cores

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IP Development Gr.1

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Agenda

- Introduction
- Throughput Measurement Consideration
- Function of SBOX
- Example of Evaluation
- Summary

Objective for Throughput Measurement

- According to the Spec, Data Transfer Rate is 2.0G bps[#1)] at Peak Time.

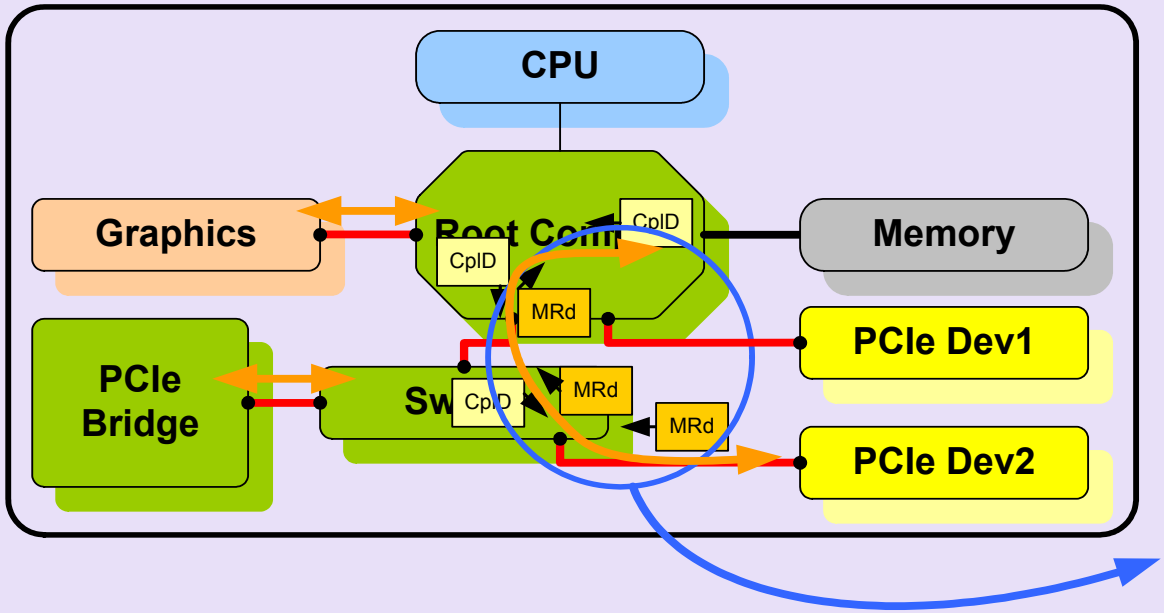
  #1) In the case of 1 Lane.

- But… How Much Bandwidth Could be Utilized In Actual Systems?
  - ✓ Customers Usually Care About Throughput.
  - ✓ It Depends on Systems Used,

    But it is Good to Know Maximum Throughput Our PCIe Cores Can Achieve in Some Systems.

What is Maximum Throughput

- The Throughput Obtained When PCIe Bus is Utilized As Much As Possible
- Example



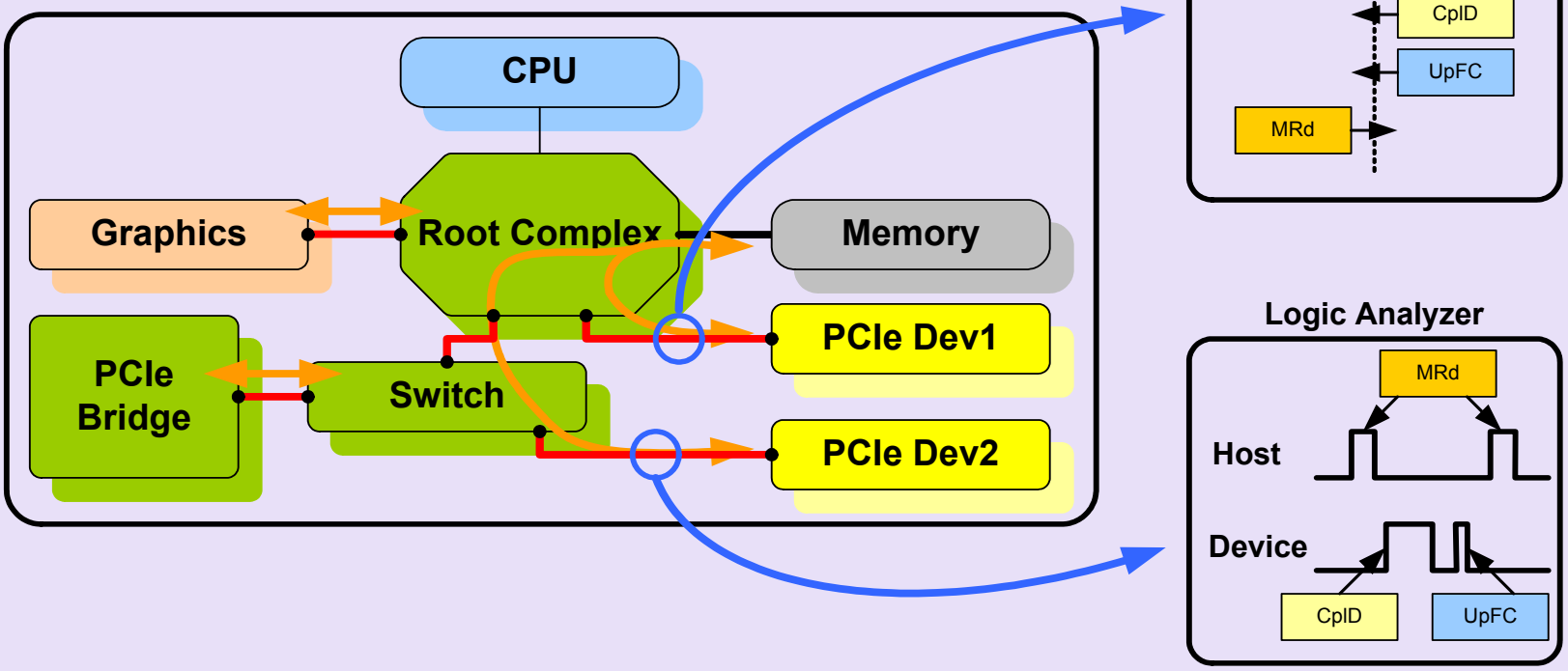
Example

Memory Read Completer Mode

Issue Memory Read Request As Much As Possible

Need for an Easy and Useful Measurement Technique

- Logging Data is NOT Good Idea!!
  - ✓ Hard to Analyze
  - ✓ Logged Data is Limited
  - ✓ Measurement Not Automatic

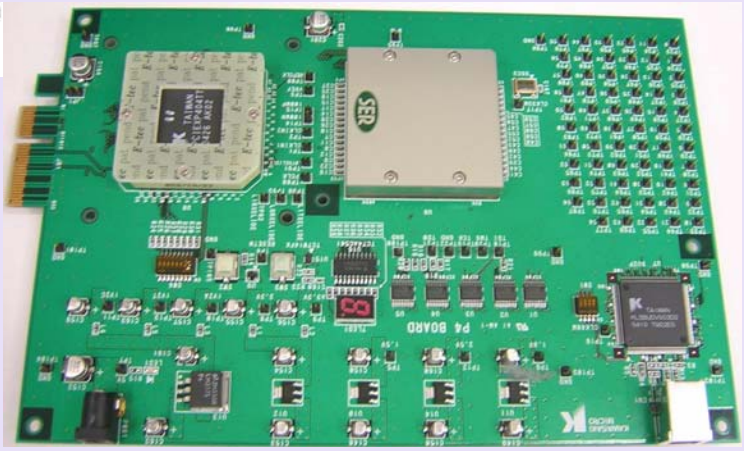


Goal

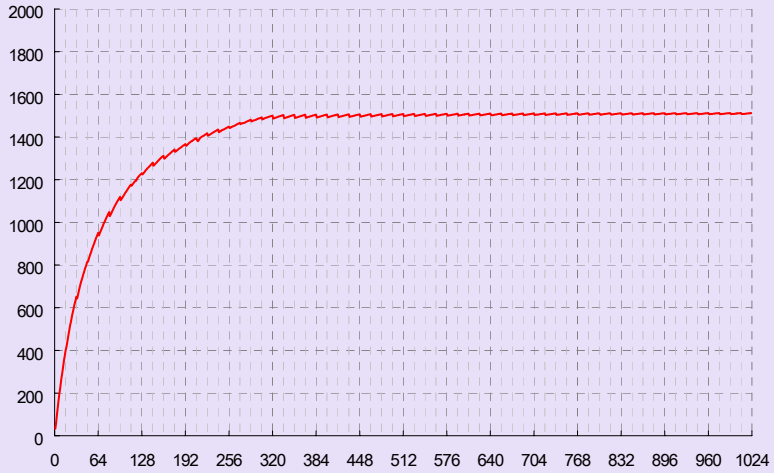
- Create Special Module over PCIe Device Core for Throughput Measurement
  - ✓ Throughput Definition
    - Maximum Throughput of a PCIe Host and Device System
  - ✓ Necessary Functions
    - Maximize the Process of Receive and Transmit of Packets.

      Device PCIe Sends and Receives Packets As Much as Possible to Utilize the Bus As Much As Possible.
    - Record Transferred Data Amount and Consumed Time
- Measure Throughput with the help of Special Module

Typical Example



- Evaluation Board
- Measurement Result



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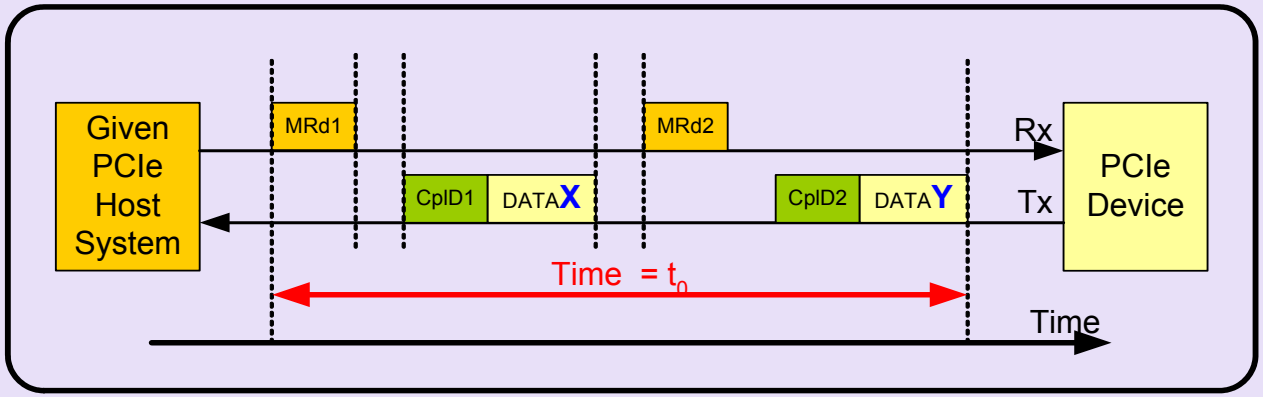
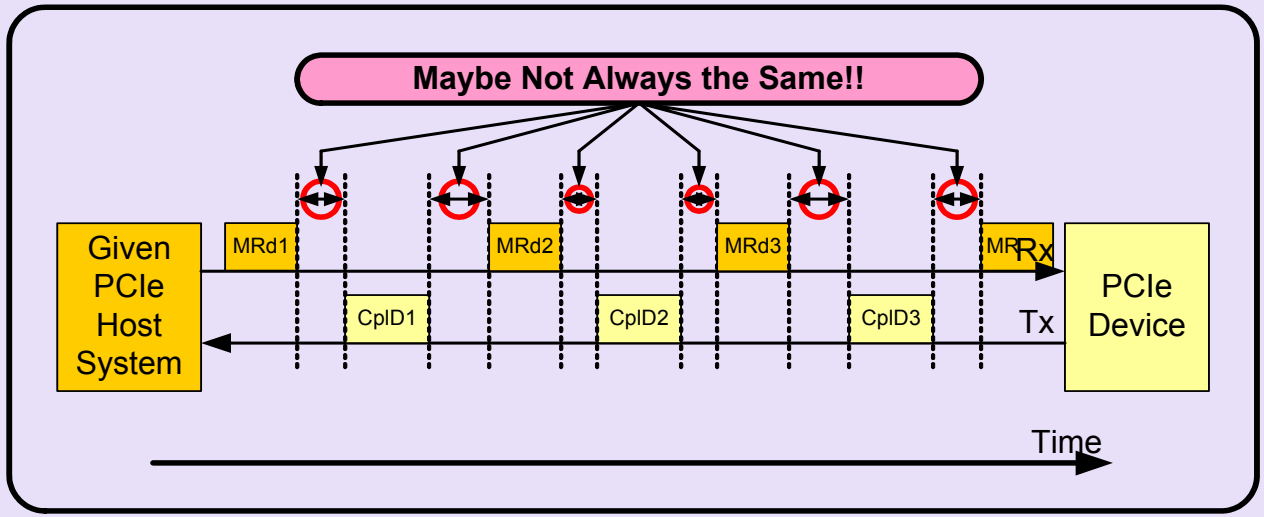
Throughput Consideration

- Throughput = Effective Data Transfer Rate
  - ✓ Count Only Data Field
  - ✓ Headers, CRC *etc*. Not Included
- Throughput = (X + Y) / t_0



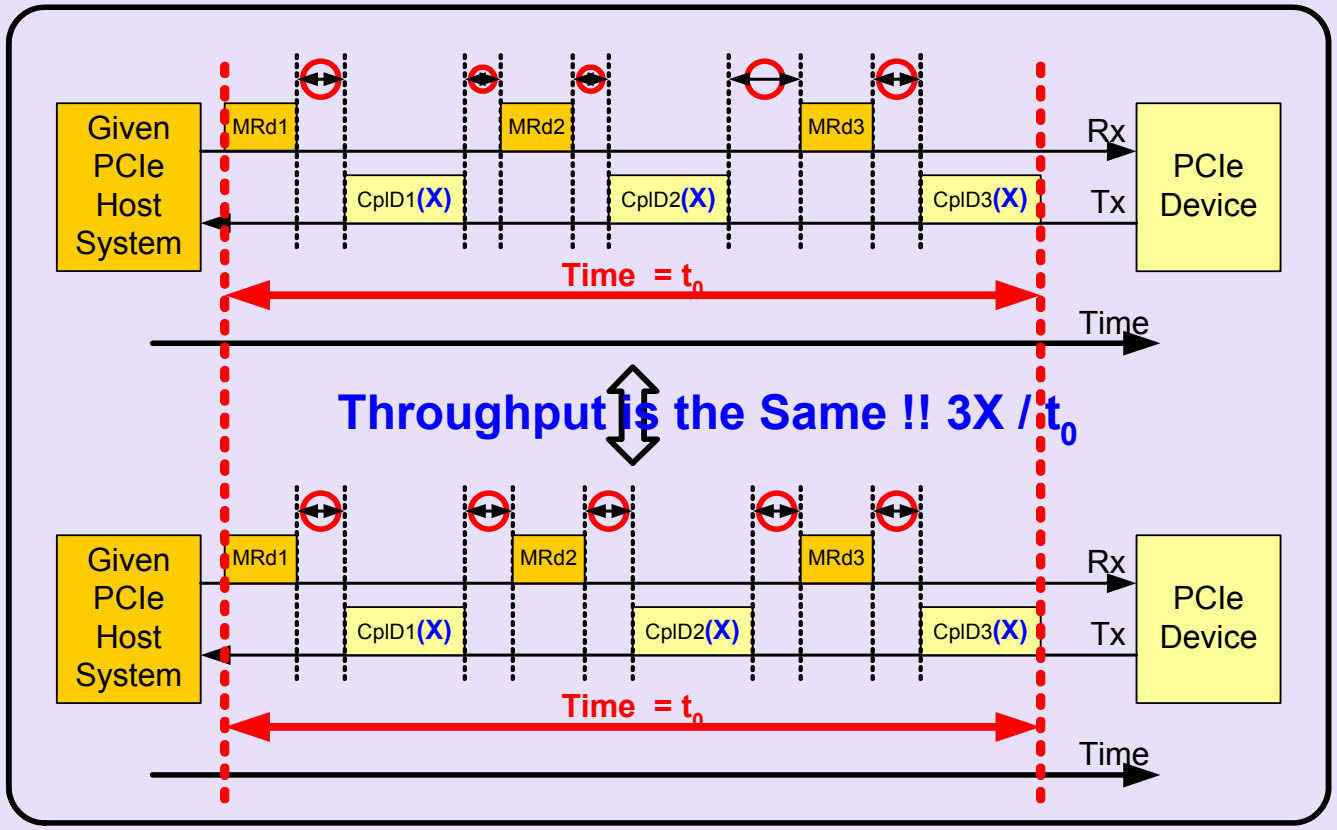
Concern for Throughput Measurement

- Response Time to Received Packets
  - ✓ Not Always the Same
  - ✓ Sometimes Long, Sometimes Short
- This Could Lead to a Different Throughput Value



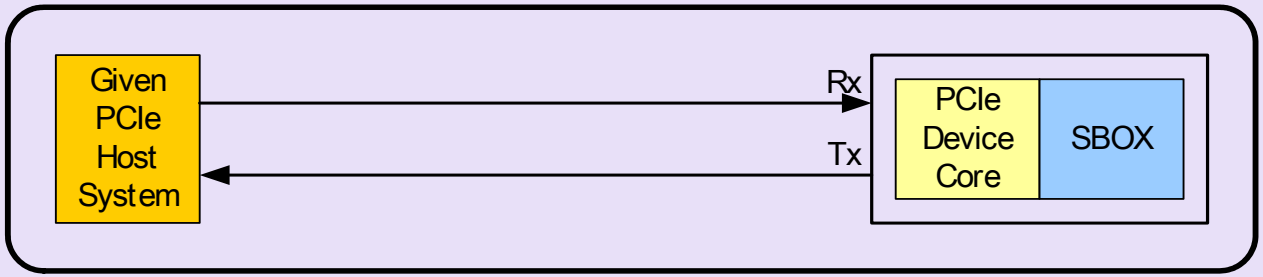
How to Get Proper Throughput Value

- Repeat the Same Request Many Times
  - ✓ Response Time Could be Averaged



Need for a Special Module SBOX

- Logging Data by Bus Analyzer or Logic Analyzer is Not Very Good Idea
  - ✓ Very Huge Log
  - ✓ Hard to Analyze!!
  - ✓ Measurement Not Automatic
- Special Module, SBOX, for Throughput Measurement to Evaluate Easily



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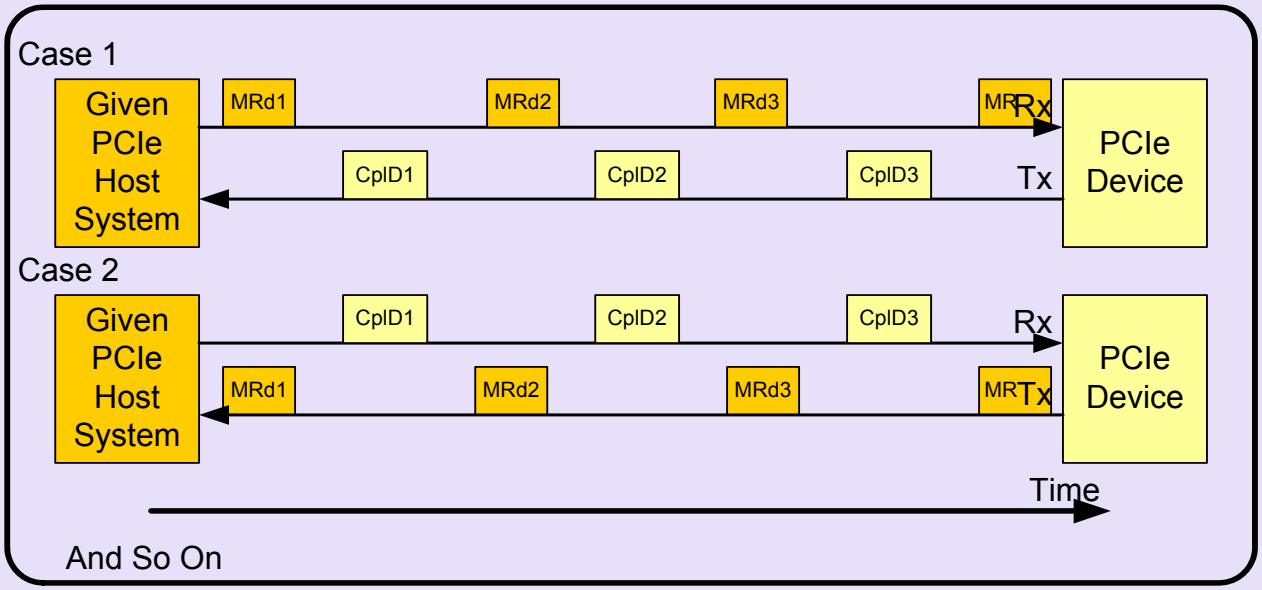
Required Function - Mode Select -

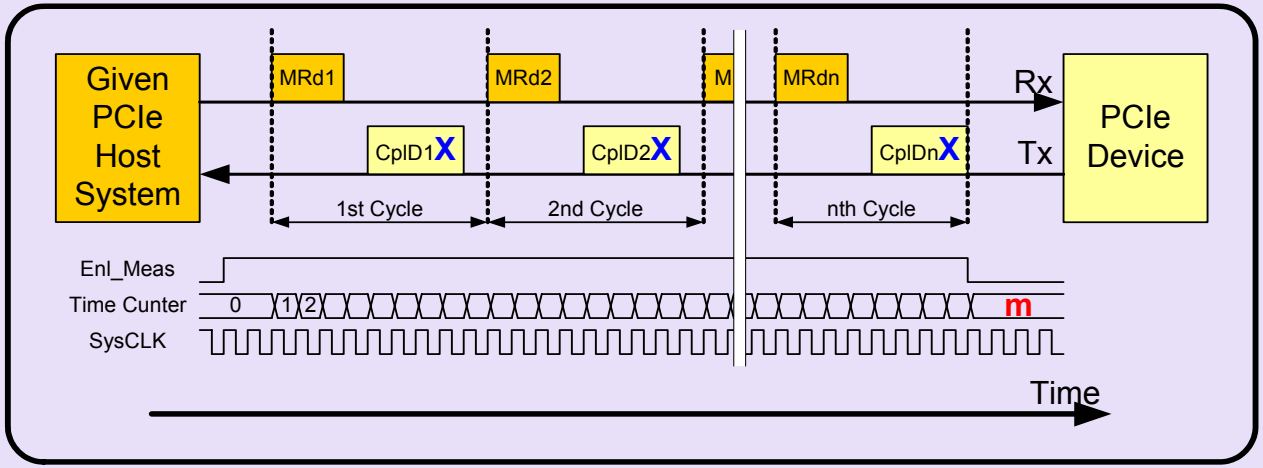
- Request Mode Selectable

No	Mode	Description
1	Memory Read Completer	PCIe Device receives Memory Read Request
2	Memory Read Requester	PCIe Device issues Memory Read Request
3	Memory Write Completer	PCIe Device receives Memory Write Request
4	Memory Write Requester	PCIe Device issues Memory Write Request



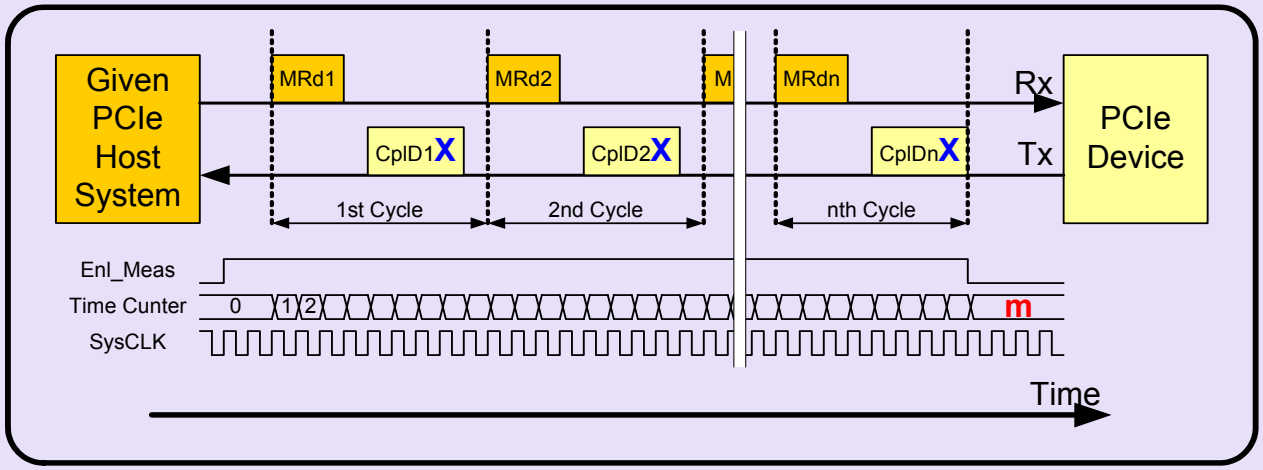
Required Function - Start / End of Measurement -

- Start of Throughput Measurement
  - ✓ Set Enable Measurement Register
    - – Measurement Starts at First TLP Receive
- End of Throughput Measurement
  - ✓ Receive of Last TLP



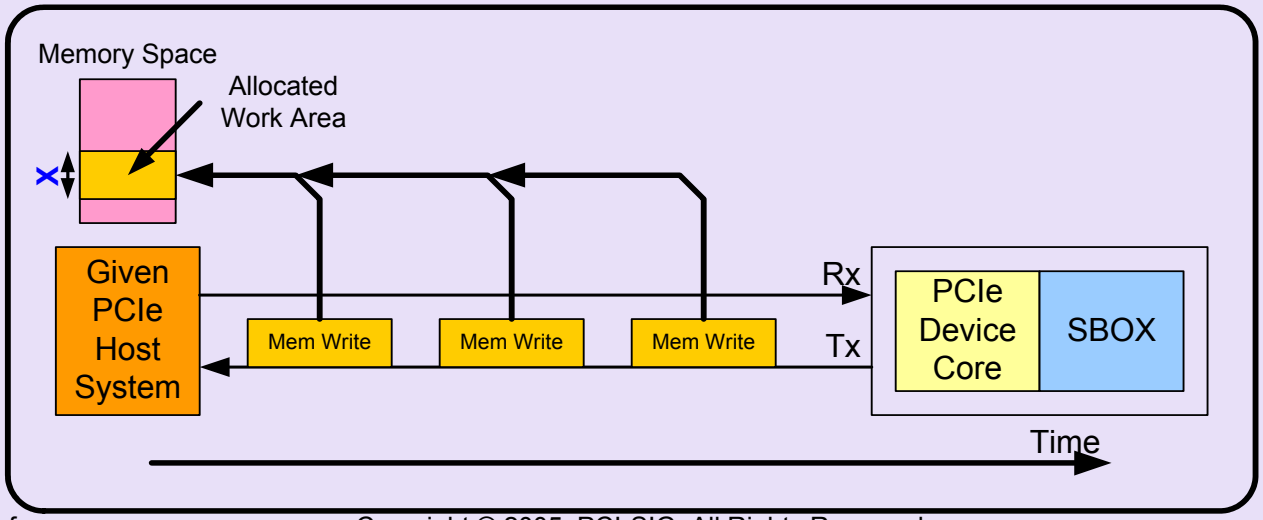
Required Function - Measurement of Time / Data -

- Consumed Time
  - ✓ Time Counter Starts Incrementing from First TLP
  - ✓ SysCLK Period * **m**
- Total Transferred Data Amount
  - ✓ Set Data Payload Size **X** (DW)
  - ✓ Set Repeat Count n
  - ✓ **X** (DW) * n

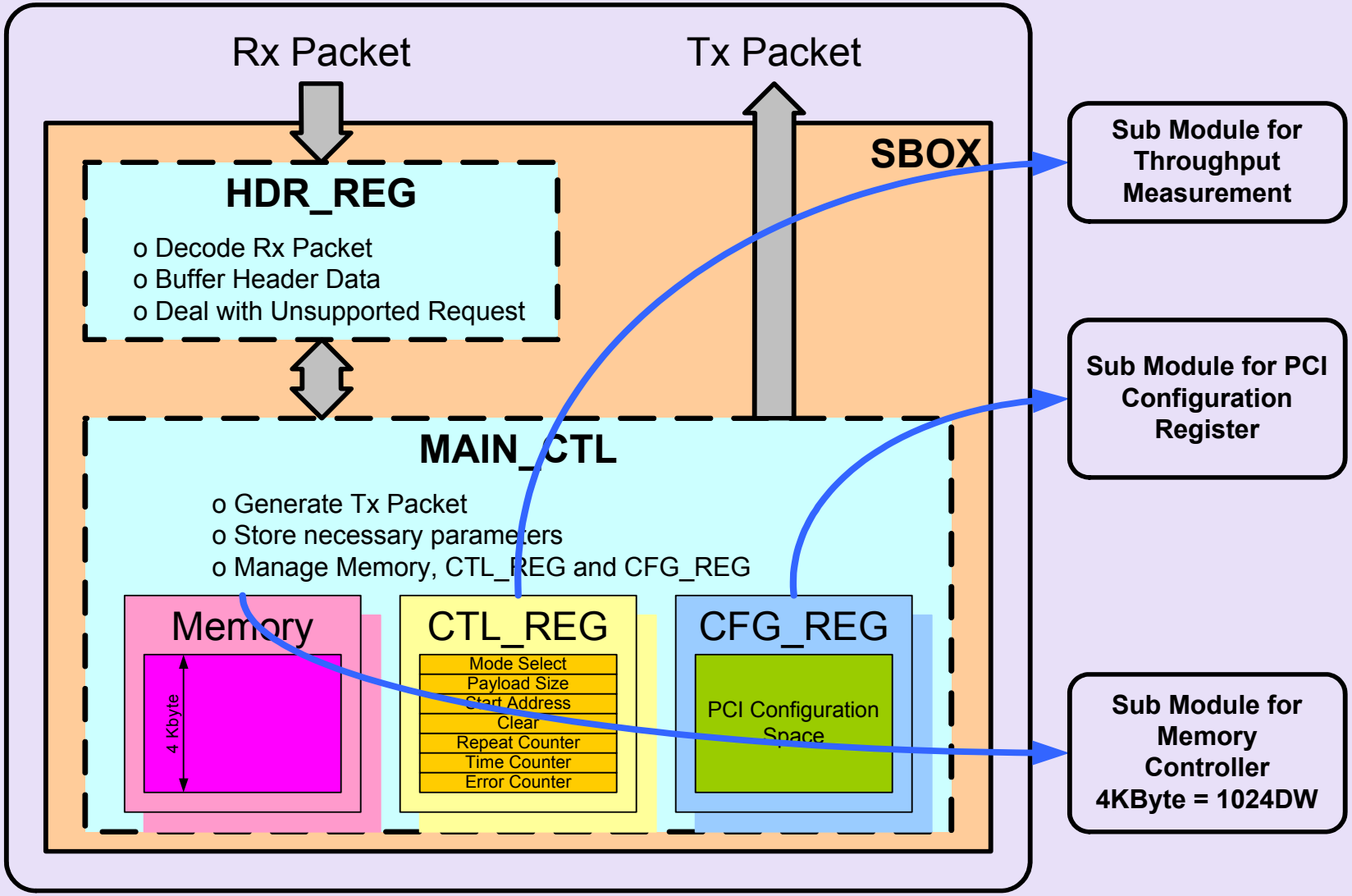


Required Function - Maximum Throughput -

- Issue Next Request As Soon As Both Host and Device are Ready
  - ✓ Fixed Allocated Work Area in Host
    - Write / Read Address is Always the Same in Every Request
    - No Need to Check Whether Address is Writable / Readable. Time Saving
    - No Worry to Break Host Systems



SBOX Block Diagram



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Overall Explanation of Evaluation

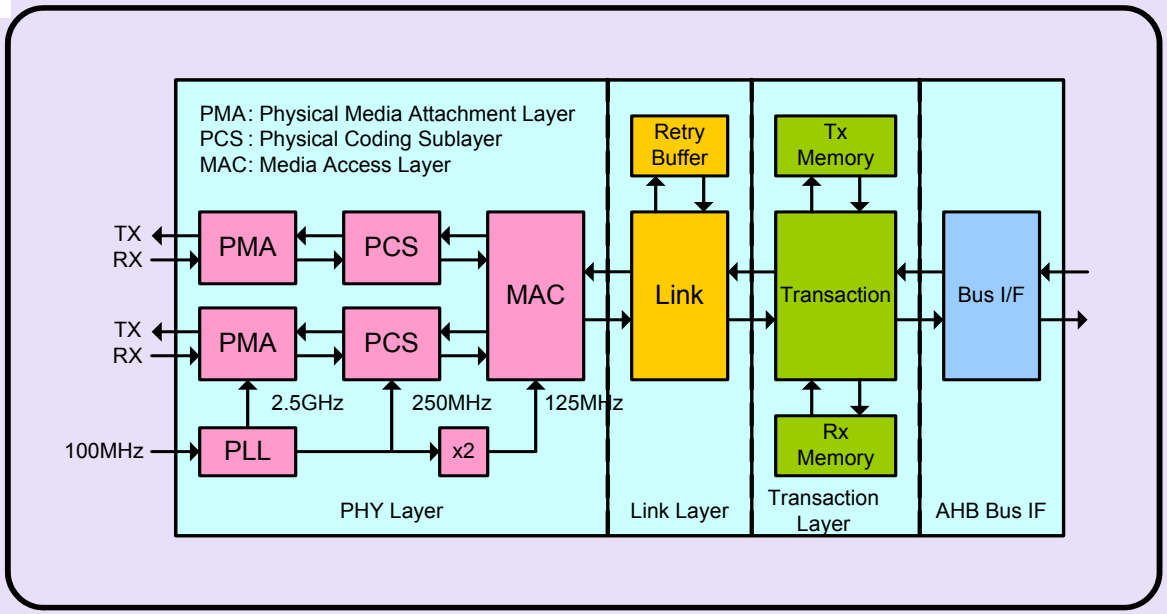
- 3 PC Systems with PCIe Host Controller
  - ✓ 3 Different PCIe Host Controllers
  - ✓ 3 Different CPUs
- Kawasaki's x1 PCIe Endpoint Controller
- Memory Read Requester Mode with Requested Data Payload Size from 1 DW to 1024 DW

Kawasaki IP Brief Explanation

No	Item	Description
1	Technology	0.13um Standard Cell 90nm Standard Cell (Under Development)
2	Macro	PHY : Hard Macro MAC, Link, Transaction, AHB Bus IF : Soft Macro
3	Lane	1 Lane, 2 Lane and 4 Lane

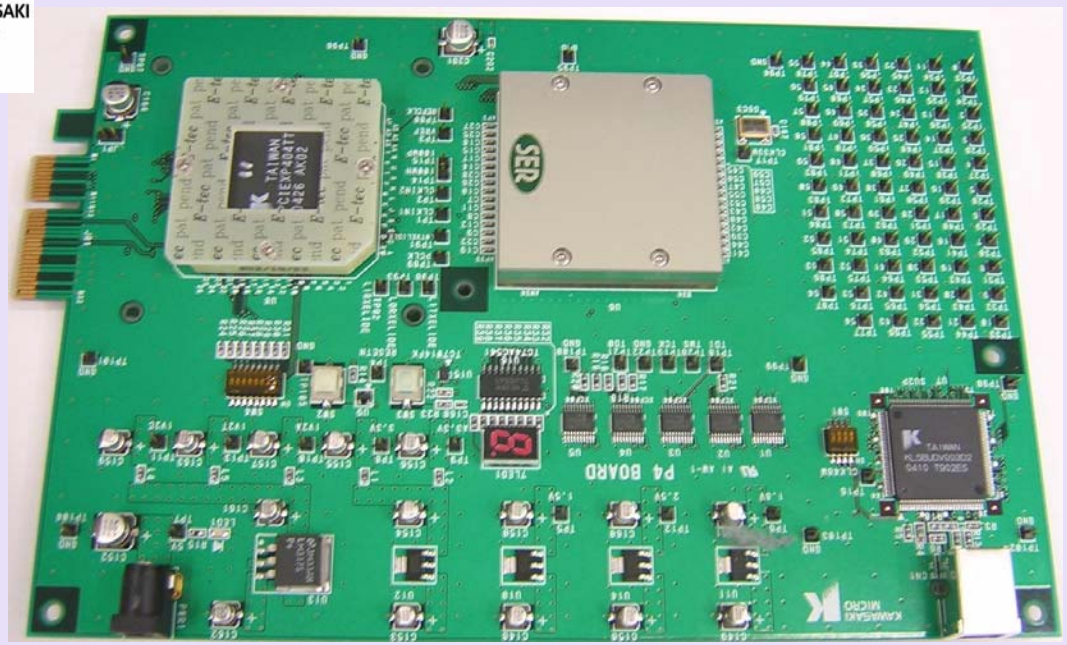
Kawasaki IP Explanation (Cont'd)

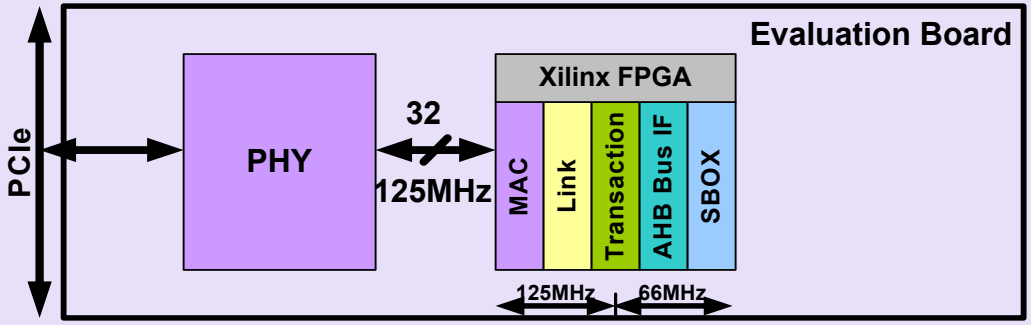
- In the case of 2 Lane



Evaluation Board

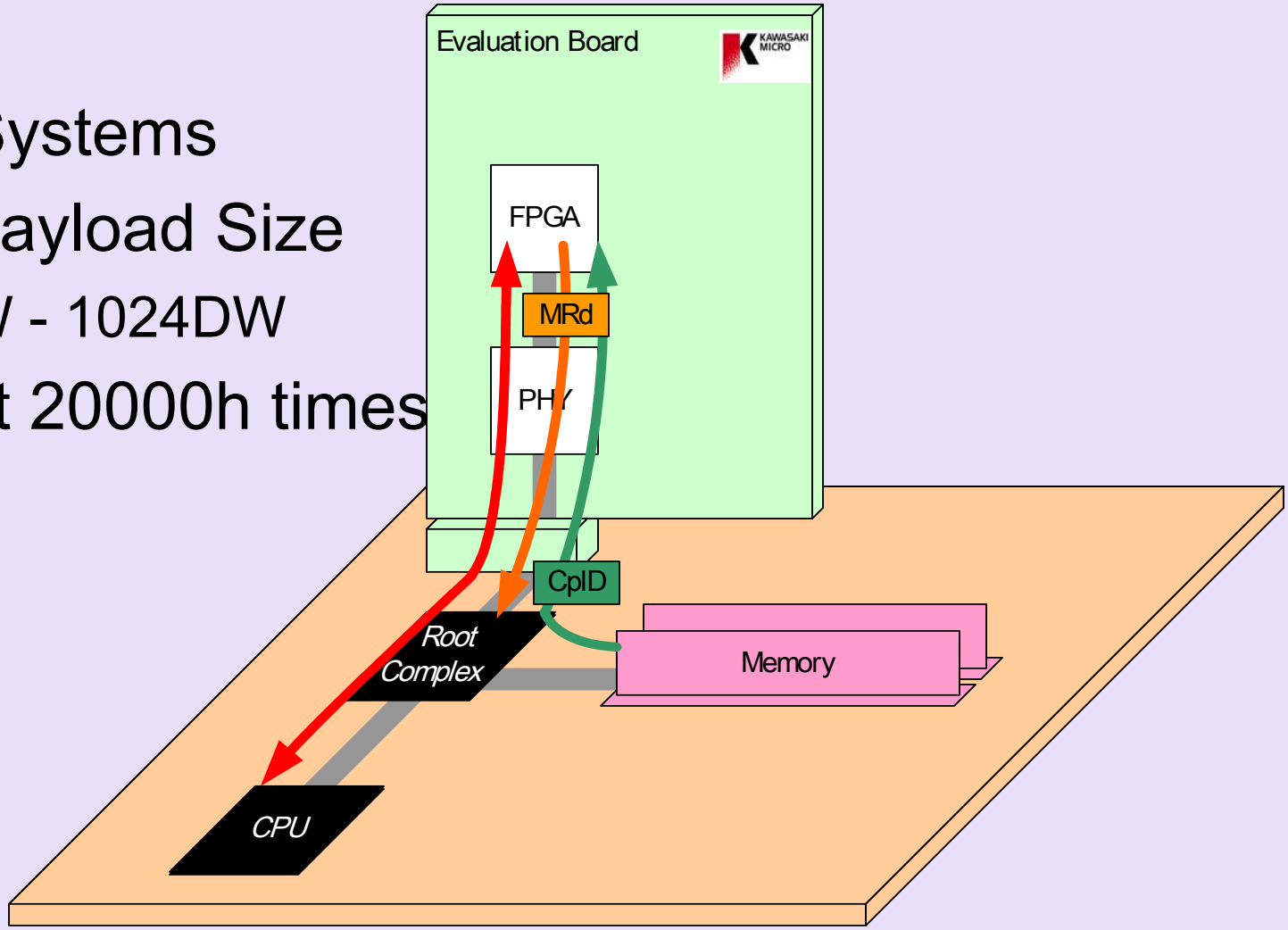
- PHY and Xilinx FPGA Only



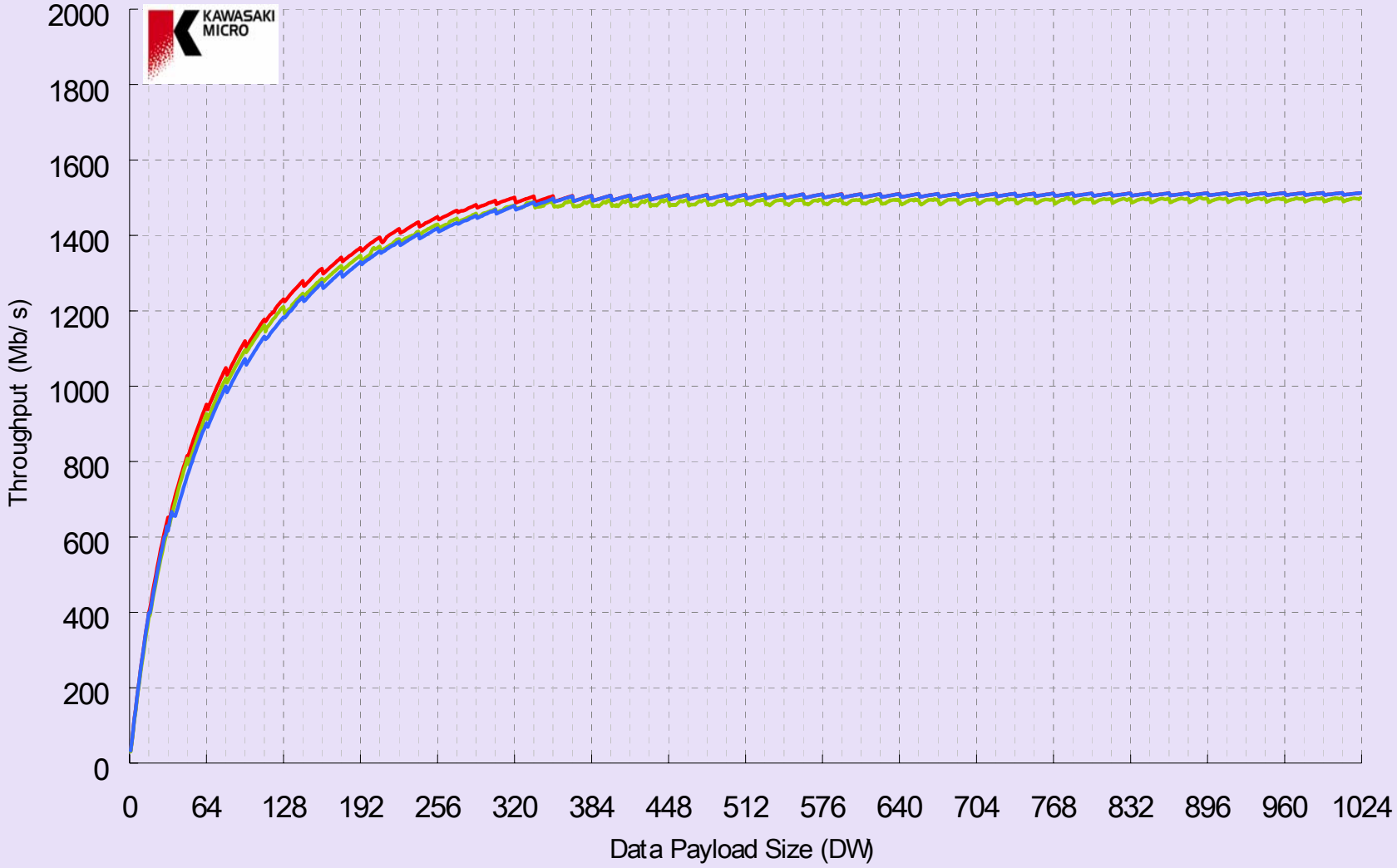


Evaluation System

- 1 Lane
- 3 PC Systems
- Data Payload Size
  - ✓ 1 DW - 1024DW
- Repeat 20000h times



Result
- 3 Different PC Systems -

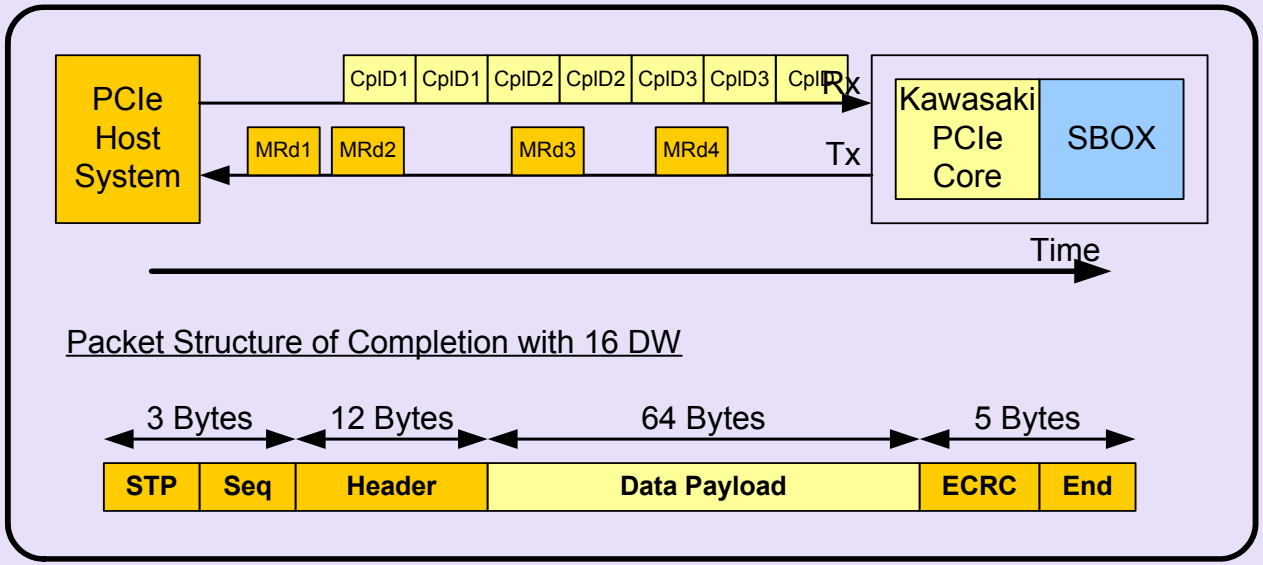


Analysis

- All Graphs Show Almost the Same Results
- According to Bus Analyzer Log, Multiple Completions returned to a Memory Read Request Over 16 DW.
  - ✓ This Causes Zigzag Shape of the Graphs
- Throughput Saturates at around 1.5G bps
  - ✓ Rx PCIe Bandwidth is Fully Utilized
  - ✓ Explanation in Next Slide

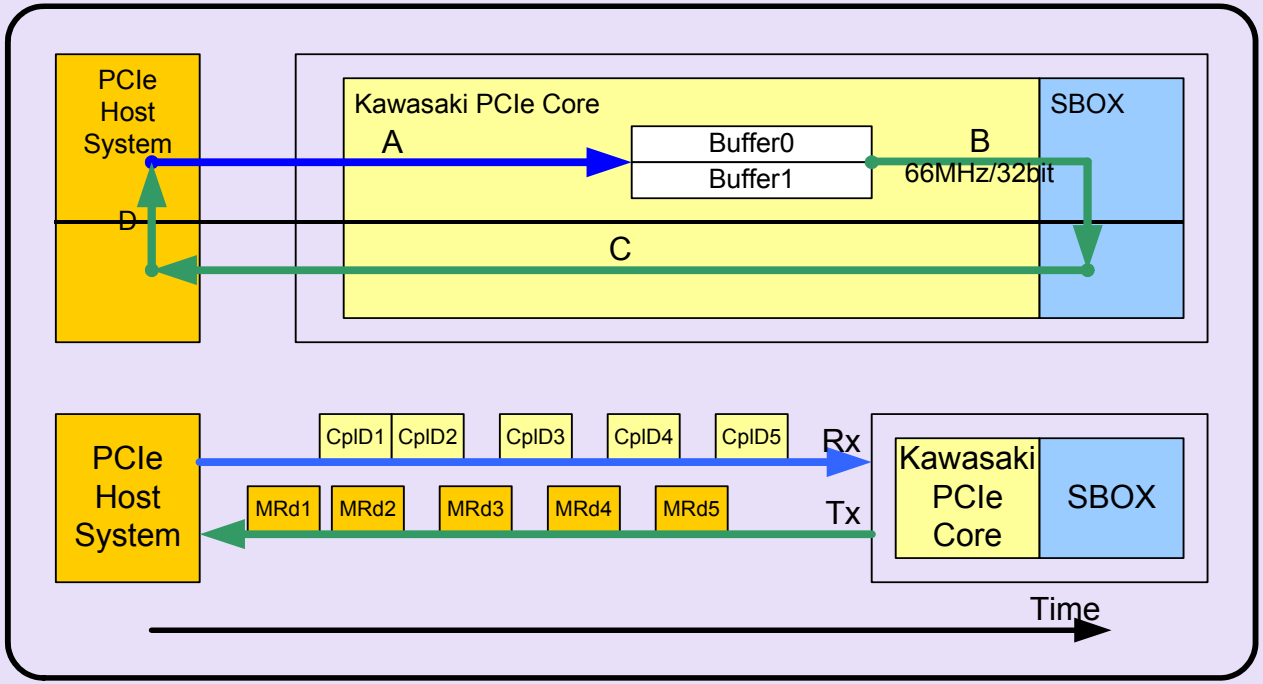
Analysis - Saturation at 1.5G bps -

- Maximum Throughput When Rx PCIe Bus is Filled with Multiple Completions with 16 DW
  - ✓ Around 1.5G bps
    - 2.0G bps * 64 / 84 = 1.524G bps



Analysis - Result Less Than 350 DW -

- Rx Path is Not Filled with Completions.
- Issuance of Next Memory Read Request is Not Fast Enough to Fill Rx Path with Completions.



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Summary

- Useful Technique for Throughput Measurement
  - ✓ Maximum Possible Throughput
- Throughput of 1.5G bps is Obtained in Memory Read Requester Mode

Thank you for attending the
PCI-SIG Developers Conference 2005.

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