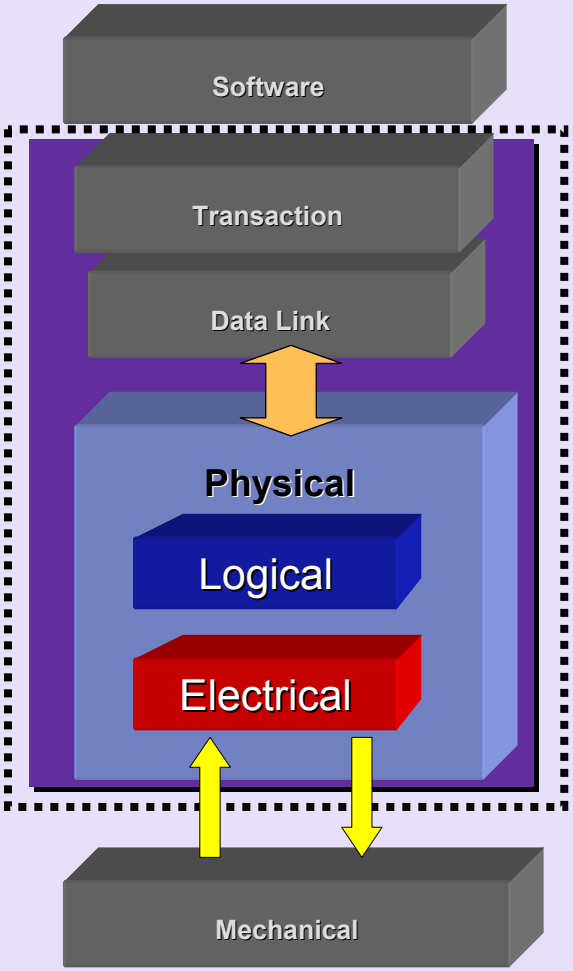
PCI Express® 1.1 Electricals & Jitter Considerations

Beijing	April 12, 2005
Tokyo	April 15, 2005
Taipei	April 18, 2005

PCI Express Physical Layer

- **PCI – PHY is digital in nature**
  - ✓ Parallel multi-drop bus
  - ✓ Bits, a clock, setup and hold times…
    - – Jitter essentially ignored
- **PCI Express – PHY is analog in nature**
  - ✓ Based on serial technology
  - ✓ Techniques developed by the communication industry
- **A transition for microprocessor based systems**
  - ✓ Microwave theory/physics challenges dominate
  - ✓ Two PLLs communicating directly

PHY Layer Design Basics

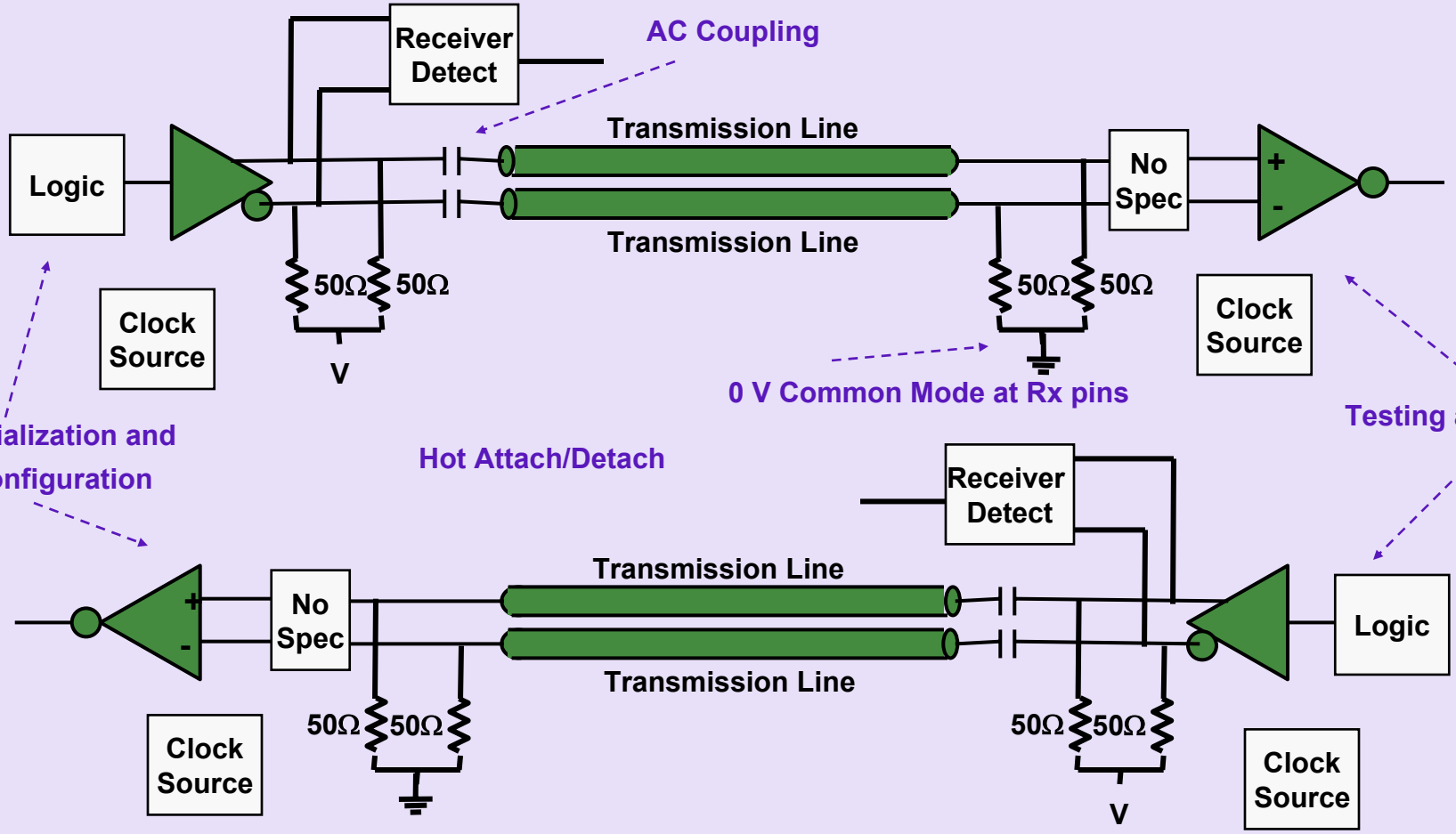


- **Logical Functions**
  - ✓ Encoding/decoding/scrambling
  - ✓ Reset, initialization, de-skew
  - ✓ Built in test modes
  - ✓ Configuration:
    - Speed, link width, lane mapping, Polarity
  - ✓ Link power management

- **Electrical Functions**
  - ✓ Transmitter/receiver
  - ✓ Clocks/PLLs
  - ✓ Clock/data recovery

PHY layer upgrades do NOT impact upper layers

Pictorial Summary

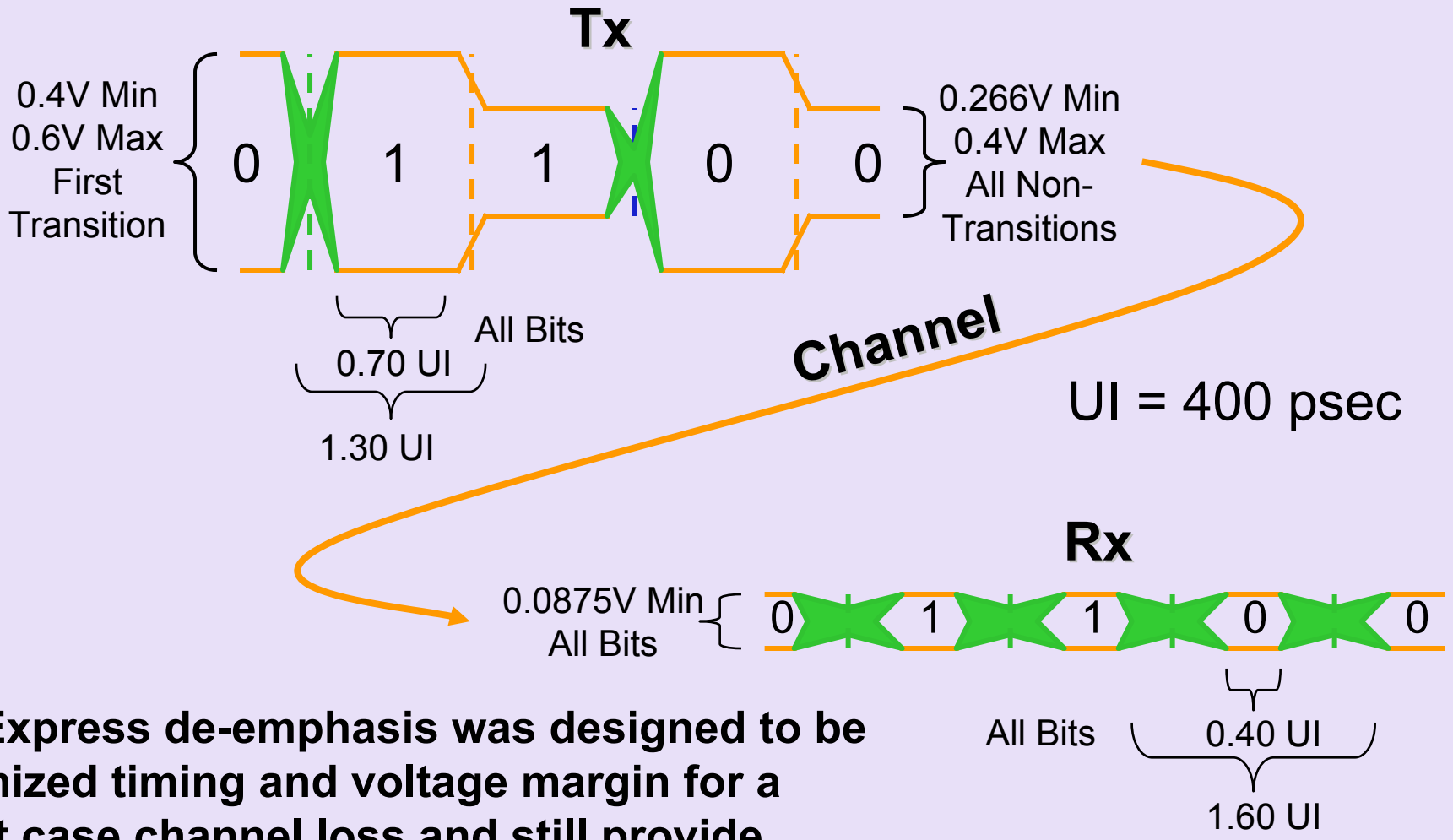


Emphasis on Low Power

ESD, EMI, Noise Suppression

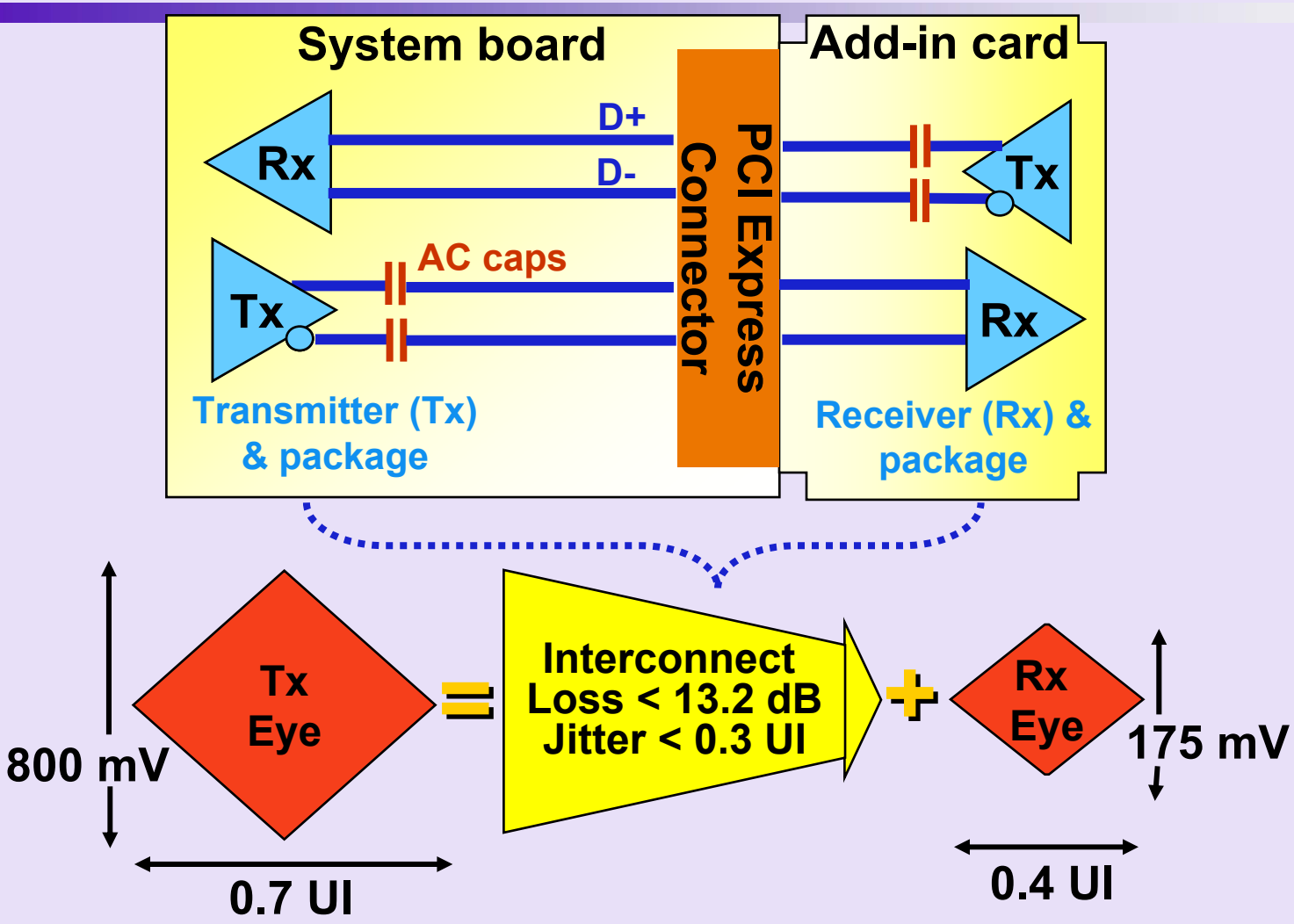
Error Behavior/Recovery

Electrical Specifications



PCI Express de-emphasis was designed to be optimized timing and voltage margin for a worst case channel loss and still provide adequate margin for the best case channel loss

System Budget

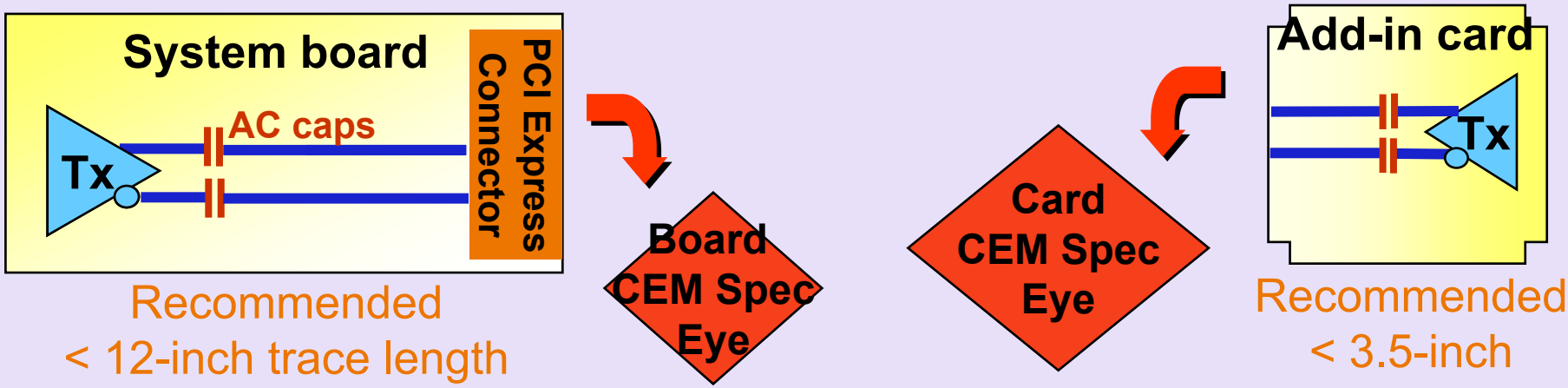


- ✓ Differential pairs
- ✓ AC coupled
- ✓ Lane-to-lane de-skew
- ✓ Polarity inversion
- ✓ On-chip equalization
- ✓ On-chip terminations

UI = Unit Interval as defined in the PCI Express Base 1.0a Specification

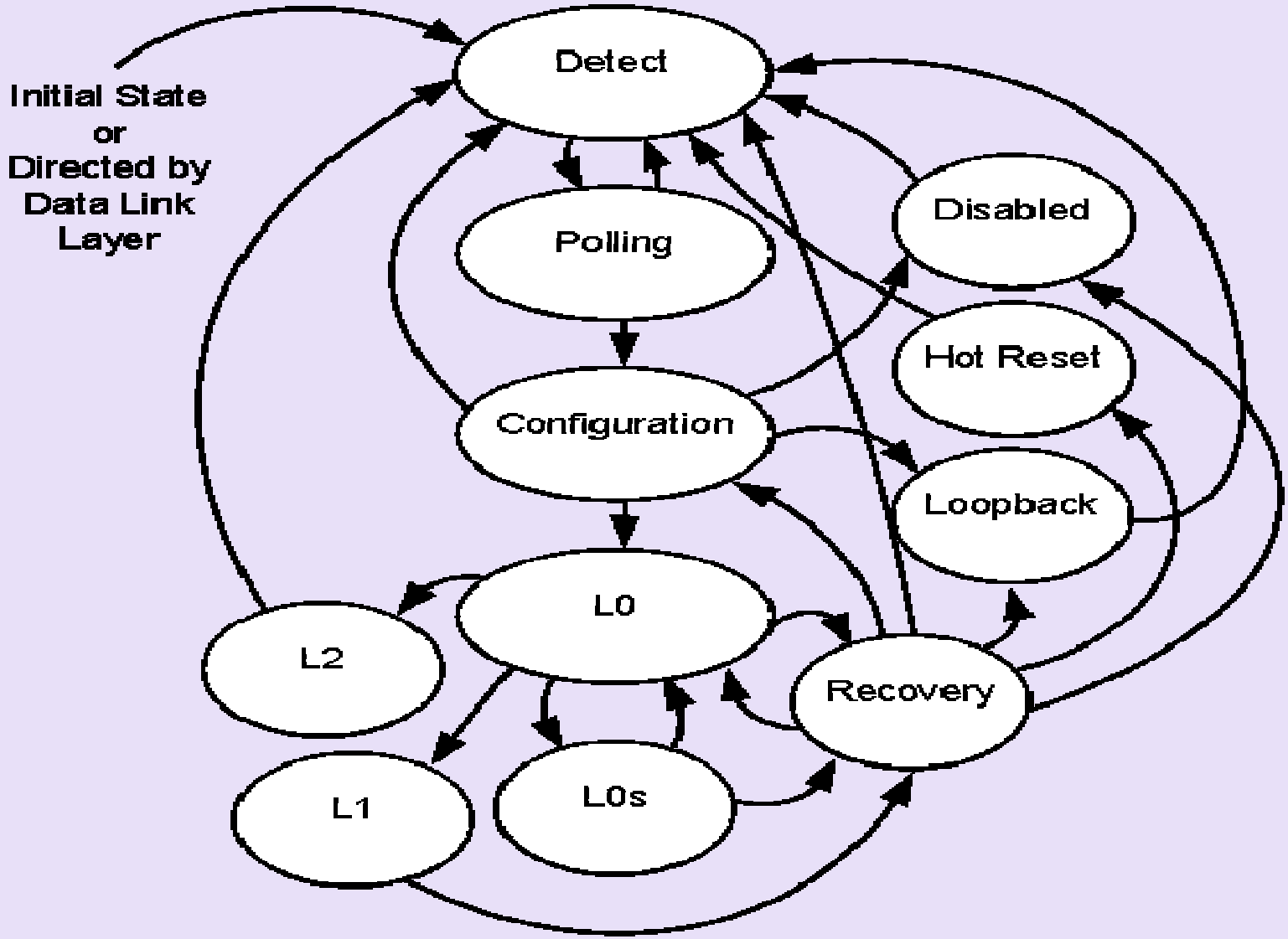
Card Electromechanical Interconnect Budget

- **Card Electromechanical (CEM) 1.0a specification defines budget allocation**
  - ✓ *Loss* and *jitter* are key parameters
  - ✓ Target impedance not as critical
  - ✓ Maintain differential pair symmetry
  - ✓ Design tradeoffs: loss vs. trace length, etc.



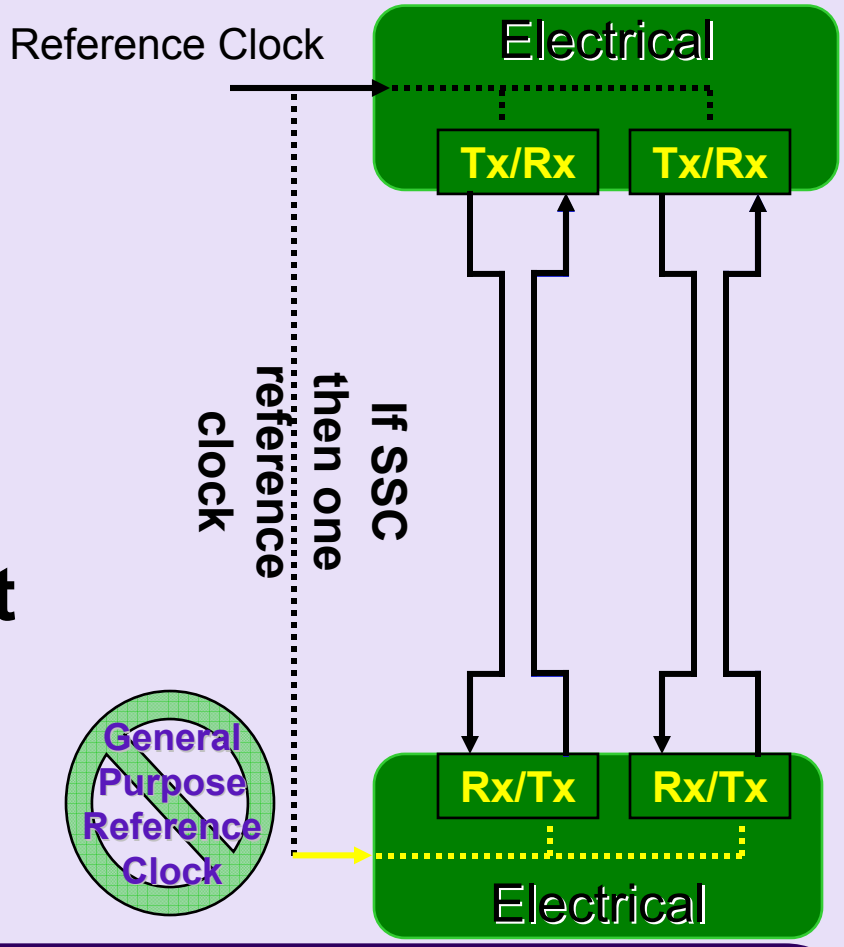
Manage loss & jitter to meet budget

Link Training & Status State Machine



Clocking Options

- **All lanes within a port must transmit data using one frequency**
- **The ports at each end of a link may transmit data at slightly different frequencies**
  - ✓ Tolerance = ±300 ppm each

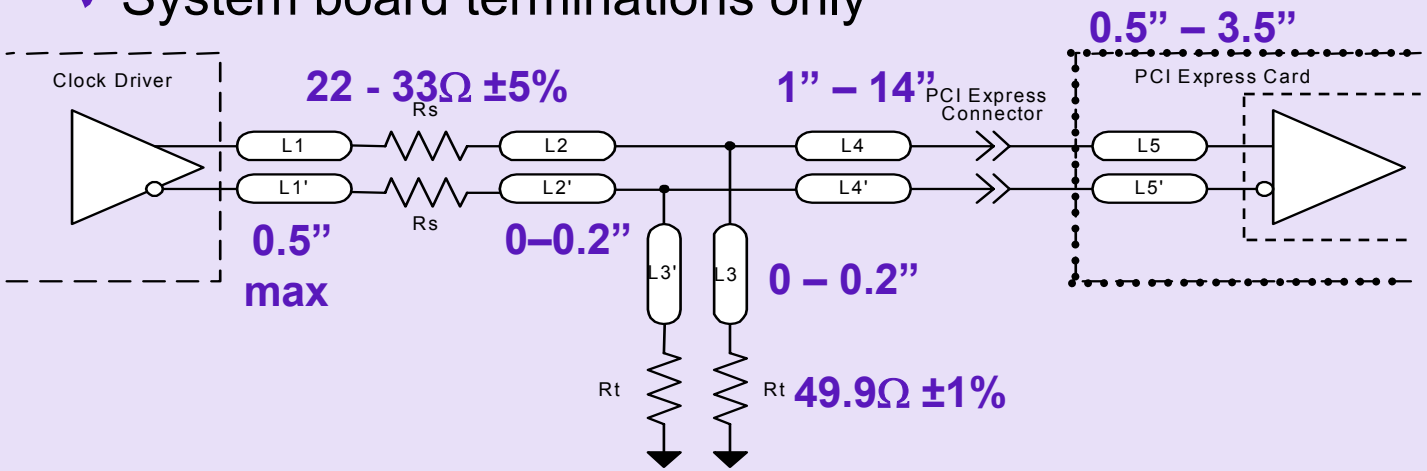


If SSC used to modulate data rate, then both ports must use same modulated clock source

Reference Clock Routing

- **Differential clock routing to each device and connector**
  - ✓ Use the same differential trace geometries
  - ✓ Length matching to different devices *NOT* required!

- **Clock driver requirements**
  - ✓ 100MHz with SSC support (e.g. CK410)
  - ✓ Choose low jitter components
  - ✓ System board terminations only



PCI Express BER/Jitter Overview

- **Base Specification Changes**
  - ✓ New clock recovery function for measuring eye diagrams
  - ✓ PLL bandwidth restrictions
  - ✓ Tx eye budget reduction
- **CEM Specification Changes**
  - ✓ Rj / Dj tables and new budgets
  - ✓ Implied Rx tolerance mask
  - ✓ Reference clock specification and sample sizes
  - ✓ Base board measurement with “dirty” reference clock

These changes are in PCIe 1.1 specifications

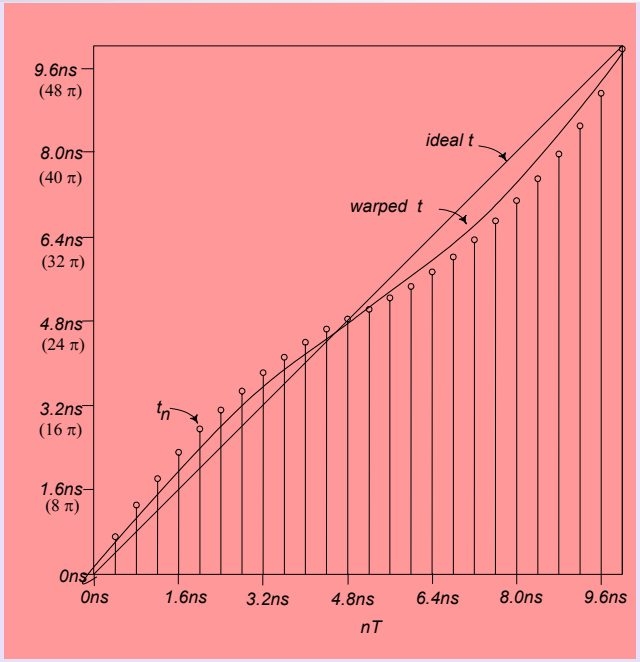
New Clock Recovery For Eye Measurement

- The estimate of the ideal clock, T, in the phase jitter is the clock recovery

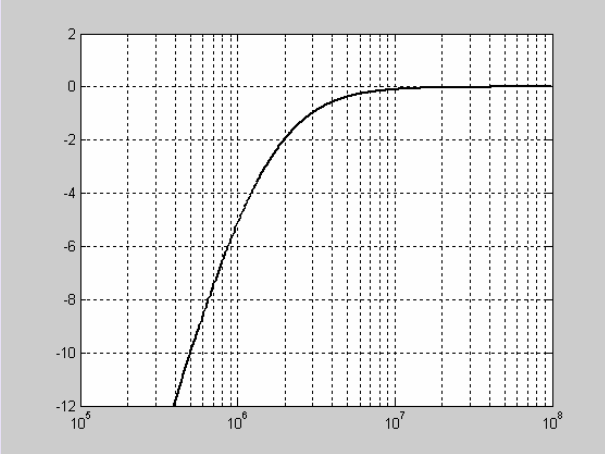
$$\Phi_n = t_n - nT, \quad n = 1, 2, \ldots, \infty$$

- Recovery can be done in T or in Φ
  - ✓ Matlab code in jitter whitepaper that applies it in Φ(s)
  - ✓ It can also be done as a sliding window using average T and looking across 416 UI

$$H_3(s) = \frac{s}{s + 2 * \pi * 1.5e6}$$



- This implies the minimum required performance of the data recovery circuit (DRC)



Jitter Method Frequency Response

- Produce Crossovers With Jitter At A Single Frequency
  - ✓ C_n = n*UnitInterval+JitAmp*sin(2π*n*UnitInterval*JitFreq)
- Peak to Peak Jitter = 2* JitAmp
- Analyze Data And Obtain JitterResult
- Compute Log_{10} (JitterResult/(2*JitAmp))
- Repeat For Frequencies Throughout Range Of Interest

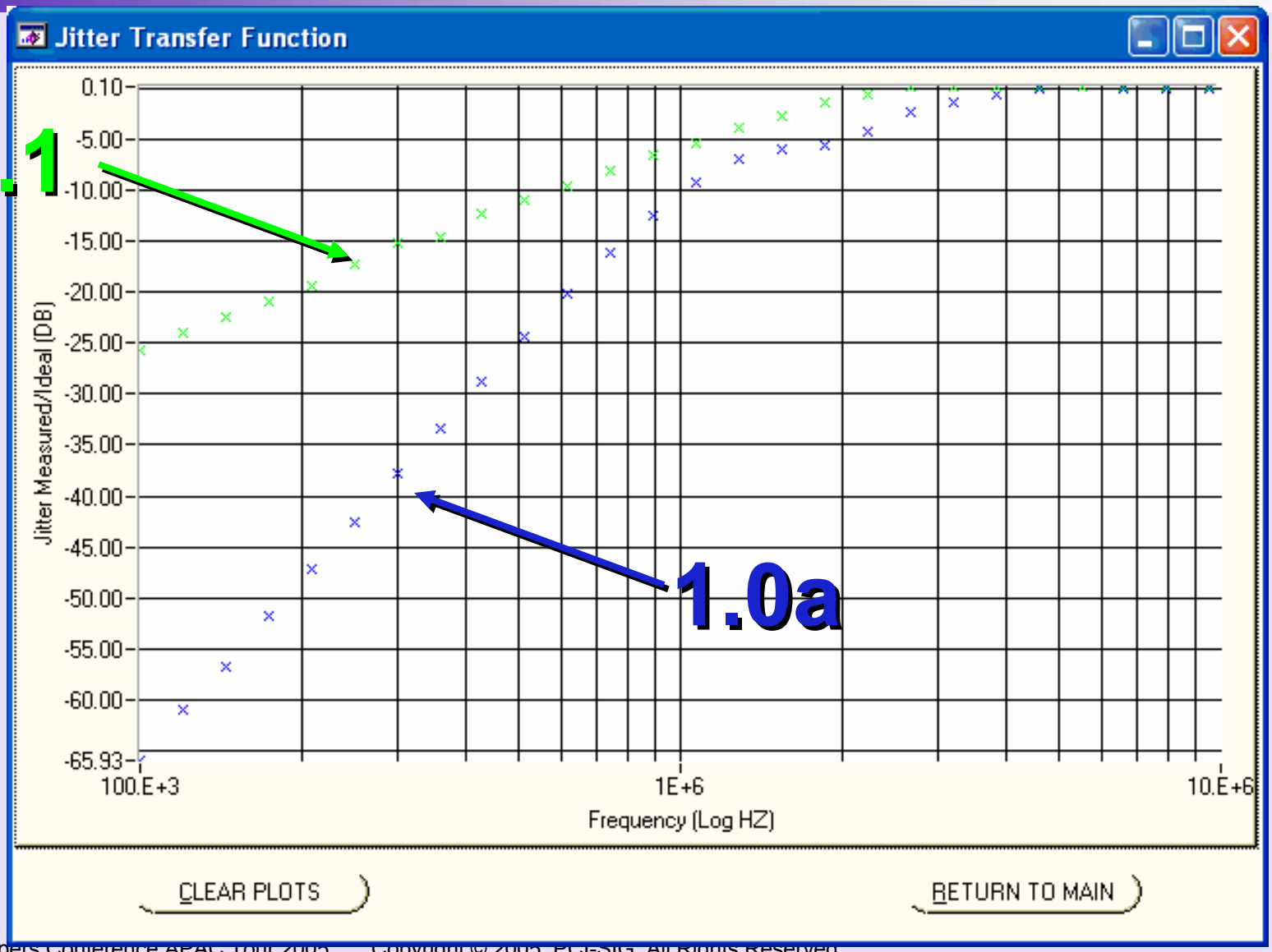
Assumes that frequency response is not amplitude dependent

Demo

1.0a Transmitter Jitter Method Frequency Response

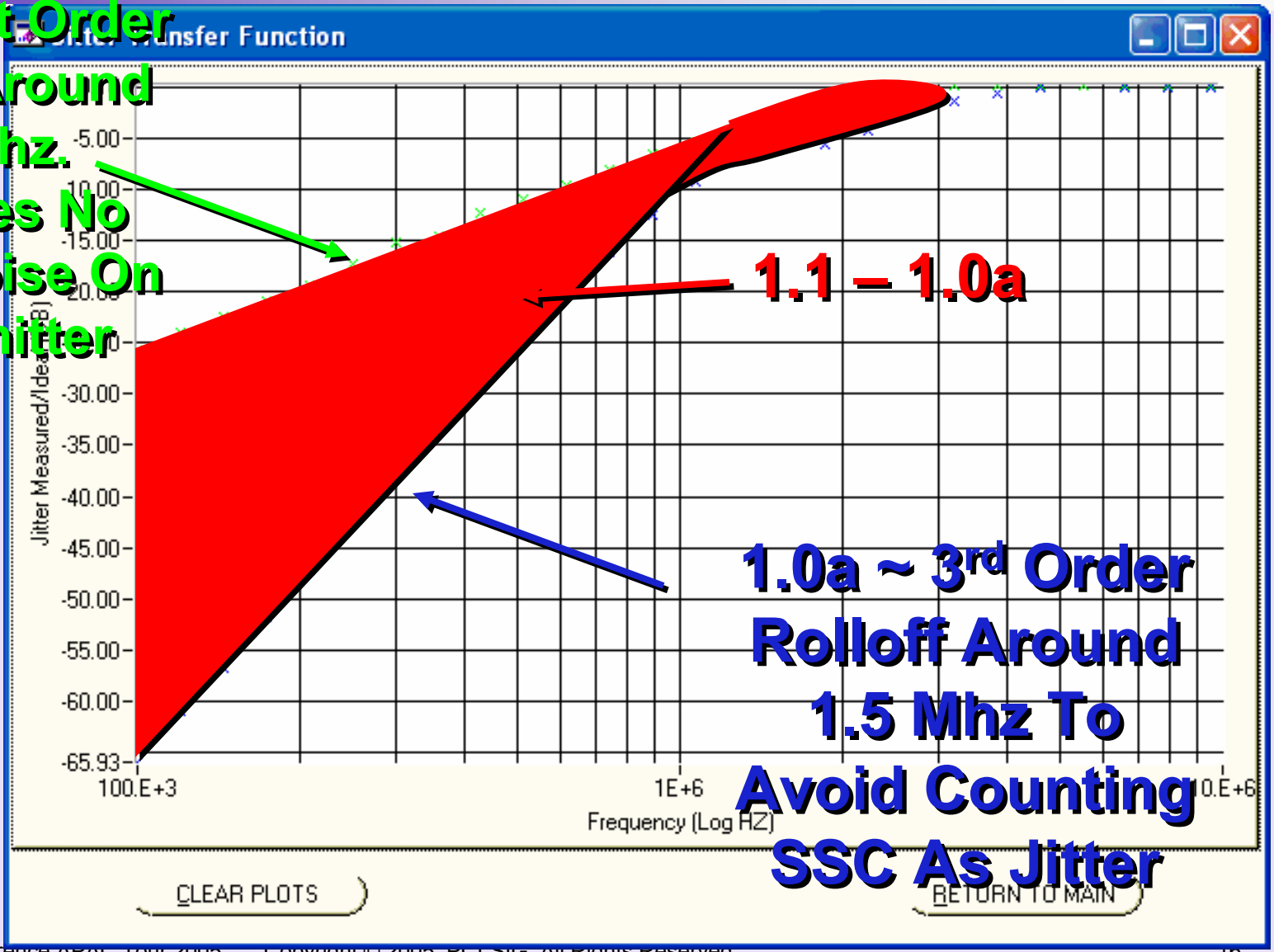
1.1 Transmitter Jitter Method Frequency Response

Frequency Response – 1.0a/1.1



Response Delta – 1.0a/1.1

1.1 ~ First Order Rolloff Around 1.5 Mhz. Assumes No Clock Noise On Transmitter



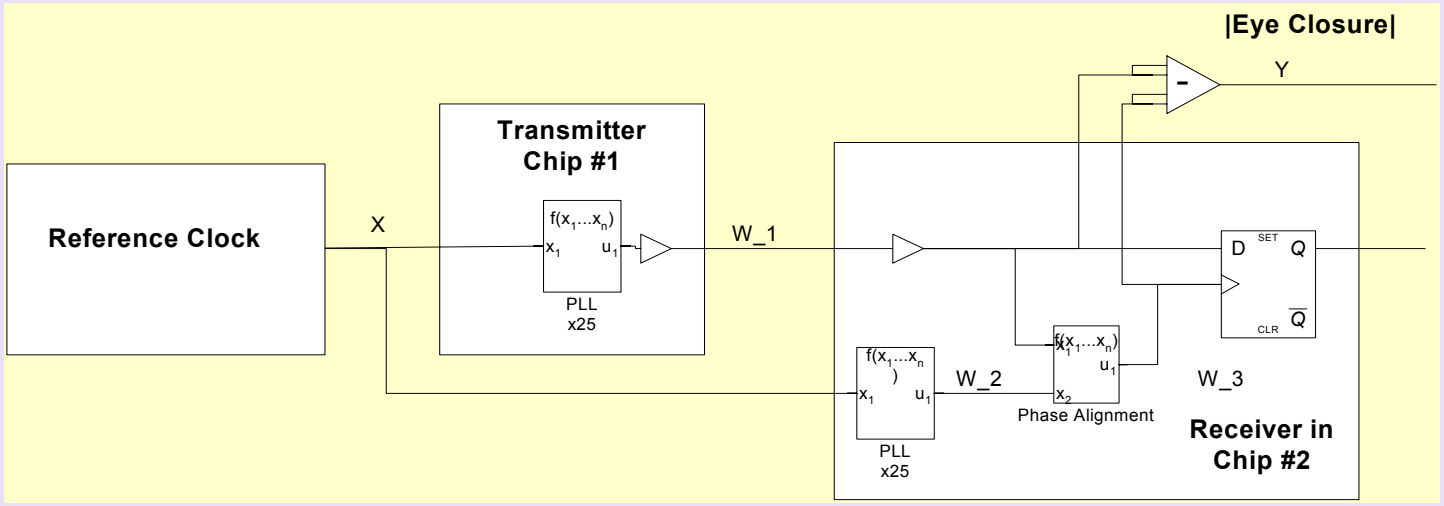
1.1 – 1.0a

1.0a ~ 3rd Order Rolloff Around 1.5 Mhz To Avoid Counting SSC As Jitter

Tx PLL Bandwidth Restrictions

- **Tx PLL bandwidth is between 1.5 and 22 MHz, peaking < 3dB**
  - ✓ **Based on second order transfer function**

- **Rx is implementation specific**



Tx Eye Reduction

- Tx reduction from 120 ps to 100 ps
  - ✓ At 10^-12 BER
- Eye measurements are to be done with a “clean” clock
- The median to max measurement is over 1e6 samples using the compliance pattern

CEM System Budget

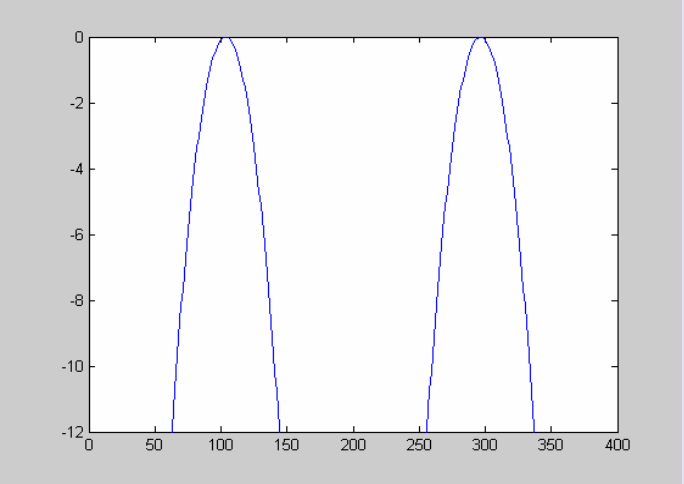
- **Minimum Rj assumptions have been taken for the Tx, reference clock and the "Internals" of the Rx**
- **These Rj terms are convolved to achieve the total system budget**
- **This is then extrapolated to 10^-6 for the CEM and compliance numbers**

Jitter Contribution	Min Rj (ps) one sigma	Max Dj (ps) P-P	Tj at BER 10^{-12} (ps)	Tj at BER 10^{-6} (ps)
Tx	**2.8**	**60.6**	**100**	**87**
Ref Clock	**4.7**	**41.9**	**108**	**86**
Media	**0**	**90**	**90**	**90**
Rx	**2.8**	**120.6**	**160**	**147**
Linear Total Tj:			**458**	**410**
Root Sum Square (RSS) Total Tj:			**399.13**	**371.52**

New CEM Jitter Budgets At Connectors (TJ at 10^12 bits)

	System Connector Jitter Limit (PP)	Add In Card Edge Fingers Jitter Limit (PP)
1.0a	**217**	**163**
1.1	**167**	**126**

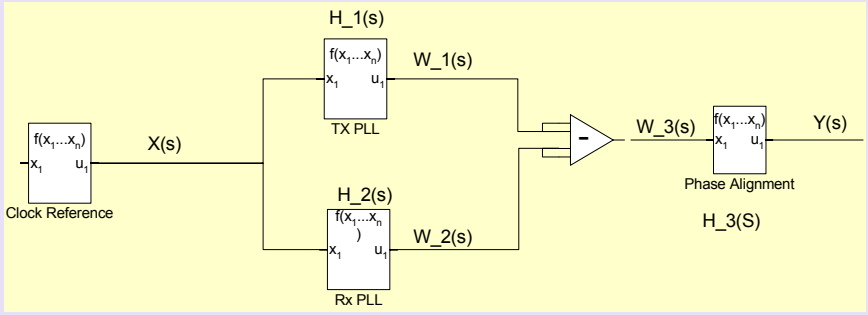
Implied Receiver Tolerance Mask

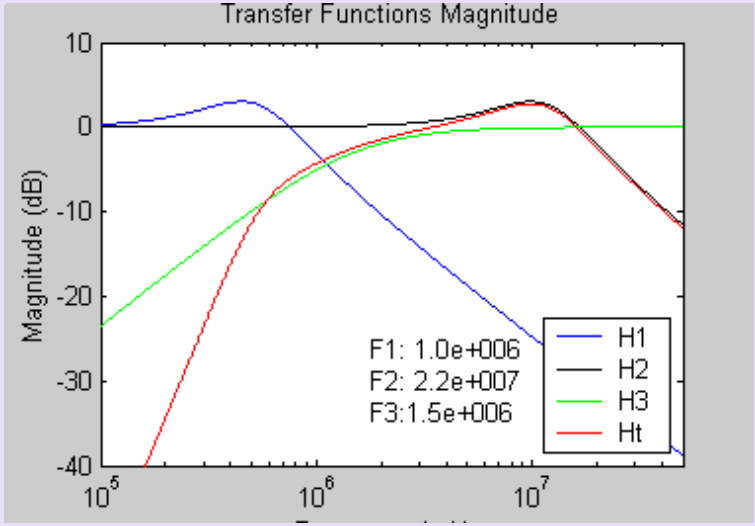


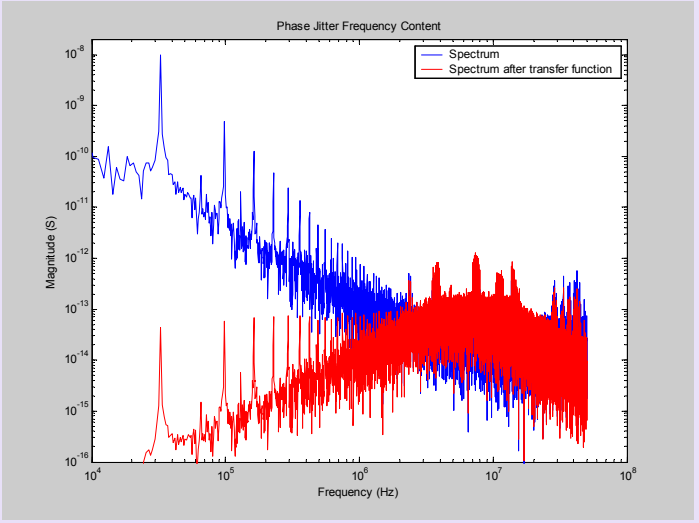
- Apply 193 ps of Dj
- Apply 5.4 ps of Rj
- BER of 10^-12 should be met at the sample size tested
- More detail to follow in white paper

Reference Clock Specification

- **The reference clock phase jitter is less than 86 ps**
  - ✓ **After the (H1 – H2) * H3 transfer function has been applied**
  - ✓ **H1 = 1.5, H2 = 22, second order**
    - **3 dB peaking**
  - ✓ **H3 = 1.5 MHz, first order**
  - ✓ **Delay of 10 ns added to H1 for transport delay**







Reference Clock Jitter Algorithm

- Produce Interval Array
- Perform FFT Of Intervals
  - ✓ FFT Removes DC Offset
  - ✓ Effectively Removes Average Interval
- Apply Jitter Transfer Function In Frequency Domain
- Perform Inverse FFT
  - ✓ Data Is Now Interval Deltas From Average Interval After Frequency Transformation (Data)
- Integrate Data
  - ✓ $IntData_n = IntData_{n-1} + Data_n$
- Peak Peak Jitter
  - ✓ Max (IntData) – Min (IntData)

Method can also be used for transmitter data with small changes

Demo
Reference Clock Jitter Calculation

BER/Jitter Summary

- The Tx specification is to be made with a clean clock
- The Tx bandwidth range and peaking is limited
- The reference clock phase jitter is limited
- The total system budget includes the convolution of Rj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