Signal Integrity Challenges and Design Practices on a Mobile Platform

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Agenda

- Overview
- Mobile platform focused requirements
- Impedance optimizations
- Rx / Tx Routing optimization
- Layer transition optimization
- Summary

Overview

- As the industry moves to PCI Express® 2.0, boosting data-rates from 2.5GT/s to 5GT/s, we look at some key factors affecting mobile-platform signal integrity and suggest design practices on the silicon package and Printed-Circuit-Board to overcome these challenges.
- Some of these strategies* include:
  - ✓ Adjusting board and package impedances in order to optimize signal integrity and board routing for dense mobile-platform layouts
  - ✓ Assessing the impact of transmitter/receiver interleaved, semi-interleaved, and non-interleaved routing on the board and package
  - ✓ Considering the impact of via stubs/routing layers to optimize performance on a mobile platform

*These are recommendations of the authors of this presentation and are not PCI-SIG® specifications

Mobile Focused Requirements

- Focus on low-power
  - ✓ Need for low swing drivers
- Implemented on boards with multiple layers
  - ✓ Non-interleaved routing is a good option
  - ✓ Need to optimize layer transitions
- Compact mobile designs require focus on tight routing
  - ✓ Optimizing the differential impedance target on package and channel

Impedance Optimizations

Impedance Optimizations

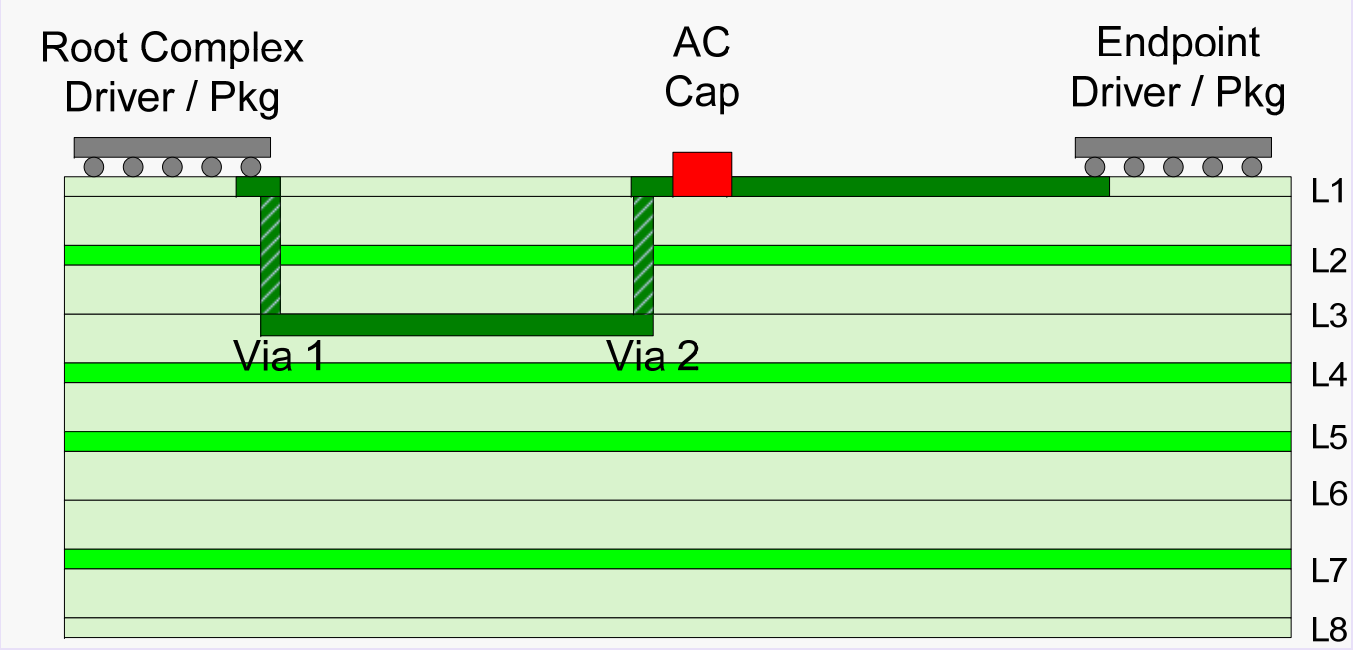
- Analyzed various differential impedance targets on the root complex package, the motherboard, and the endpoint package on the motherboard at 5GT/s

	Root Complex Pkg	Motherboard Pkg	Endpoint Pkg
Case 1	85 Ω	85 Ω	85 Ω
Case 2	90 Ω	90 Ω	90 Ω
Case 3	95 Ω	95 Ω	95 Ω

- Need to select the optimal impedance for signal integrity and routability

Case Study Topology

- Considered single routing topology with a combination of stripline and microstrip routing
- Simulated 1 – 10” on the motherboard
- Set the driver and receiver termination values to 100 Ohms differential while changing the package and channel impedance to 85ohms

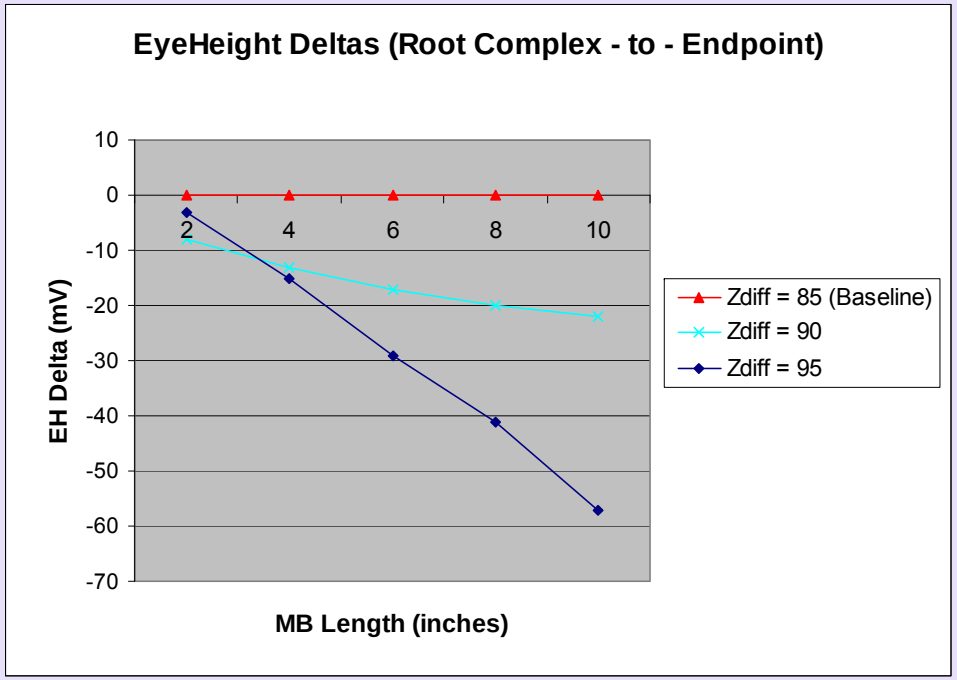


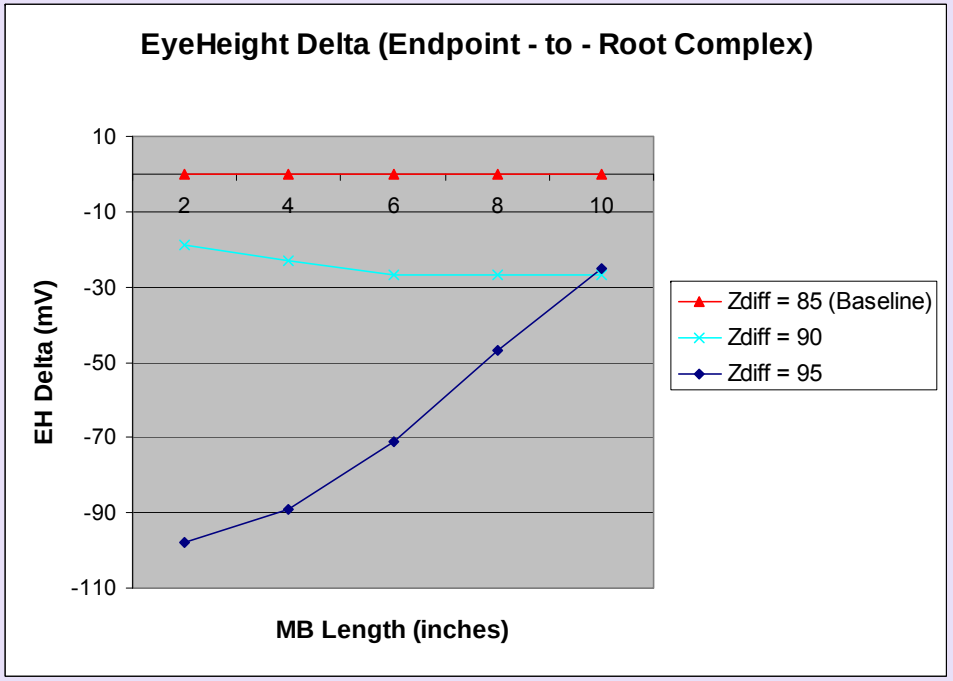
Example Root Complex: CPU/Chipset

Example Endpoint: Discrete GFX device

Impact on Eye Height

- Matching 85Ω differential impedance for the motherboard and packages consistently provides higher eye height margins
- Charts below show the delta in margins with 85Ω as the baseline:





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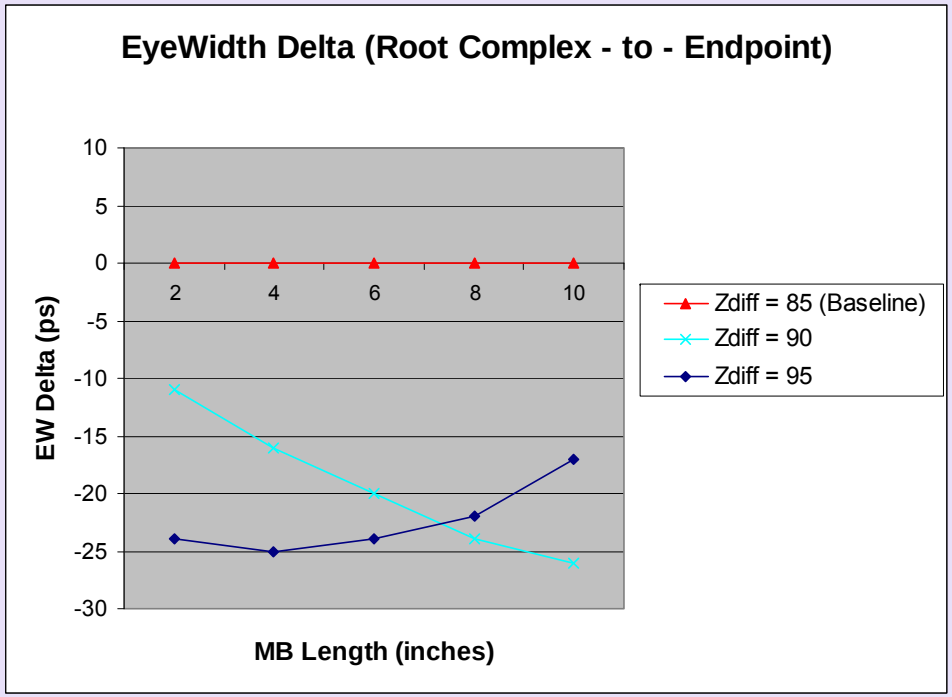
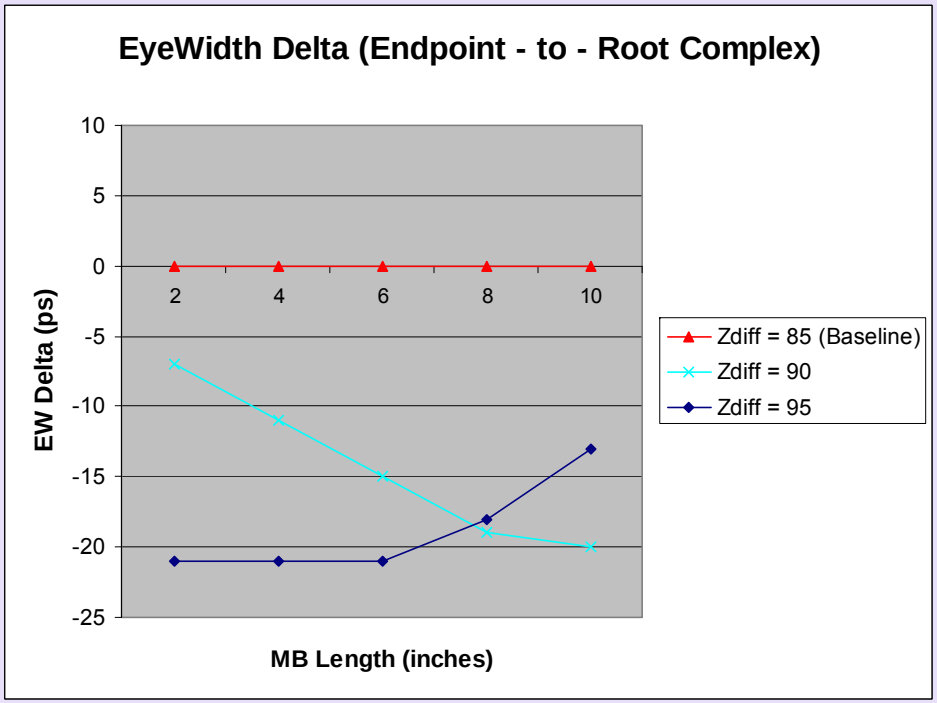
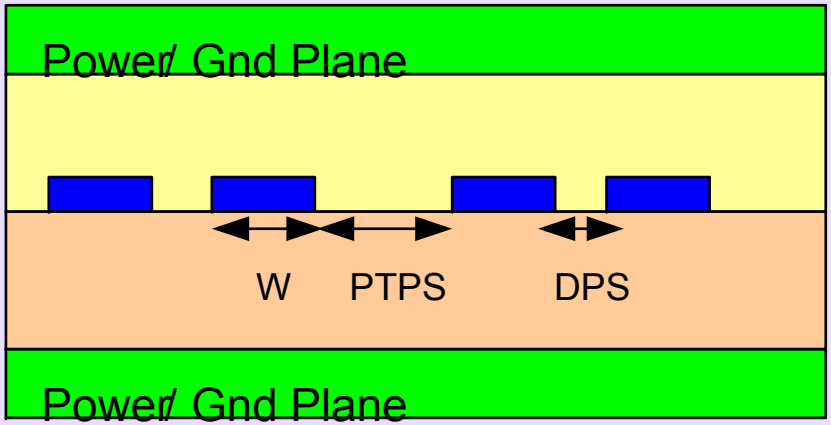




Impact on routability



- W: Trace width
- PTPS: Pair to pair spacing
- DPS: Differential pair spacing

- Lowering the differential impedance on motherboard from 100 Ω to 85 Ω reduces the PTPS by ~25% and DPS by ~45%
  - ✓ Saves real estate on board
  - ✓ Enables smaller form factor designs

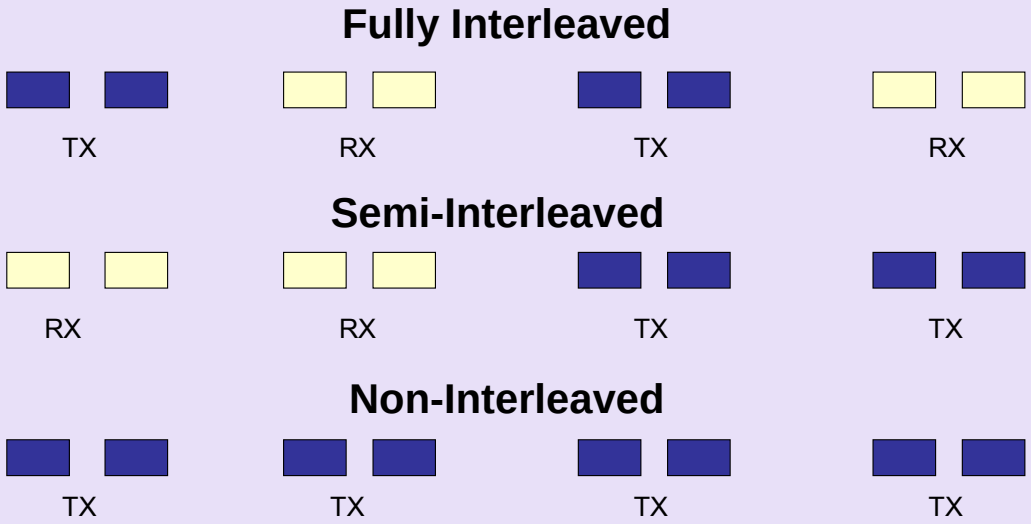
Summary

- 85Ω package + channel differential impedance provides optimal eye width and eye height
- 85 Ω also allows for tighter differential pair spacing which is better for routability on both the package and motherboard
- As power is a concern on mobile platforms, assuming 85 Ω channel with100 Ω terminations helps maintain same power levels as that with a 100 Ω channel
  - ✓ Did not analyze 80 Ω on the motherboard due to difficulty in achieving this low impedance with mobile motherboard assumptions

Rx / Tx Routing Optimization

Rx / Tx Routing Optimization

- Designers should carefully consider their Rx / Tx routing configurations when doing layout



- Crosstalk from interleaved routing has a significant impact on signal integrity
- In a mobile platform, where multiple layers are available, motherboard routing should be non-interleaved
- Crosstalk from the package routing is also significant and its impact should be considered. The following experiments show that impact.

Rx / Tx Routing Optimization

- Analyzed various Rx / Tx routing configurations on the package and compared the impact on eye height / width and cross-talk levels for the channel operating at 5GT/s

	Root Complex Pkg	Motherboard	Endpoint Pkg
Case 1- NNN	Non-interleaved	Non-interleaved	Non-interleaved
Case 2- INI	Interleaved	Non-interleaved	Interleaved
Case 3- SNS	Semi-interleaved	Non-interleaved	Semi-interleaved
Case 4- INS	Interleaved	Non-interleaved	Semi-interleaved
Case 5- NNI	Non-interleaved	Non-interleaved	Interleaved

Case Study Topology

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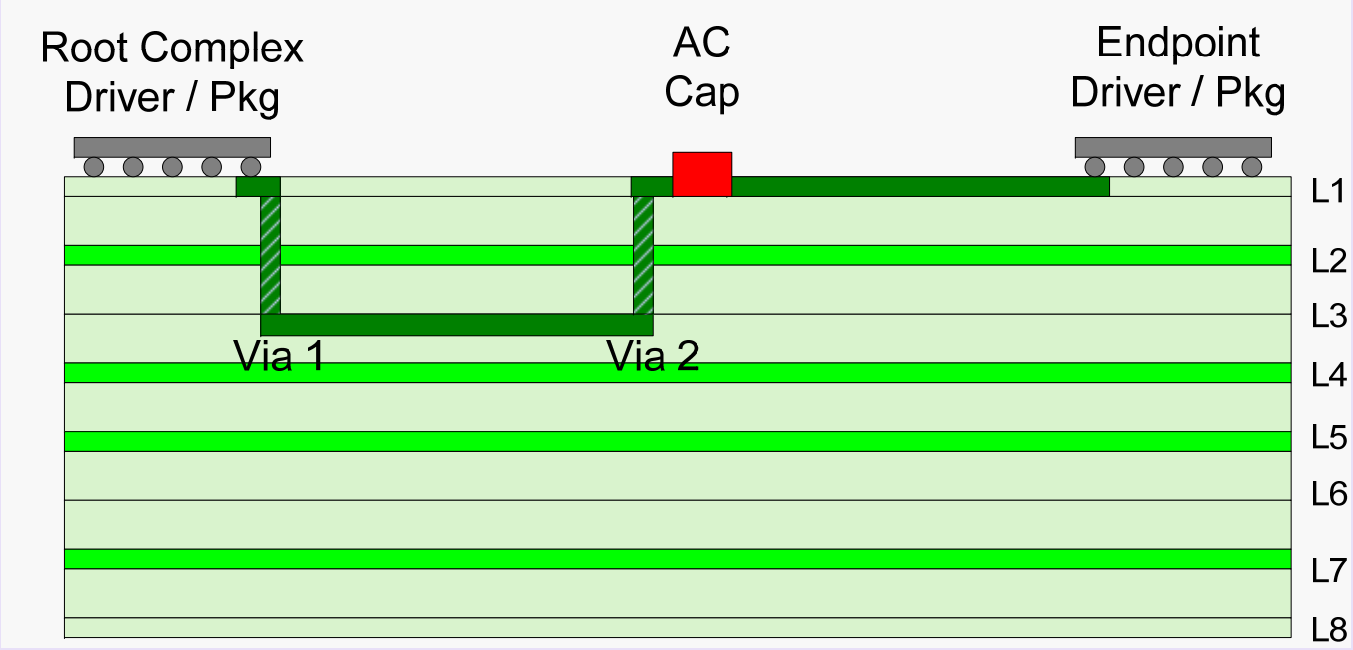
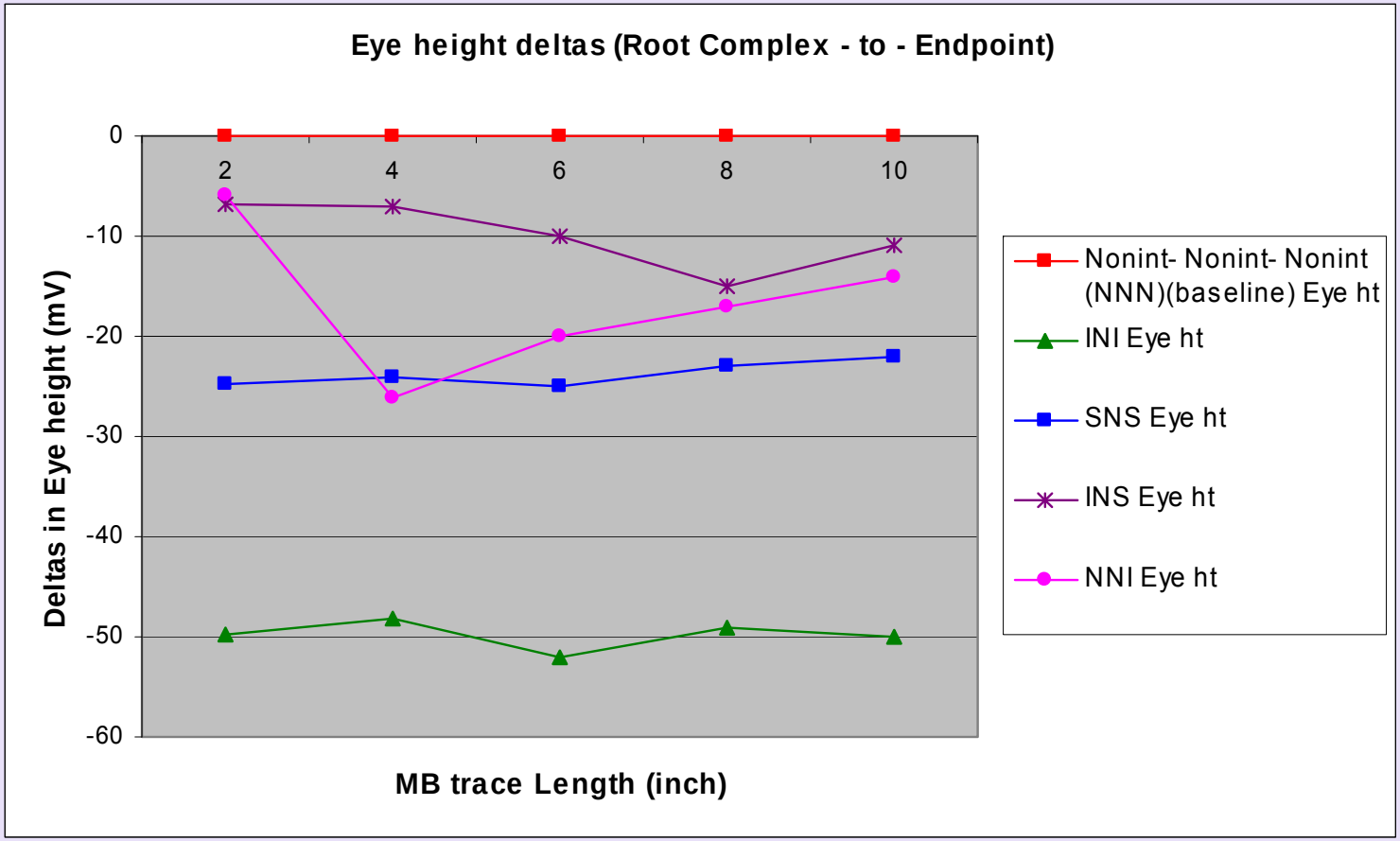


Example Root Complex: CPU/Chipset

Example Endpoint: Discrete GFX device

Impact on Eye Height

- Root Complex driving: Interleave - Non interleave (Motherboard)- Interleave (end point pkg) results in the least eye height
- Non interleave - Non interleave (MB)- Non Interleave (end point pkg) results in the most eye height



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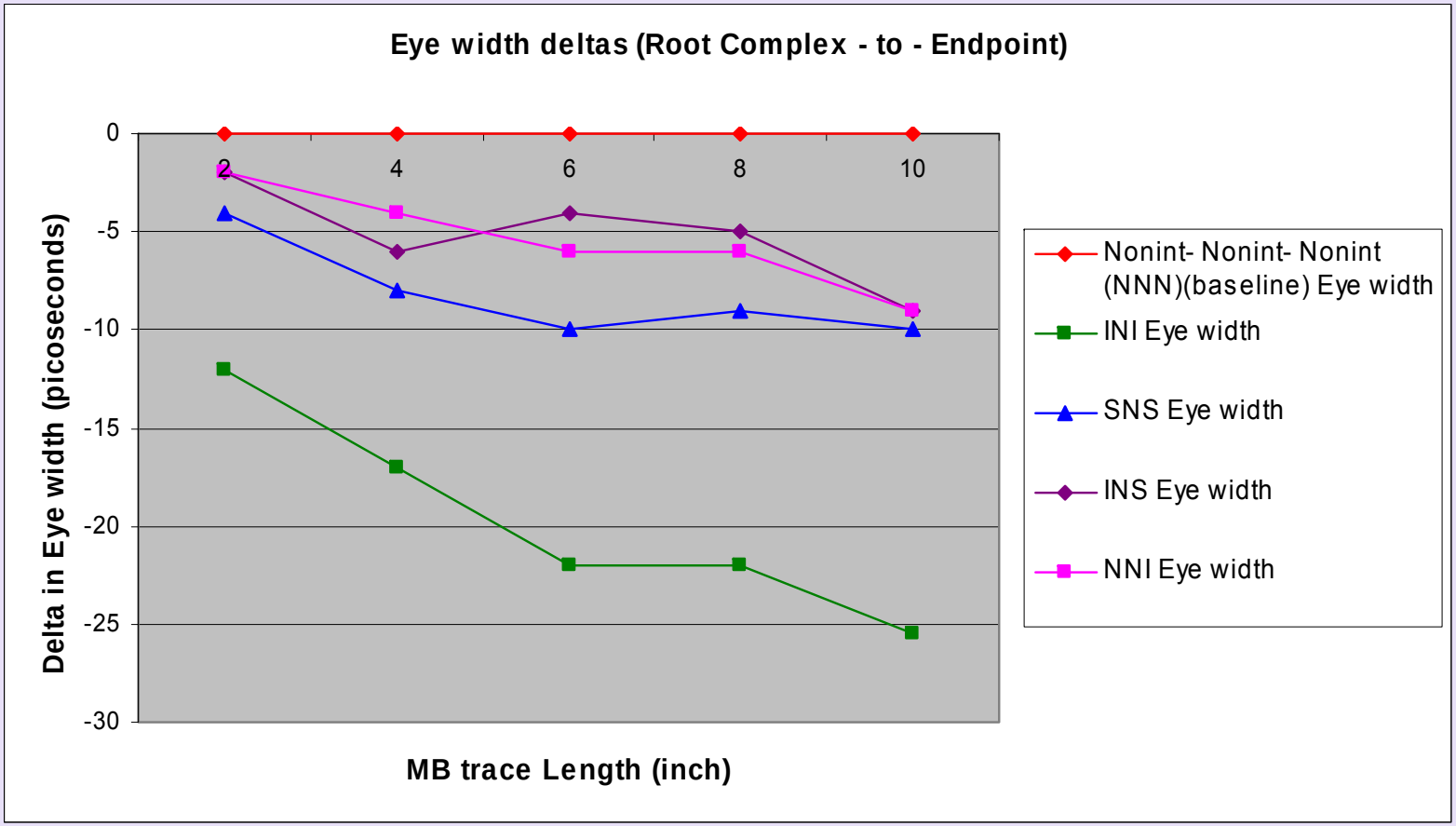
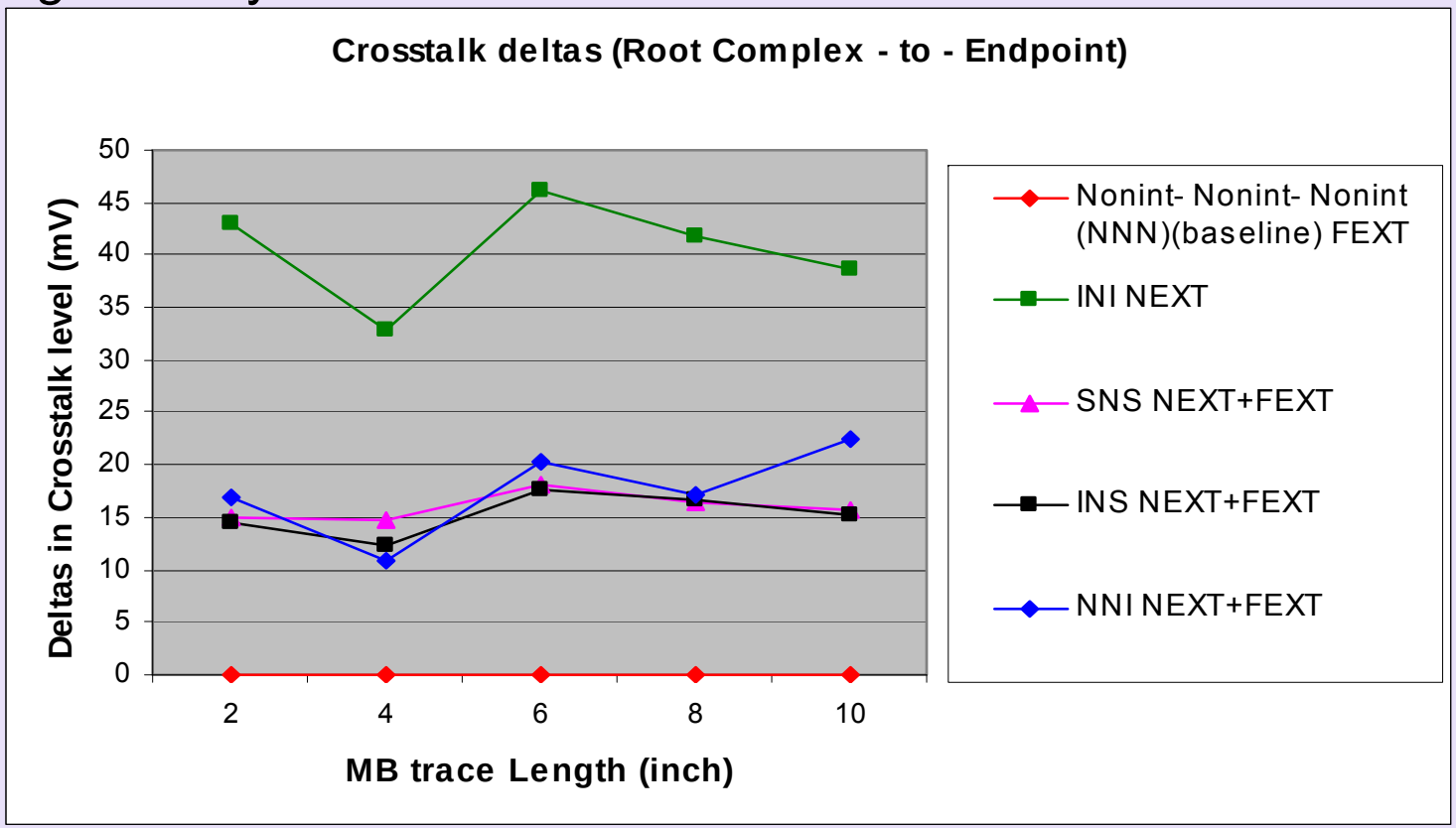
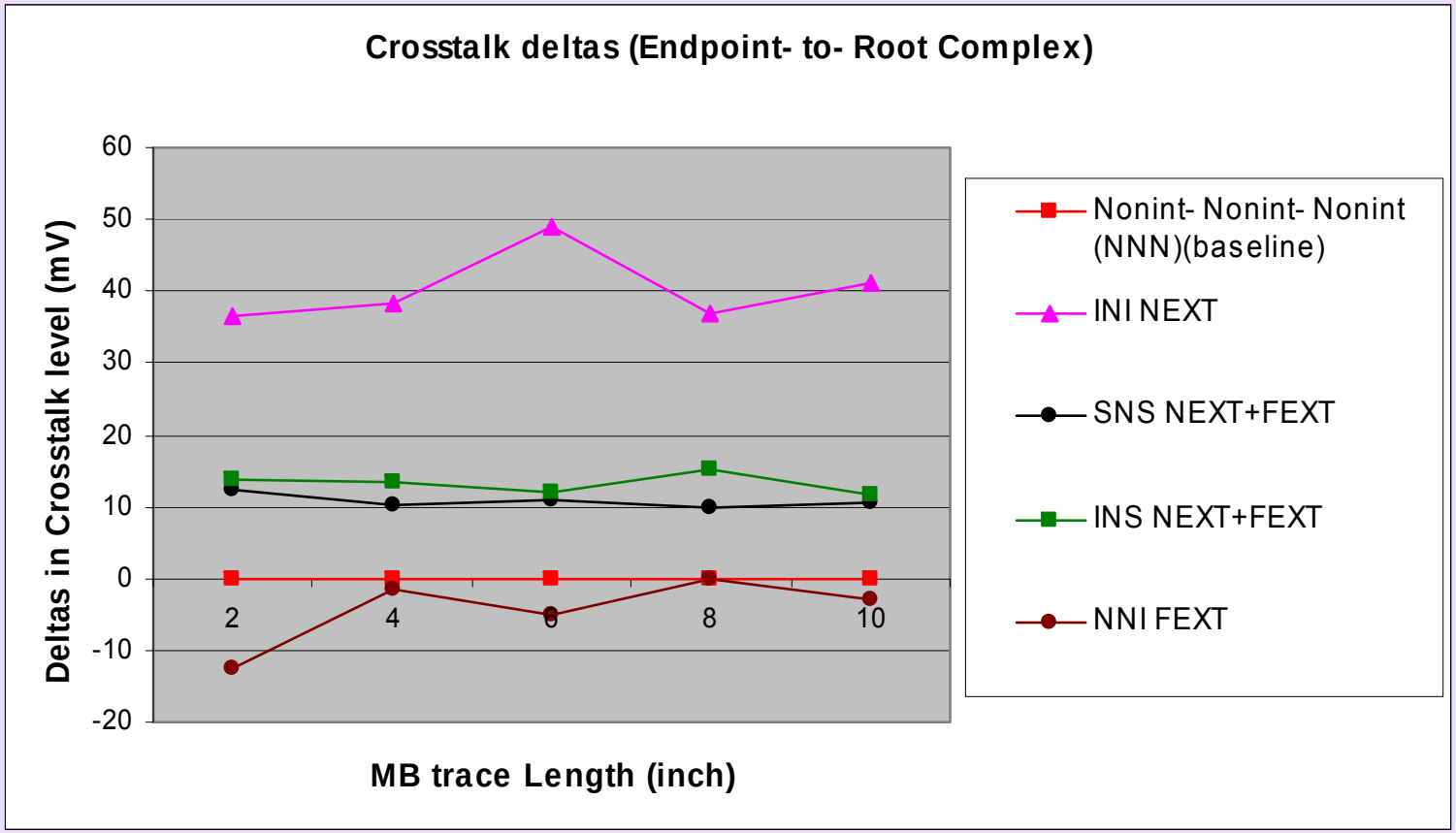


Crosstalk Results – Root Complex Driving

- Interleaving on both packages (I-N-I configuration) results in maximum crosstalk- dominated by near end crosstalk (NEXT)
- Implementing all non-interleaved routing can reduce the crosstalk significantly



Crosstalk Results – End Point Driving



- Impact on crosstalk due to interleaving on both packages is quite significant

Summary for Package Routing Combinations

- Non-interleaving on both packages produces the best results
- Interleaving on both packages is not advisable due to increased NEXT
- Interleaving or semi-interleaving on one of the packages (root complex or end point) does not have a large negative impact
- Non-interleaved routing is a good option due to availability of multiple routing layers in mobile layouts

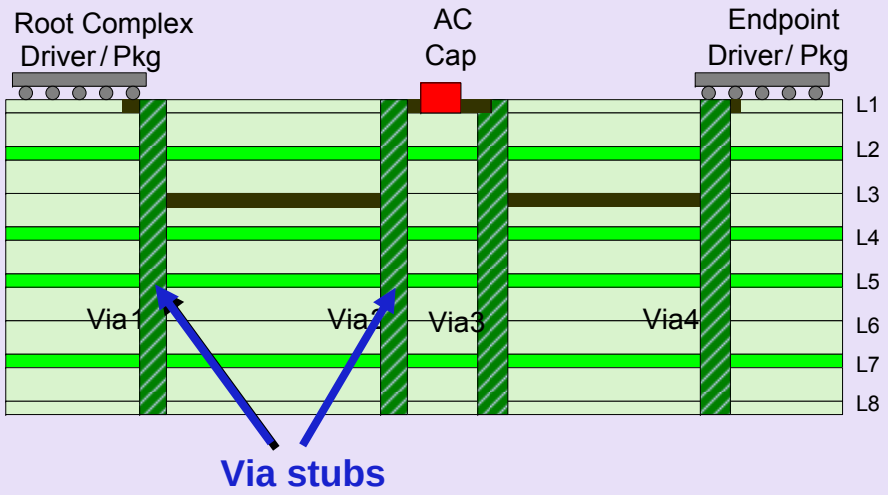
Layer Transition Optimizations

Layer Transition Optimization

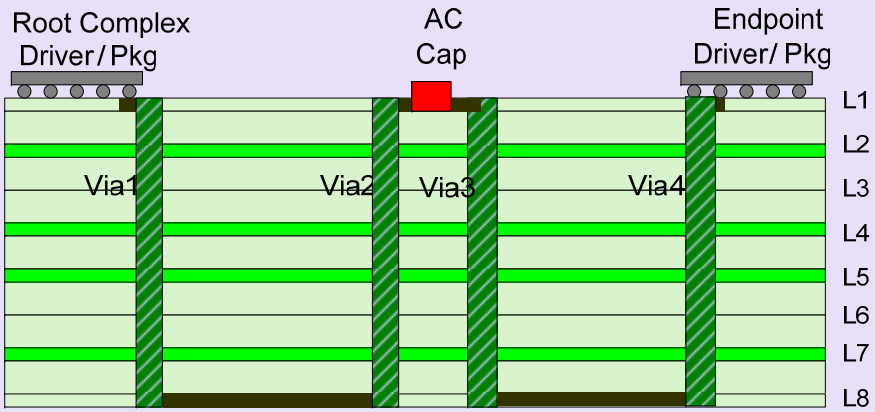
- On a mobile platform, designers should carefully consider the routing layers they select for high speed signals such as PCI Express 2.0
- Via stub affects can have a significant impact on eye height and eye width
- The case study example run at 5GT/s looks at an 8-layer motherboard with all routing on:
  - ✓ Layer 1
  - ✓ Layer 3
  - ✓ Layer 6
  - ✓ Layer 8
- The study looks at 10” motherboard routing
  - ✓ Also looked at 2” motherboard case and saw similar results

Case Study Topology

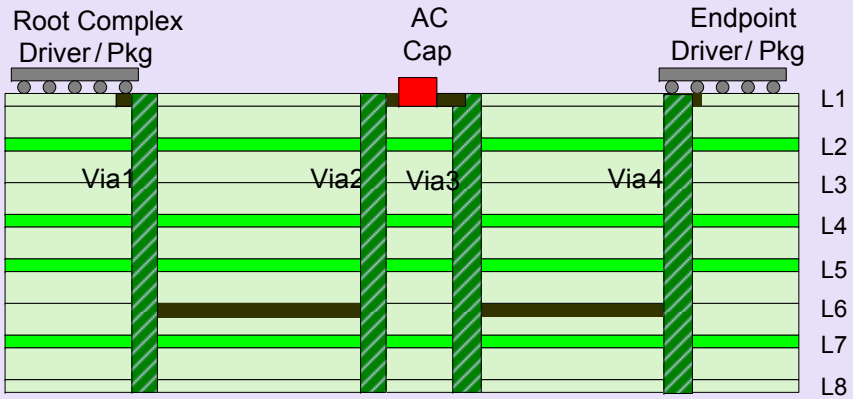
Layer 3 Routing (1to3 Via)



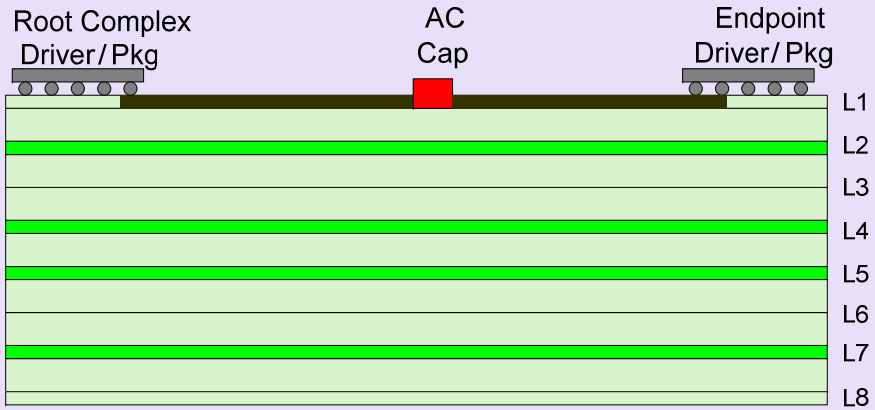
Layer 8 Routing (1to8 Via)



Layer 6 Routing (1to6 Via)



Layer 1 Routing (No Vias)



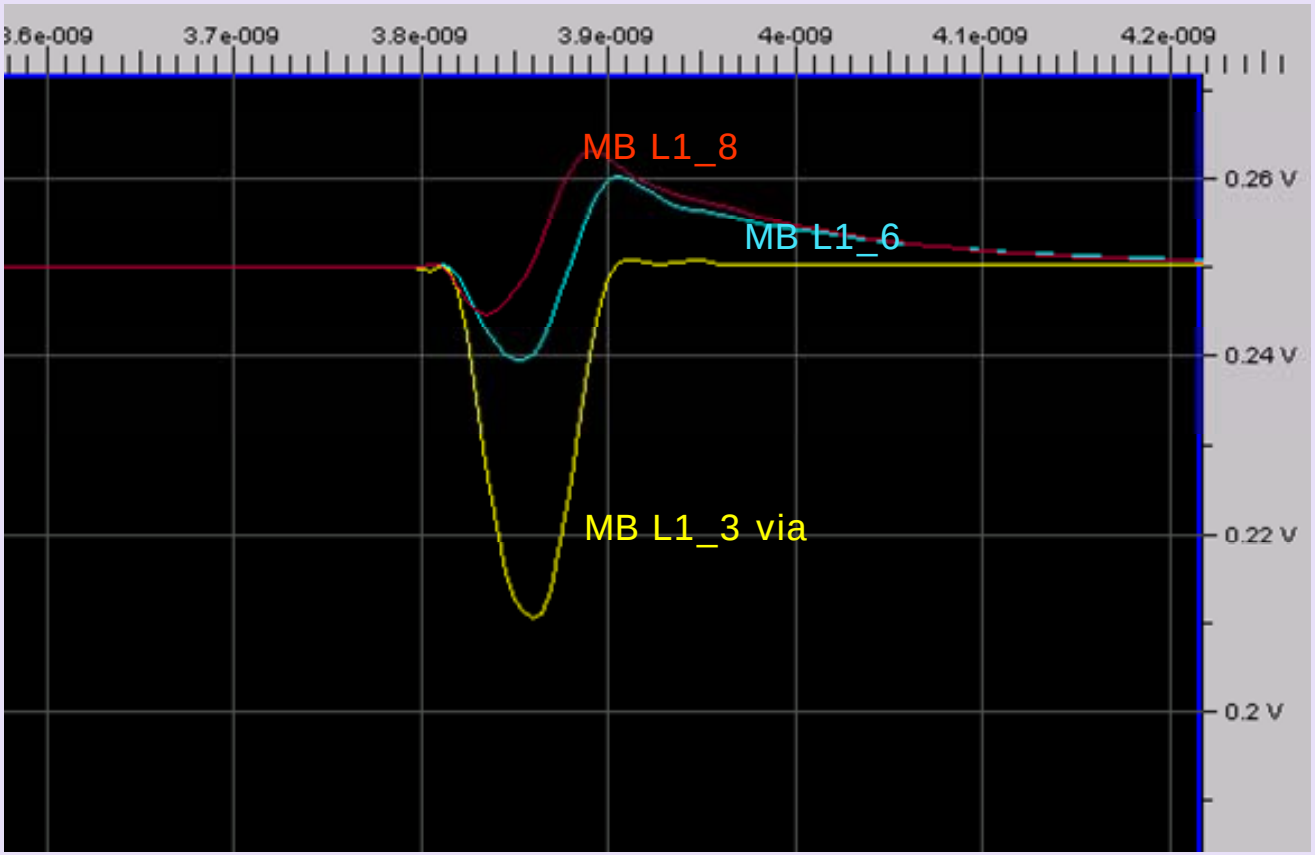
Impact on Eye Height and Width

- Transitioning from layer1 to layer3 results in worst case eye height
- For this case, the via stub has little impact on eye width margins
- If doing stripline routing, designers should consider using the far routing layer (Layer 6 in example). This reduces the resonance effects of the via stub
- Removing all vias improves eye height and eye width margins
  - ✓ However, microstrip routing can have other negative design impacts, such as EMI and limited routing space due to dense component placement on PCB top/bottom layers.

	All SL routing; 1to3 Vias	All SL routing; 1to6 Vias	All MS routing; 1to8 Vias	All MS routing; No vias
Eye Height (mV)	Baseline	+ 3	+ 17	+ 32
Eye Width (ps)	Baseline	+ 1	- 3	+ 6

Capacitive Effect of 1to3 Via

- Looking at via model in the time domain into a test load, the capacitive affects of the Layer1-to-Layer3 via can be seen



Overall Summary

- On a mobile platform, there are many optimizations that can be made to improve signal integrity and routability for PCI Express 2.0
  - ✓ Lower differential impedance on the package and motherboard to 85 Ohms
  - ✓ Use all non-interleaved routing
  - ✓ Consider reducing layer transitions; Using optimal layers for routing
- At higher data rates (5GT/s), these optimizations can no longer be considered insignificant and should be implemented where possible

Thank you for attending the PCI-SIG Developers Conference Europe 2007.

For more information please go to www.pcisig.com

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