



PCI Express® Future

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Disclaimer

The information in this presentation refers specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG workgroups, but all material is subject to change before the specifications are released.

Increased Speed

PCIe Speed Evolution

- Introduced at 2.5GT/sec
 - ✓ Commonly called 2.5GHz
 - PCI-SIG eventually adopts GigaTransfers per Second (GT/s) terminology
 - ✓ 100 MHz reference clock provided
 - Eases synchronization between ends
 - Particularly when Spread Spectrum Clocking is used
 - Optional, but nearly universal in traditional “PC” world
 - ✓ 8b/10b encoding used to provide DC balance and reduce “runs” of 0s or 1s which make clock recovery difficult
- Specification Revisions: 1.0, 1.0a, 1.1

PCIe Speed Evolution (cont'd)

- Speed doubled to 5GT/sec
 - ✓ Reference clock remains at 100 MHz
 - Lower jitter clock sources required vs 2.5GT/sec
 - Generally higher quality clock generation/distribution required
 - ✓ 8b/10b encoding continues to be used
- Specification Revisions: 2.0, 2.1
 - ✓ Devices choosing to implement a maximum rate of 2.5GT/sec can still be fully 2.x compliant!

PCIe Speed Evolution (cont'd)

2 x 5 = ?

PCIe Speed Evolution (cont'd)

$$2 \times 5 = 8 \text{ ???}$$

- Speed “doubled” over PCIe 2.x 5GT/sec
- 8GT/sec electrical rate
- Reference clock remains at 100 MHz
 - Very similar requirements to 5GT/sec mode
- Specification Revisions: 3.0
 - ✓ Devices choosing to implement a maximum rate of 2.5GT/sec or 5GT/sec can still be fully 3.0 compliant!

PCIe Speed Evolution (cont'd)

- 128/130 encoding reduces overhead from the 20% loss of 8b/10b
 - ✓ Original plan was scrambling-only for exactly 2x the 5GT/sec bandwidth
 - $5000\text{Mb/sec} / (10\text{bits/byte}) = 500\text{MB/sec per lane}$
 - $8000\text{Mb/sec} / (8\text{bits/byte}) = 1000\text{MB/sec per lane}$
 - ✓ Pure 128/130 encoding is ~1.5% loss
- Scrambling replaces DC-offset and run-length reduction functions of 8b/10b

PCIe Speed Evolution (4.0 Plan of Record)

2 x 8 = ?

PCIe Speed Evolution (4.0 Plan of Record)

$$2 \times 8 = 16$$

- 16GT/sec electrical rate
- Reference clock remains at 100 MHz
 - ✓ New option for independently clocked Spread Spectrum mode
- Retains “3.0” enhancements
 - ✓ 128/130 encoding
 - ✓ Link equalization
- Devices with a max rate of 2.5GT/sec, 5GT/sec, or 8GT/sec can still be fully 4.0 compliant!

PCIe Speed Evolution (4.0 Plan of Record)

- When?
 - ✓ Spec complete in 2013-2014?
- Where is the work being done?
 - ✓ PCI-SIG Electrical Workgroup (EWG)
<http://www.pcisig.com/apps/org/workgroup/pciexpress/electrical/>
 - ✓ PCI-SIG Protocol Workgroup (PWG)
<http://www.pcisig.com/apps/org/workgroup/pciexpress/protocol/>
- Where to find out more?
 - ✓ Watch for Review Drafts to all-members e-mail
 - ✓ Watch PCI-SIG Review Zone
http://www.pcisig.com/specifications/pciexpress/review_zone

Independent Reference Clocks with Spread Spectrum

Independent Reference Clocks with Spread Spectrum

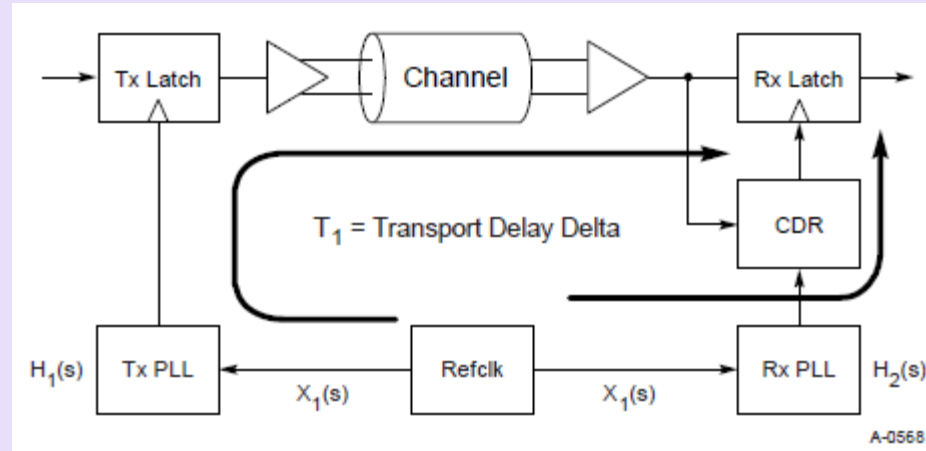
- Base Specification Defines Independent Clocking Mode today
 - ✓ RefClk not used between upstream and downstream components
 - ✓ Explicitly forbids Spread Spectrum Clocking (SSC)
- Cabled environments need SSC, want to NOT carry RefClk
 - ✓ PCI-SIG Small Footprint Cable
 - ✓ Other cable specs

Independent Reference Clocks with Spread Spectrum

- Will require Base Specification changes
 - ✓ Larger elasticity buffer
 - ✓ More frequent insertion of SKIP ordered set
 - ✓ Non-trivial receiver changes in Clock Data Recovery (CDR) logic
- Current proposal is ECN to 3.0
 - ✓ Member preference for ECN or new revision?
 - ✓ Review and respond to review draft(s) when they are published to general membership!

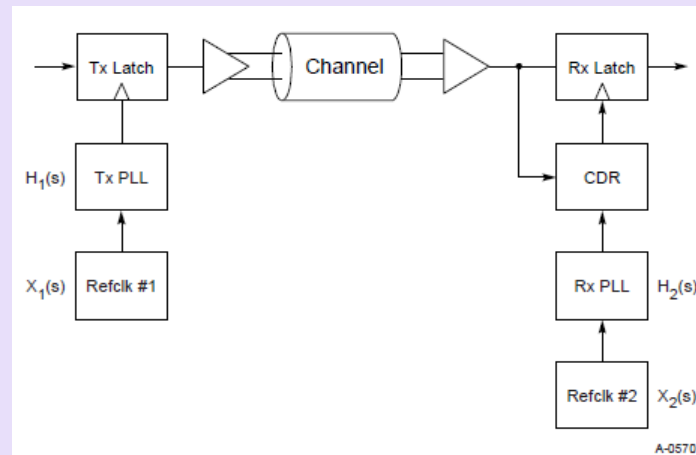
Independent Reference Clocks with Spread Spectrum

- Today's Common Clock mode



- Independent RefClk mode

✓ Today: No SSC



Independent Reference Clocks with Spread Spectrum

- When?
 - ✓ Proposed ECN being discussed now
 - ✓ Could be ready Q3 '12
- Where is the work being done?
 - ✓ PCI-SIG Electrical Workgroup (EWG)
<http://www.pcisig.com/apps/org/workgroup/pciexpress/electrical/>
 - ✓ PCI-SIG Protocol Workgroup (PWG)
<http://www.pcisig.com/apps/org/workgroup/pciexpress/protocol/>
- Where to find out more?
 - ✓ Watch for ECR Review to all-members e-mail
 - ✓ Watch PCI-SIG Review Zone
http://www.pcisig.com/specifications/pciexpress/review_zone

Link State Power Enhancements

Link State Power Enhancements

- Add new “sub-states” of L1 to provide more power savings
 - ✓ Allow port to turn off its PLL and receiver/transmitter circuitry
 - ✓ Goal is to hit μW of power per lane vs mW today
- Use CLKREQ# pin bidirectionally to enter/exit new lower power L1 sub-states
 - ✓ Pin exists in miniPCle form-factors
 - ✓ Could repurpose a reserved pin on CEM form-factor
- Use requires LTSSM changes
- PHY design changes to leverage power savings

Link State Power Enhancements

- When?
 - ✓ Proposed ECN being discussed now
 - ✓ Could be ready Q2 '12
- Where is the work being done?
 - ✓ PCI-SIG Protocol Workgroup (PWG)
<http://www.pcisig.com/apps/org/workgroup/pciexpress/protocol/>
- Where to find out more?
 - ✓ Watch for ECR Review to all-members e-mail
 - ✓ Watch PCI-SIG Review Zone
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Low Power Signaling

Low Power Signaling

- Teaser: Nothing formal to date
- Much interest in dramatically lower power per lane
 - Mobile and tablet form-factors?
 - Ultra-thin laptops?
- Opportunities for many development directions
 - Refined PCIe PHY(s)?
 - All-new PHY?
 - What is optimum signaling rate?

Small Footprint Cabling

Small Footprint Cabling

- New workgroup formed Q4'11
- Goal to develop smaller footprint cabling than existing PCIe Cable
 - ✓ Internal version
 - ✓ External version
 - ✓ Lower cost
- Desire to eliminate RefClk from cable
 - ✓ Would require adoption of Independent Reference Clocks with Spread Spectrum mode

Small Footprint Cabling

- When?
 - ✓ 0.3 Revision to members in late April 2012
 - http://www.pcisig.com/apps/org/workgroup/wg_members/document.php?document_id=8399
- Where is the work being done?
 - ✓ PCI-SIG New Cable Workgroup
 - <http://www.pcisig.com/apps/org/workgroup/cable/>
- Where to find out more?
 - ✓ Watch for Review Drafts to all-members e-mail
 - Respond with feedback!
 - ✓ Watch PCI-SIG Review Zone
 - http://www.pcisig.com/specifications/pciexpress/review_zone

PCIe Storage Connector

PCIe Storage Connector

- New workgroup formed in Q1 '12
- Partnership between PCI-SIG and SFF
- Leveraging work on SFF-8639 connector
- PCI-SIG electrical experts assisting with development and validation
- Goal is to support 8GT/s and future 16GT/s PCIe

Thank you for attending the
PCIe Technology Seminar

For more information please go to
www.pcisig.com