LTSSM Implementation at 5 GT/s and Beyond

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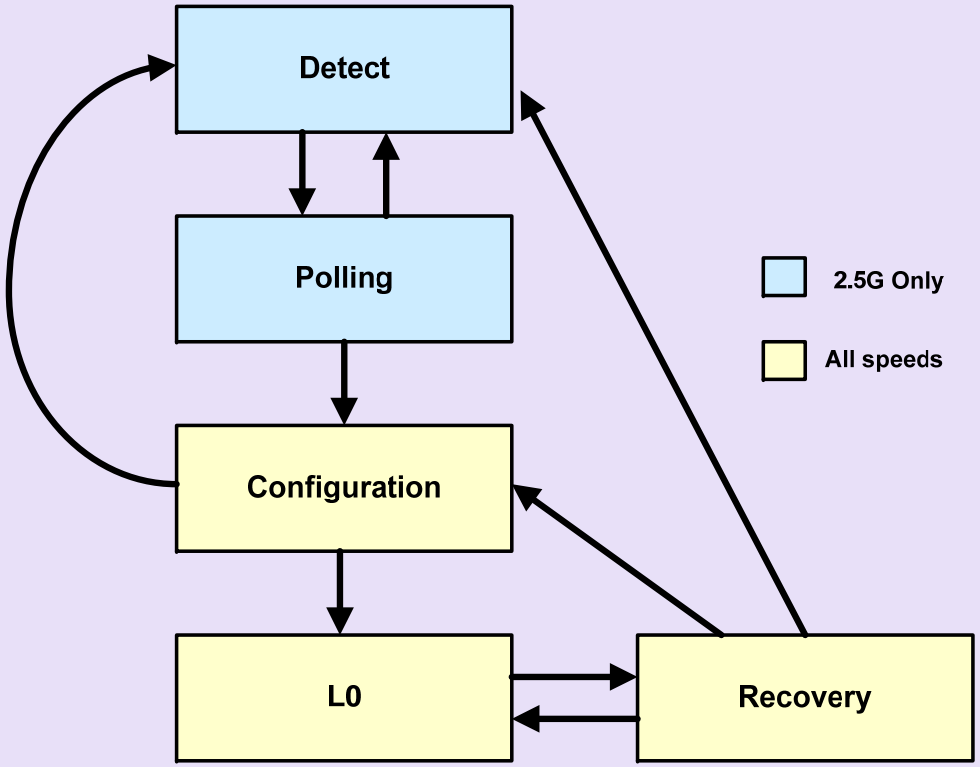
Agenda

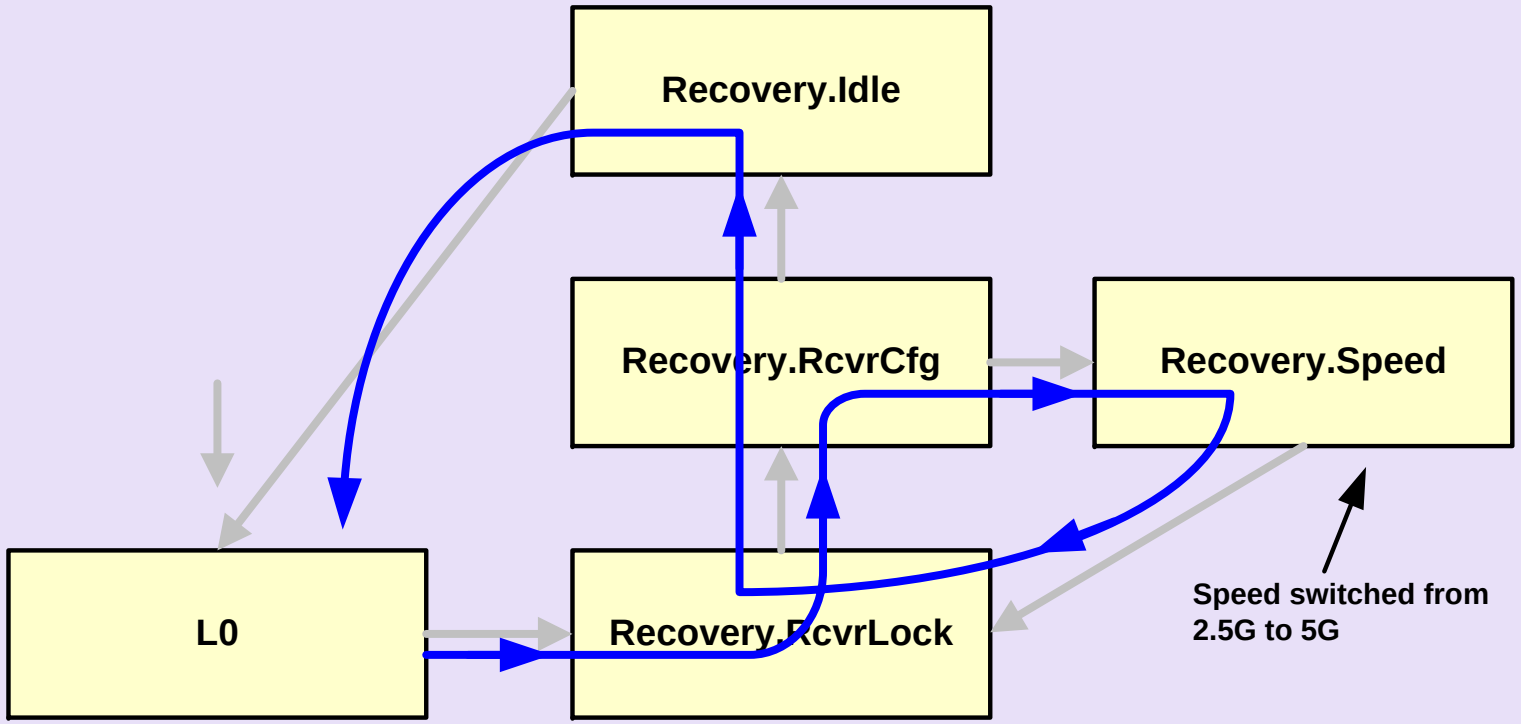
- Link Training Status State Machine (LTSSM) Overview
  - ✓ Speed negotiation overview
  - ✓ Negotiating lane speeds beyond 5 GT/s
- LTSSM Example Implementation
  - ✓ Implementation challenges
  - ✓ Modular LTSSM design
  - ✓ Results from FPGA implementation at 10 GT/s lane speed

LTSSM Overview



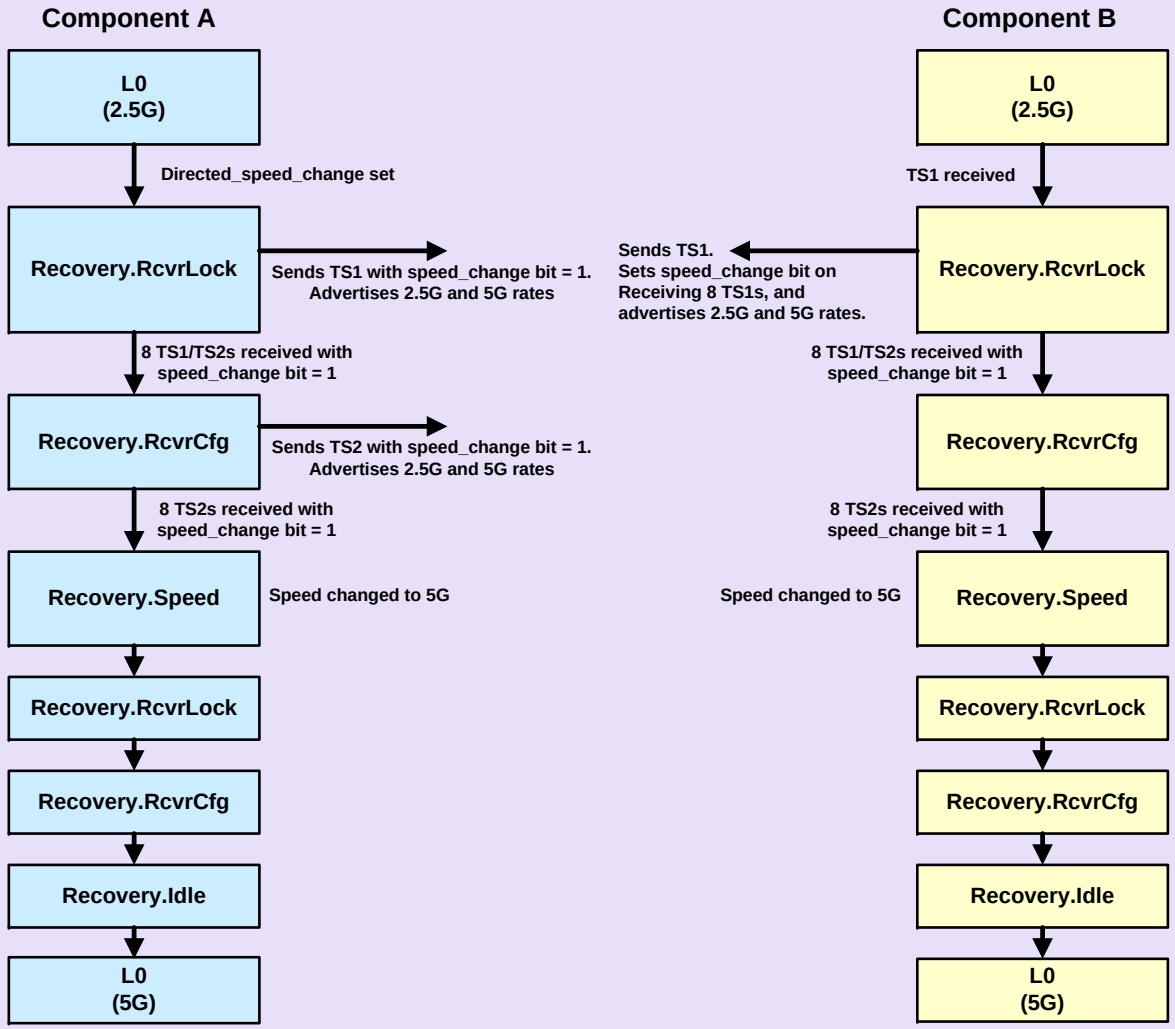
- States not shown: L0s, L1, L2, Loopback, Disabled, Hot Reset

LTSSM Speed Negotiation



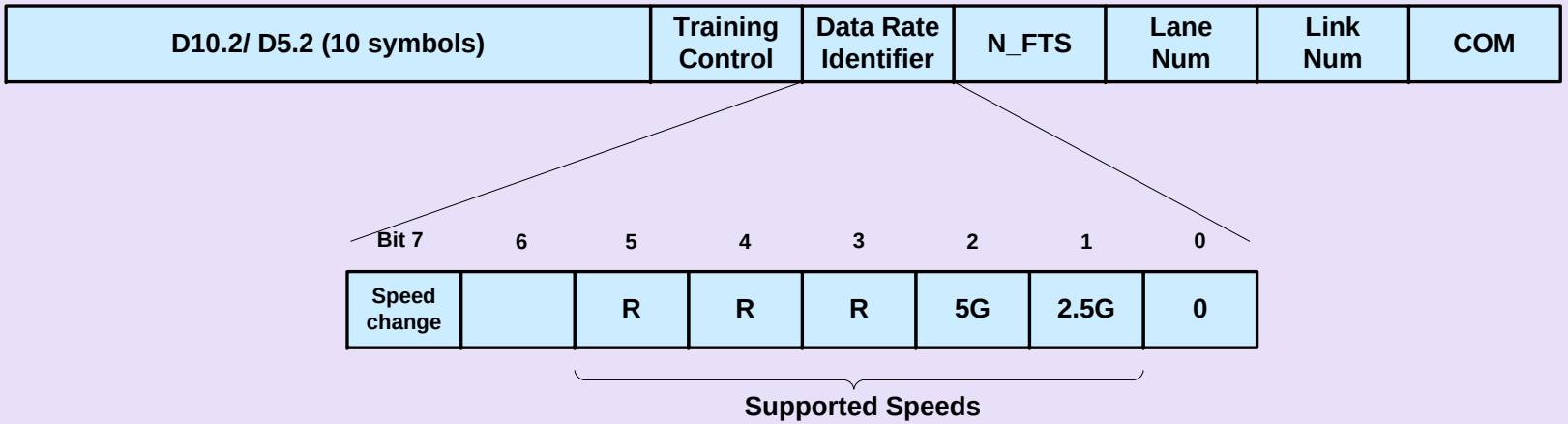
- Successful speed negotiation from 2.5G to 5G

Speed Negotiation From 2.5G to 5G



Speed Advertisement

- Supported speeds advertised in TS1/TS2 sequences

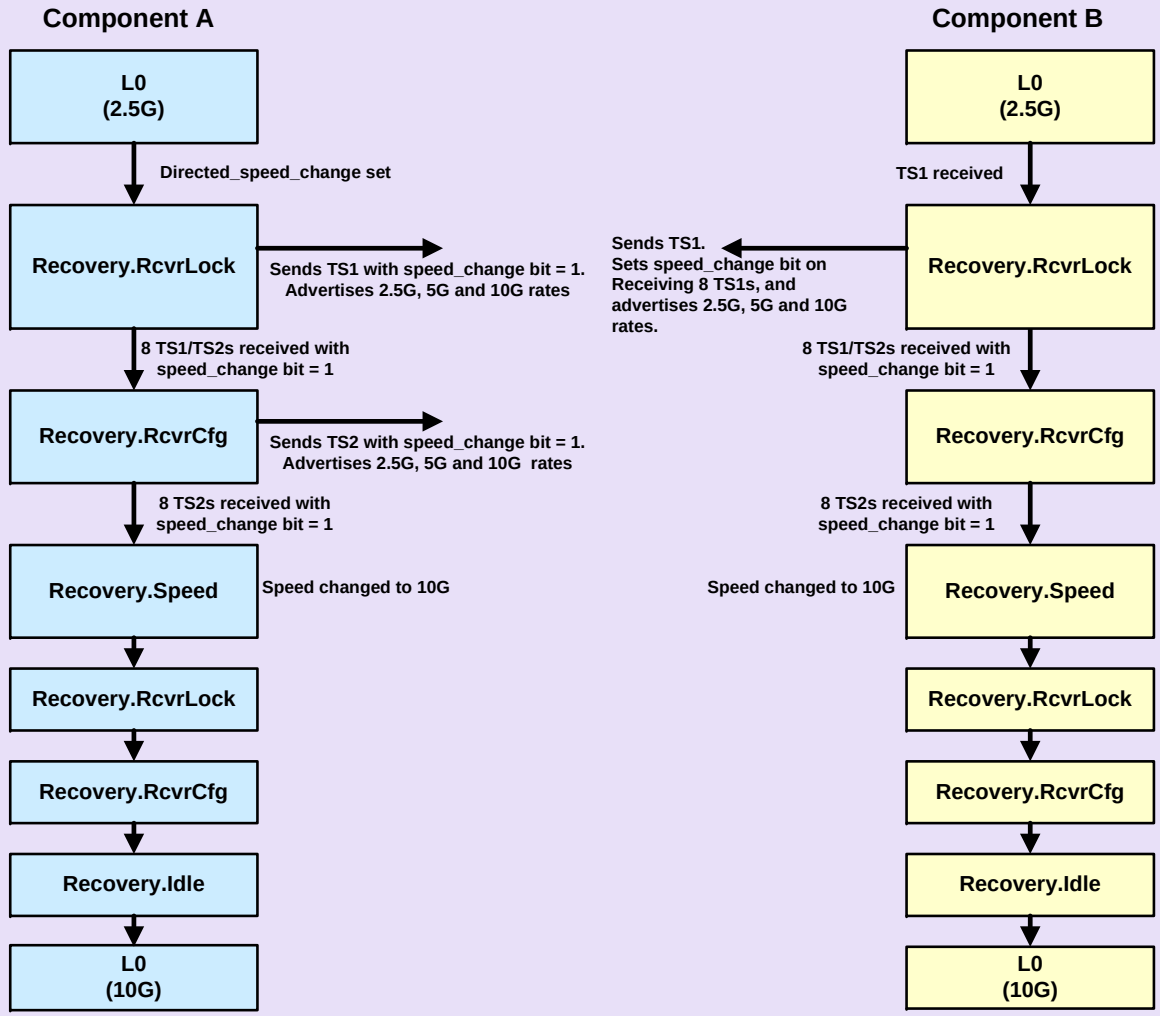


- Bit 3 used to advertise 10G capability in our implementation

Negotiating Speeds Beyond 5 GT/s

- PCIe® 2.0 defines lanes speeds of 2.5 and 5.0 GT/s
- Speed negotiation protocol may be extended for lane speeds beyond 5 GT/s
  - ✓ Example implementation allows 2.5, 5 and 10 GT/s lane speeds.
  - ✓ Demonstrates:
    1) Scaling of speed negotiation protocol beyond 5 GT/s
    2) Feasibility of implementing LTSSM in relatively low-speed logic

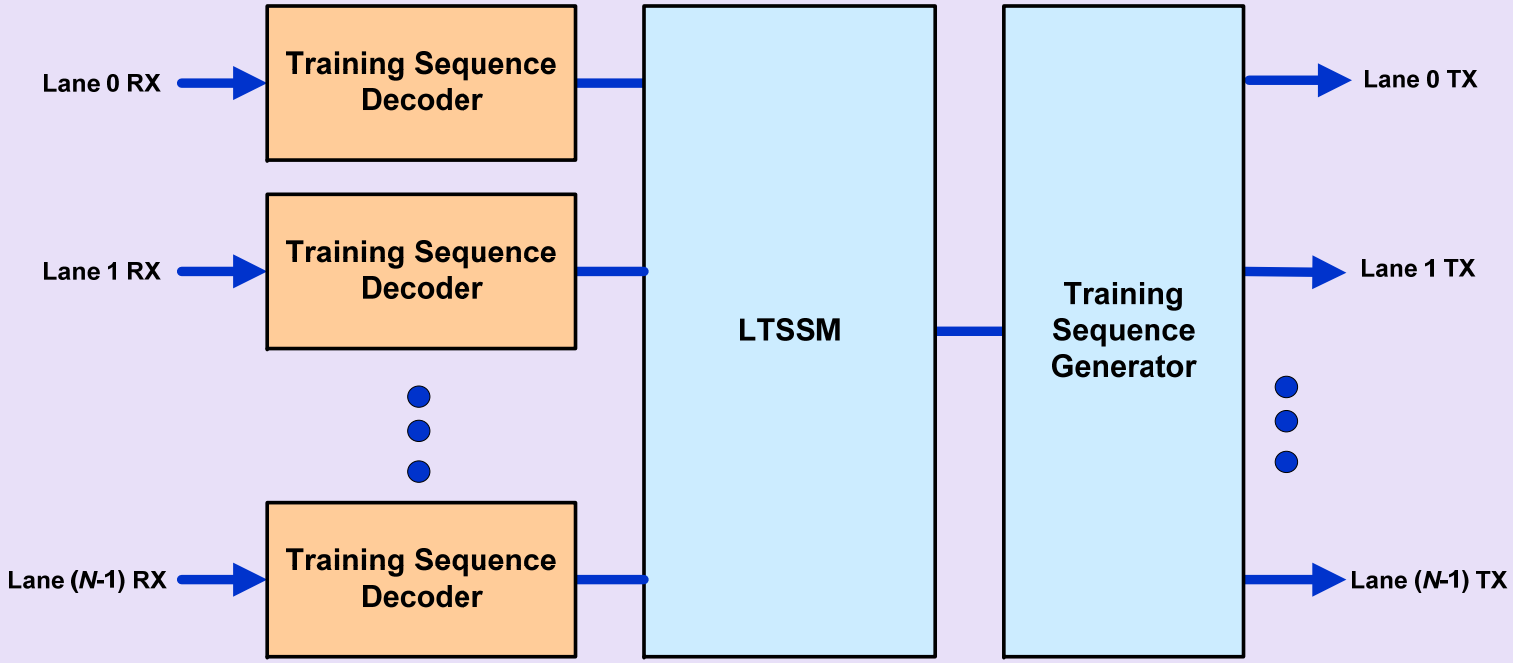
Speed Negotiation From 2.5G to 10G



LTSSM Implementation

- Specification facilitates modular implementation
  - ✓ All lanes transmit same TS data, except link and lane number fields
    - Single transmit-side module for all lanes
  - ✓ Separate receive-side module per lane
- Challenges
  - ✓ Lane skew on receive side
  - ✓ Phy errors on receive side
  - ✓ Transmitting compliance pattern

LTSSM Example Implementation

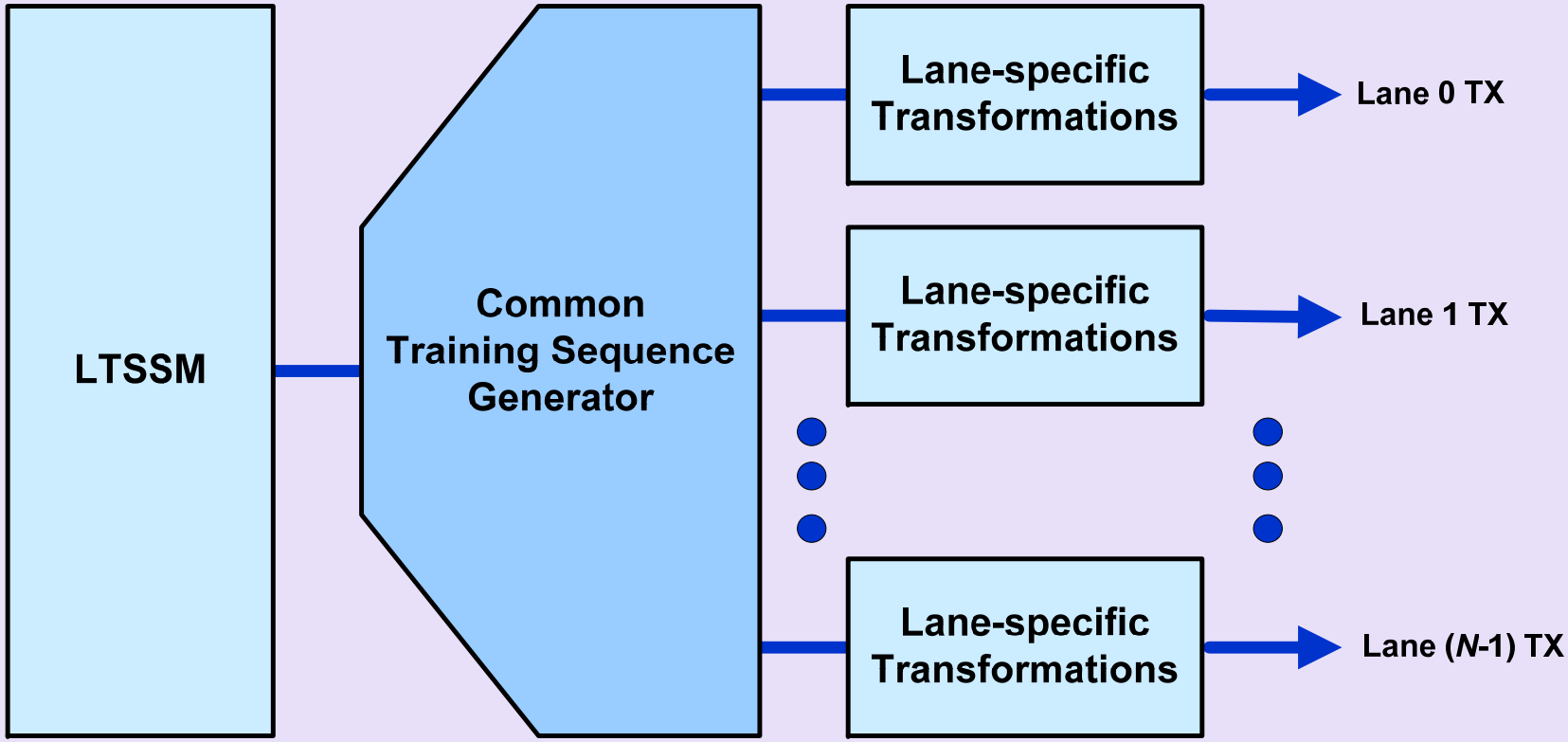


Transmitting Training Sequences

D10.2/ D5.2 (10 symbols)	Training Control	Data Rate Identifier	N_FTS	Lane Num	Link Num	COM

- Transmit side primarily transmits TS1/TS2 on all configured lanes
  - ✓ Some field settings are a function of LTSSM state
    - TS1/TS2, link number, lane number
  - ✓ Most fields can be changed on all lanes simultaneously
- Data path can be from 1 byte to 16 bytes per lane
- Single data path can feed all lanes

LTSSM Transmit-Side Implementation



LTSSM Receive-Side Implementation

- Independent receive-side modules needed to decode Training Sequences
  - ✓ Skew may cause outputs to be misaligned
  - ✓ Phy errors may disqualify output
- Decoding may be done in parallel
  - ✓ Data path can be from 1 byte to 16 bytes

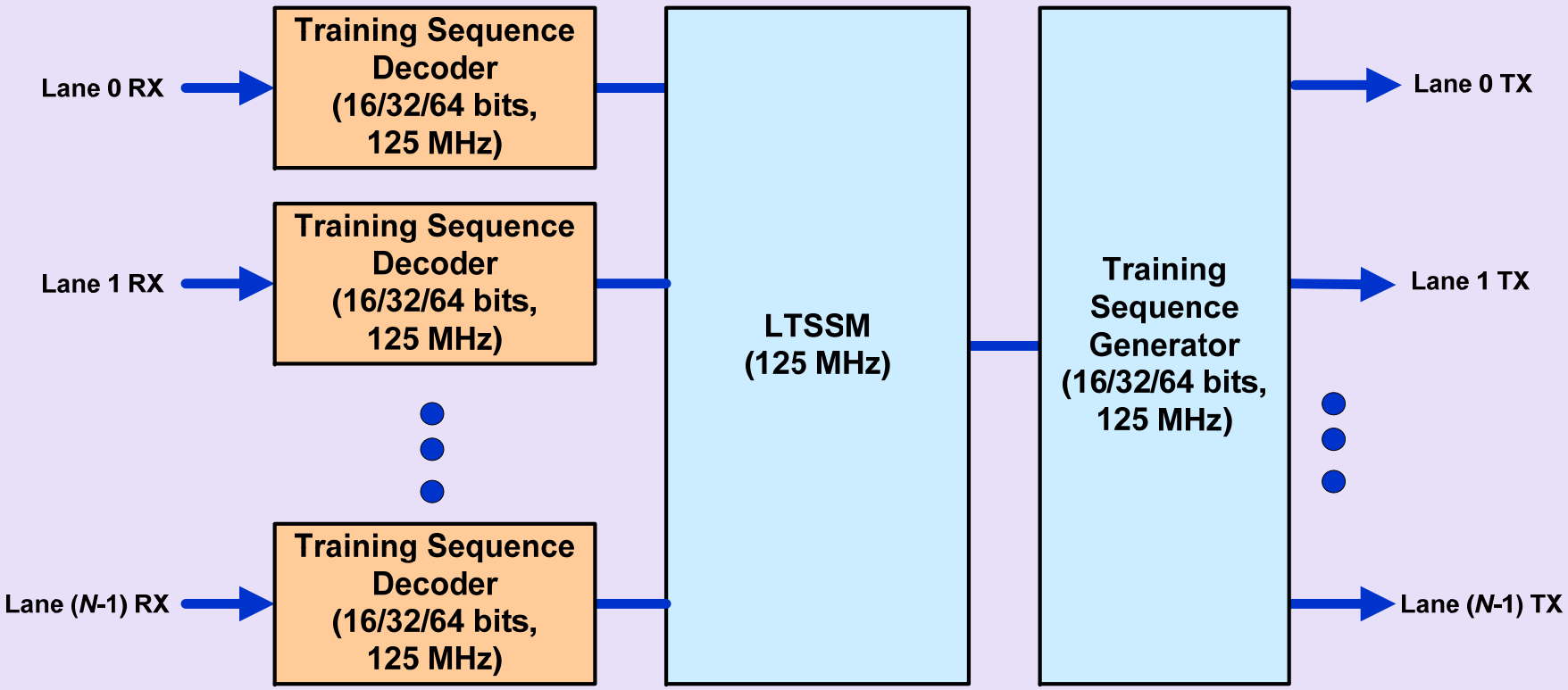
LTSSM Receive-Side Example Implementation

- Consists of *N* instances of same Training Sequence Decoder module
  - ✓ Module decodes TS1/TS2, extracts fields
  - ✓ Implements building blocks for generating LTSSM inputs
    - Example: 8 TS1s received with link number and lane number = PAD
  - ✓ Enables same LTSSM design to be used at different lane speeds

LTSSM Example Implementation

- Implemented RC and EP sides of LTSSM
  - ✓ Max lane speed of 10 GT/s, and up to 10 lanes
  - ✓ 125 MHz clock
- Consists of
  - ✓ Main LTSSM module
  - ✓ Training Sequence Generator Module with configurable data path width
  - ✓ Training Sequence Decoder Modules (1 per lane) with configurable data path width

LTSSM Example Implementation



Summary

- The PCIe LTSSM Specification, despite its complexity, enables a scalable and modular implementation.
  - ✓ Design can be partitioned into 3 key blocks
    - Main LTSSM module, independent of lane speed
    - Common transmit-side module with configurable data path width
    - Per-lane receive-side modules with configurable data path width
- Example implementation demonstrates feasibility at lane speeds higher than 5 GT/s

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