PCIe® 3.0: 8.0 GT/s Digital Retimer

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Rationale

- As data rates increase the need for good signal conditioning increases
- Two methods of active signal conditioning are considered
  - ✓ Analog Repeater
  - ✓ Digital Retimer

Agenda

- Review of PCIe® 1.x & 2.x
- Review of PCIe 3.0
- PCIe 3.0 Repeater
- PCIe 3.0 Retimer

PCIe 1.x & 2.x

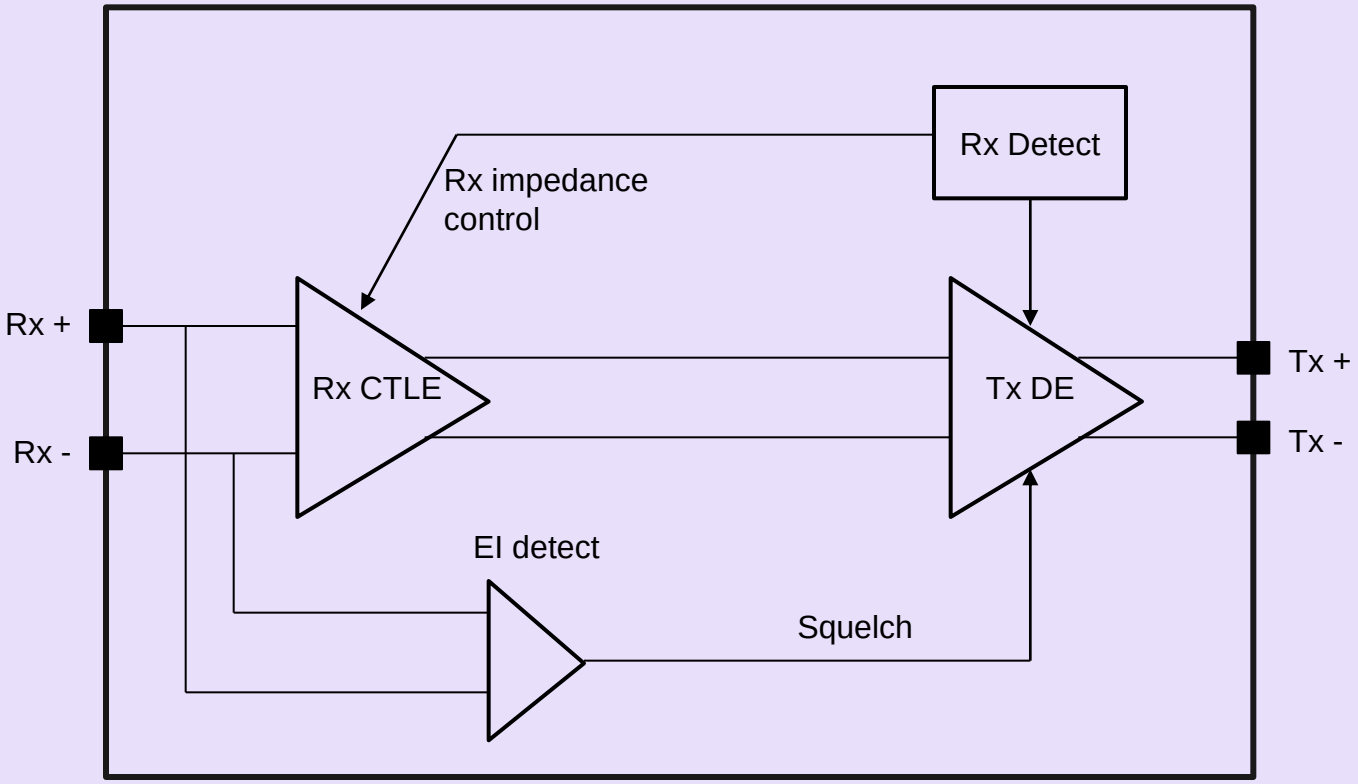
PCIe 1.x/2.x Requirements

- 2.5/5.0 GT/s
- 8b10b coding
- Tx (Selectable) de-emphasis
  - ✓ -3.5 db 2.5 GT/s
  - ✓ -3.5/-6 db 5.0 GT/s
- Rx
  - ✓ Continuous Time Linear Equalizer (CTLE)
  - ✓ No adaptive Rx equalization
- EI detect
- Rx detect

PCIe 1.x/2.x Repeater (Typical)

- Analog only data path
  - ✓ Low latency
  - ✓ Not protocol aware
- No Clock and data recovery (CDR)
  - ✓ Removes some data dependant jitter (DDJ)
  - ✓ Does not remove random jitter (RJ)
- Rx
  - ✓ Continuous Time Linear Equalizer (CTLE)
  - ✓ Pin strap/EEPROM programmable boost, DC Gain, etc
  - ✓ EI detect circuit
- Tx FIR
  - ✓ de-emphasis only
  - ✓ Pin strap/EEPROM Programmable de-emphasis of -3.5 db to -6 db
  - ✓ Fixed delay (no recovered clock) at 200ps for de-emphasis
  - ✓ Rx detect circuit
  - ✓ Squelch on EI detect

Repeater Block Diagram

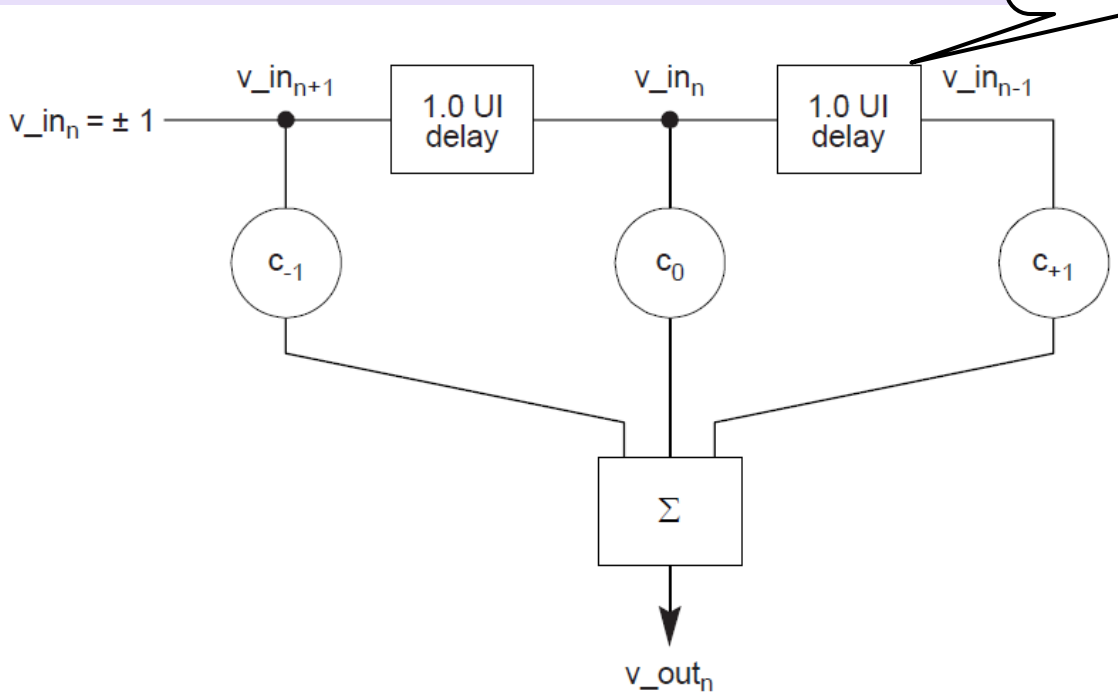


PCIe 3.0

PCIe 3.0 Requirements

- 8.0 GT/s
- Data scrambling + 2 bits of framing
  - ✓ 128B130B
- Tx
  - ✓ 10 presets OR coefficient matrix
  - ✓ Preshoot and de-emphasis
- Rx
  - ✓ CTLE
  - ✓ DFE
- EQ procedure

PCIe 3.0; Tx FIR



$$v\_out_n = (v\_in_{n+1} * c_{-1}) + (v\_in_n * c_0) + (v\_in_{n-1} * c_{+1})$$

$$|c_{-1}| + |c_0| + |c_{+1}| = 1 \qquad c_{+1} \le 0 \qquad c_{-1} \le 0$$

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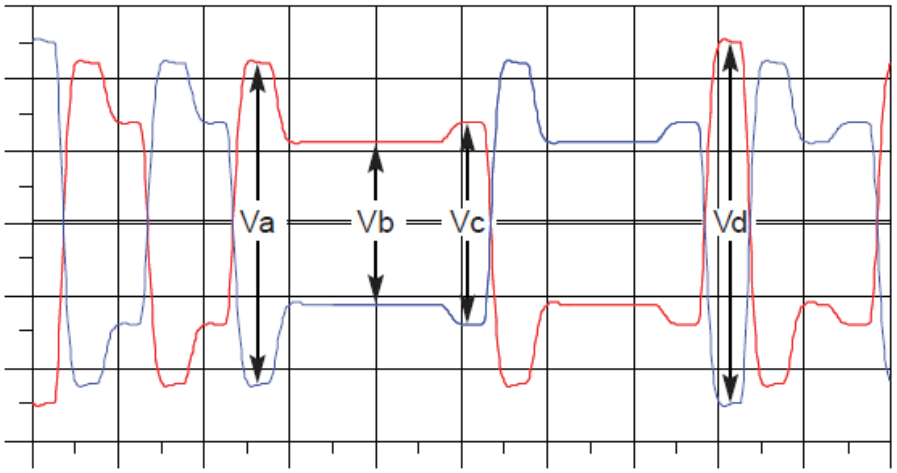
Figure 4-41: Tx Equalization FIR Representation

PCIe 3.0; Tx FIR



De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb

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Figure 4-42: Definition of Tx Voltage Levels and Equalization Ratios

PCIe 3.0; Coefficient Matrix

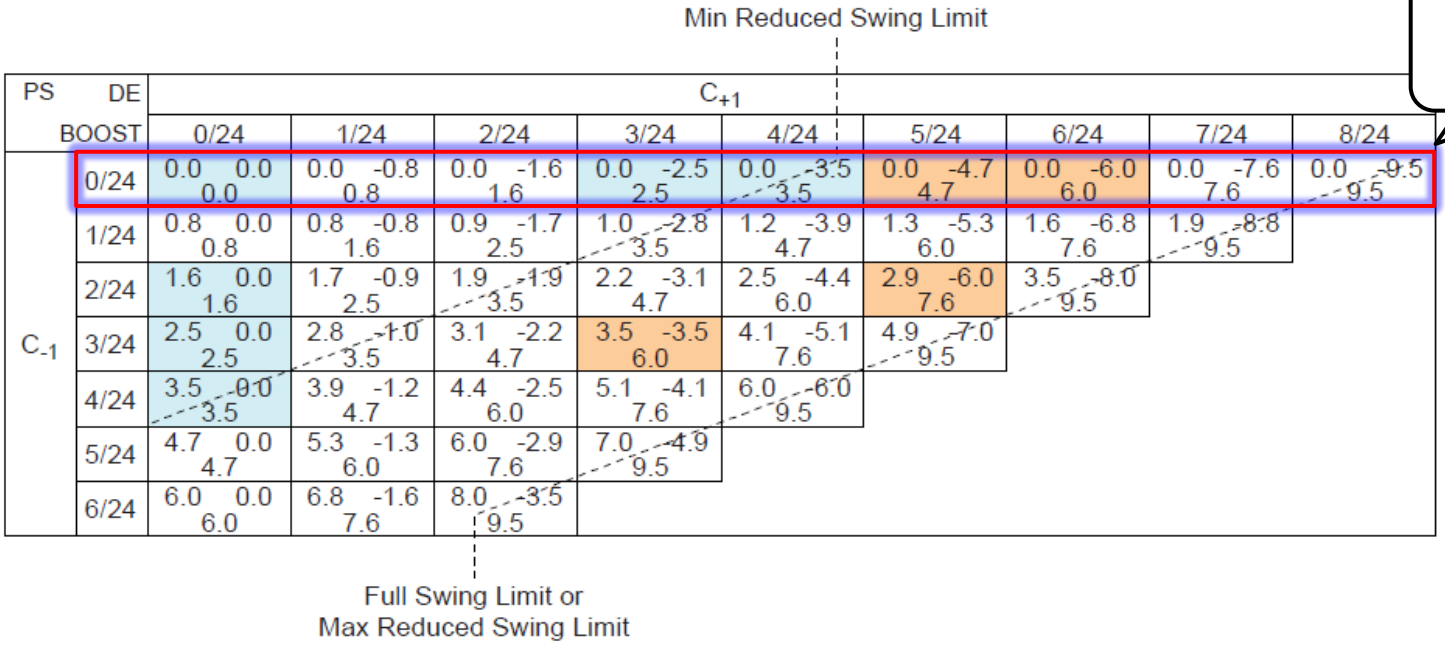


Figure 4-45: TxEQ Coefficient Space Triangular Matrix Example

PCIe 3.0; Rx CTLE

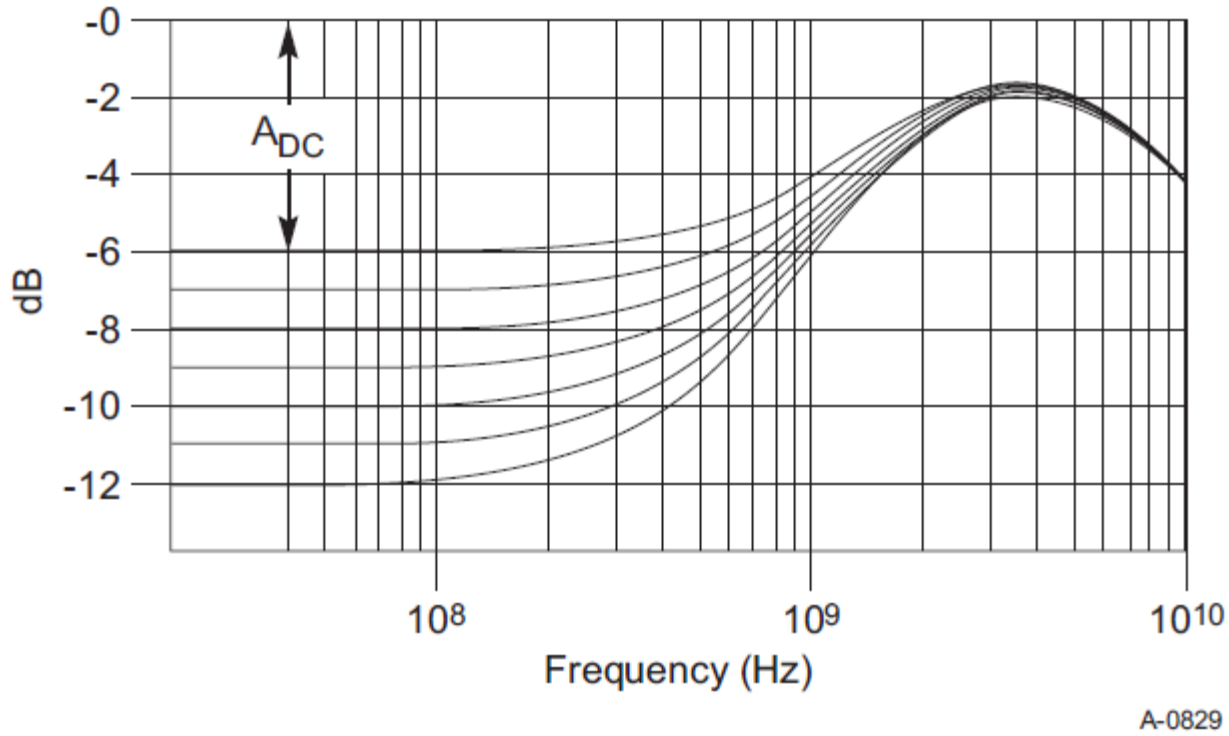
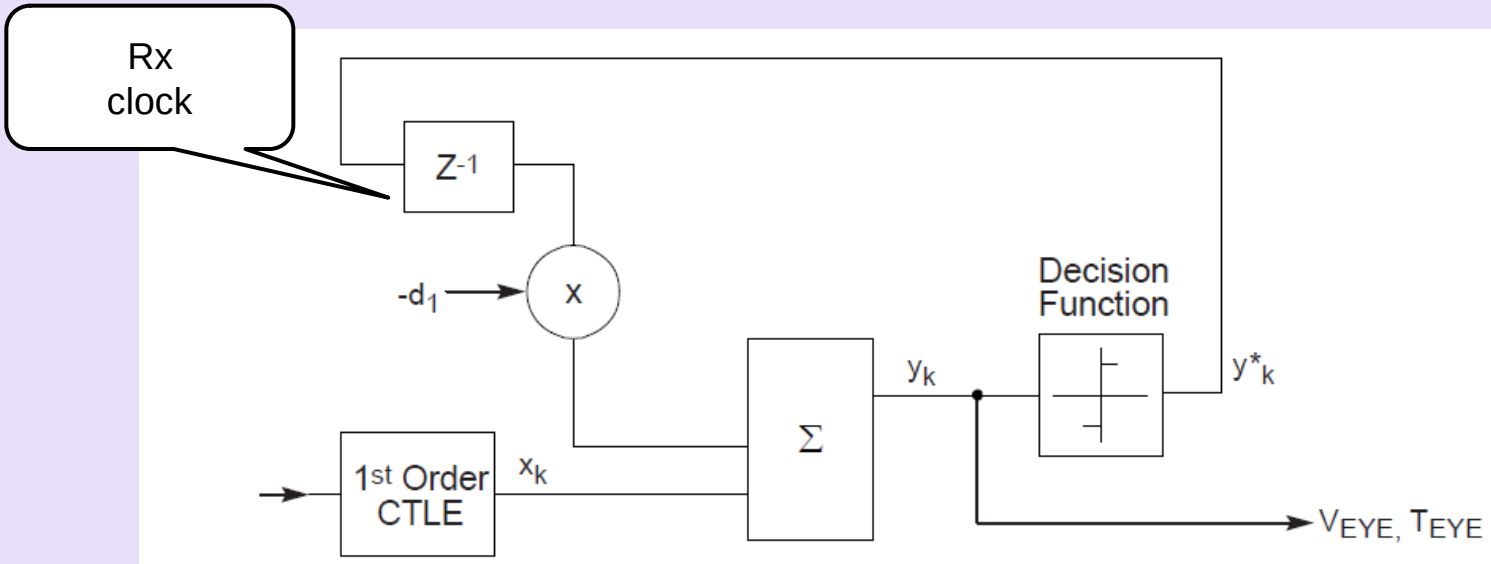


Figure 4-69: Loss Curves for Behavioral CTLE

PCIe 3.0 Rx DFE



$y_k = x_k - d_1 \mathrm{sgn}(y_{k-1})$

y_k = DFE summer differential output voltage.

y^*_k = decision function output voltage. $|y^*_k| = 1$

x_k = DFE differential input voltage

d_1 = feedback coefficient

k = sample index in UI

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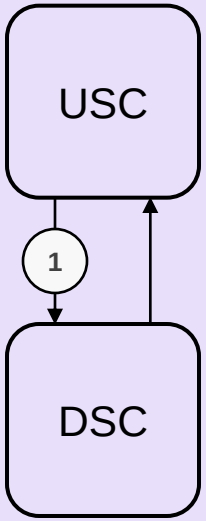
Figure 4-70: Equation and Flow Diagram for 1-tap DFE

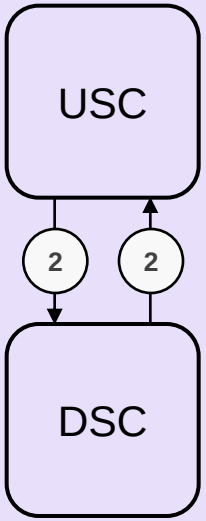
Native EQ Procedure

Phase 0



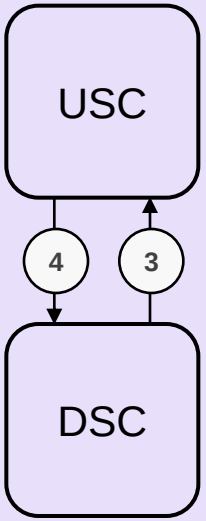
(1) USC Advertize Tx preset & Rx hint with 8b10b coding to Retimer USP

Phase 1



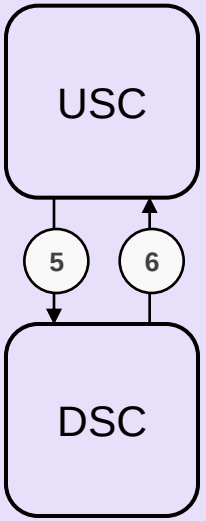
(2) Using presets from phase 0, change data rate to 8.0 GT/s. Achieve better than 10E-4 BER.

Phase 2



(3) DSC requests USC's Tx setting
(4) USC adjusts Tx setting.
DSC adjusts its Rx (CTLE and DFE) settings for each Tx request

Phase 3



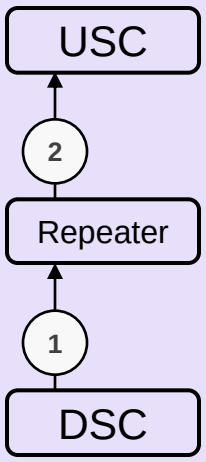
(5) USC requests DSC's Tx setting
(6) DSC adjusts Tx setting.
USC adjusts its Rx (CTLE and DFE) settings for each Tx request

PCIe 3.0 Repeater

PCIe 3.0 Repeater Challenges

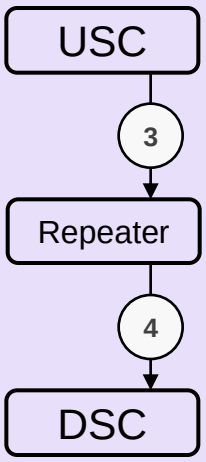
- No inferred EI
  - ✓ False EI detect
  - ✓ Not protocol aware, EIOS, SKP ordered set, FC update, etc.
- Rx
  - ✓ No recovered clock for DFE
  - ✓ Reference receiver has DFE
- Tx
  - ✓ No recovered clock for 3 stage FIR
  - ✓ Coefficients change as function of data rate
- EQ procedure

PCIe 3.0 Repeater Phase 2



(1) DSC requests Tx coefficients

(2) Repeater passes on Tx request to USC



(3) USC adjusts Tx coefficients

(4) Repeater continues to use programmed coefficients

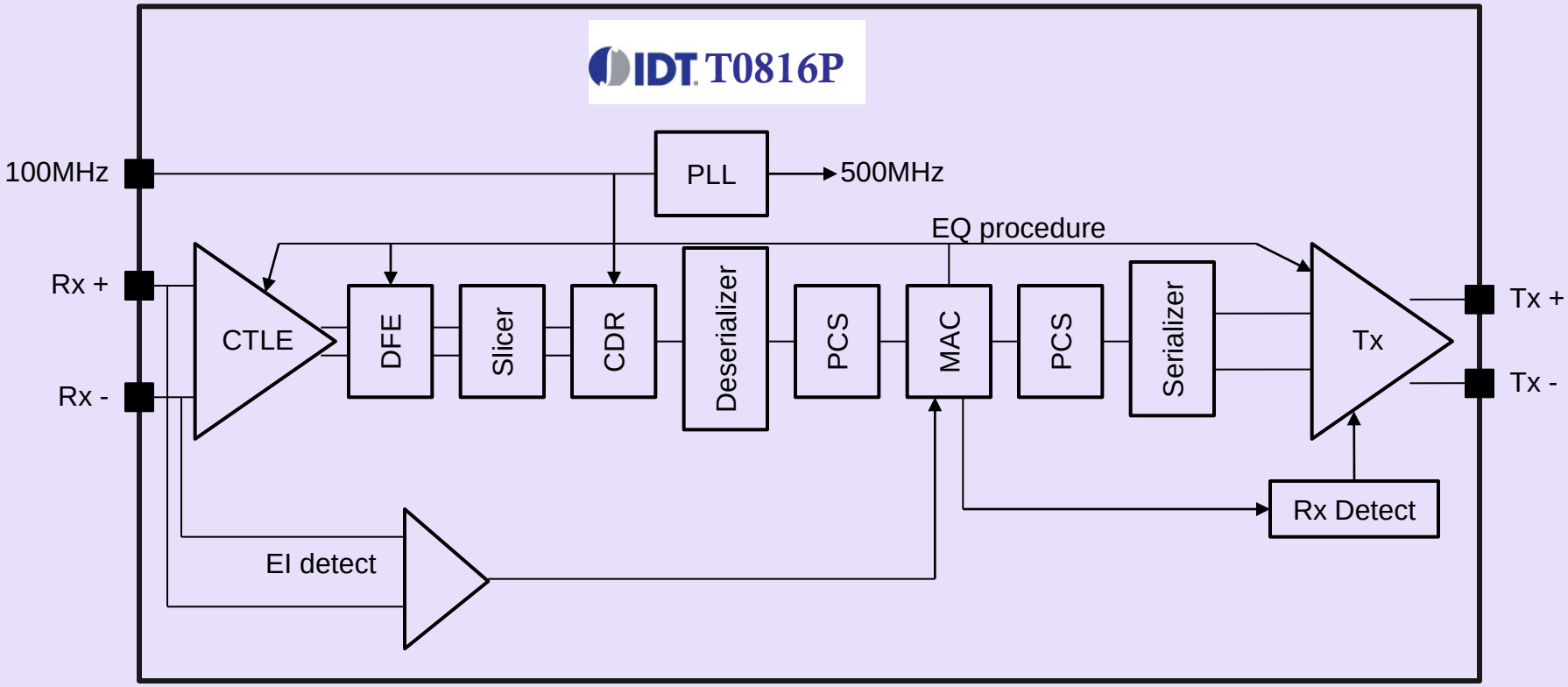
- The DSC's Tx requests affect the USC Tx, not the Repeater Tx
- Each segment requires adjustment of Tx and Rx to optimize BER
- Same issue for phase 3
- Similar issue for phase 0

PCIe 3.0 Digital Retimer

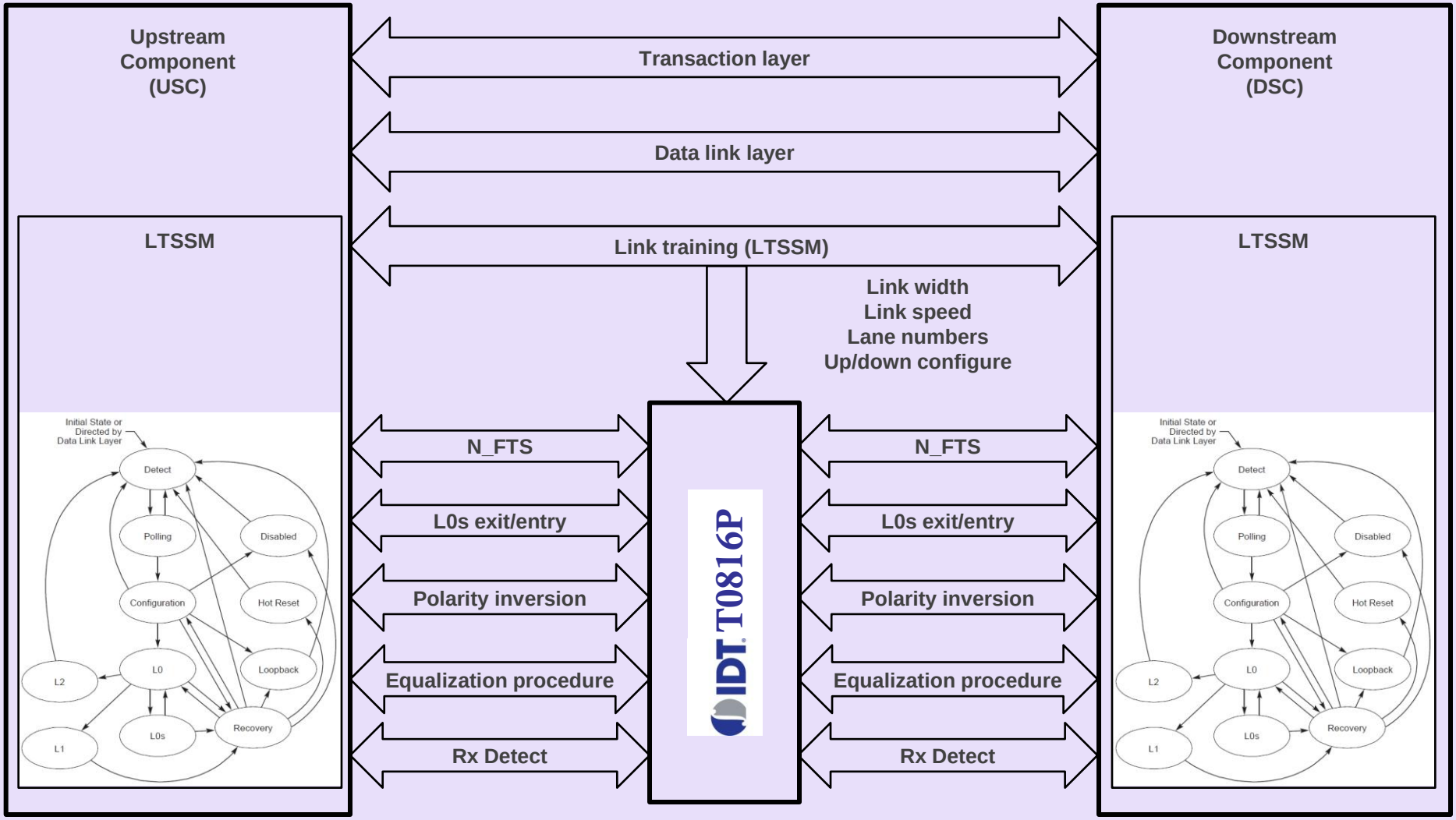
Retimer Features (Typical)

- Physical Layer aware
  - ✓ Terminate Phase 2/3 EQ procedure
  - ✓ Inferred EI, etc
- Transparent to DL and TL Layers
  - ✓ Low Latency
- Tx
  - ✓ 3 stage FIR, full coefficient matrix support
  - ✓ Generate compliance pattern
- Rx
  - ✓ CDR
  - ✓ 4 tap DFE
  - ✓ CTLE
  - ✓ On die scope
  - ✓ DDJ & RJ

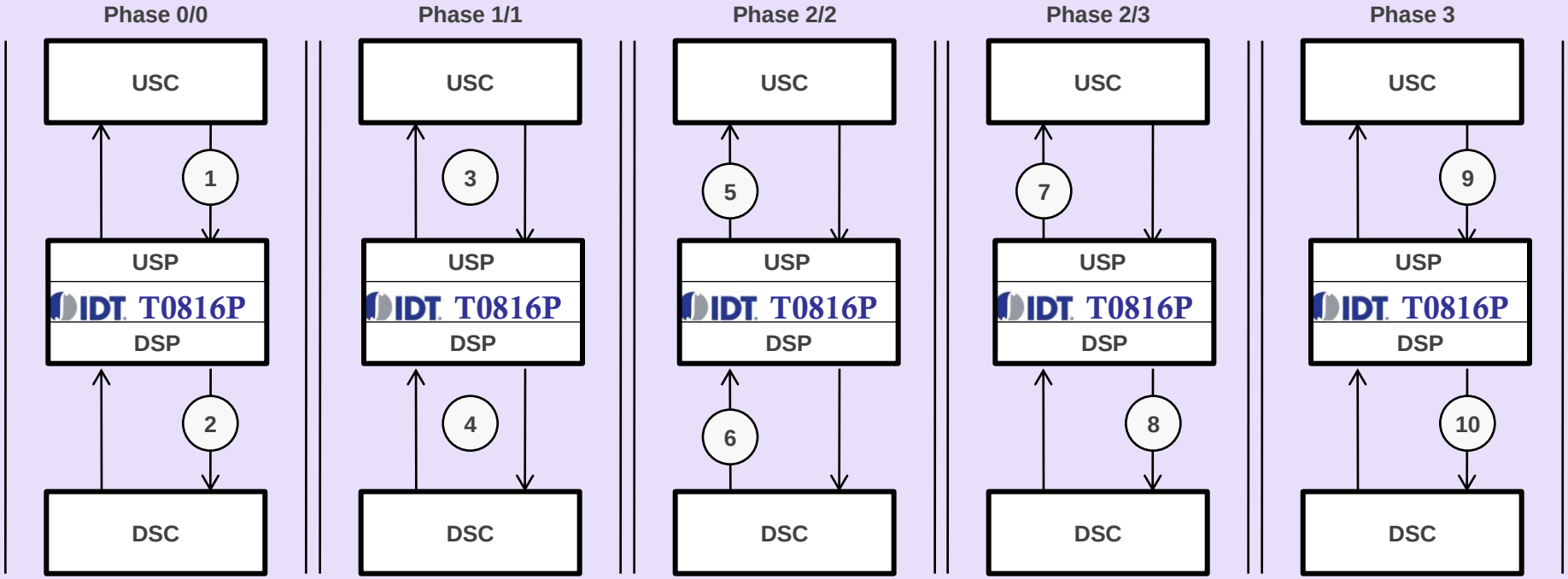
Retimer Diagram (Typical)



Protocol View



Retimer EQ Procedure



(1) USC Advertize preset & hint with 8b10b coding to Retimer USP

(2) Retimer DSP Advertize preset & hint with 8b10b coding to DSC

(3) Using presets at 8G data rate, get better than 10-4 BER between USC and Retimer USP

(4) Using presets at 8G data rate, get better than 10-4 BER between Retimer DSP and DSC

(5) Retimer USP adjusts USC Tx, and its Rx settings for optimal settings

(6) DSC adjusts Retimer DSP Tx, and its Rx settings for optimal settings

(7) Retimer USP ports waits in phase 2

(8) Retimer DSP adjusts DSC Tx, and its Rx settings for optimal settings

(9) USC adjusts Retimer USP Tx, and its Rx settings for optimal settings

(10) Retimer DSP waits in phase 3

Clock Compensation

- Retimers receive a 100MHz REFCLK
  - ✓ Common or non common
  - ✓ If SSCLK is used, must be common clock
- Non common REFCLKs must be +/- 300ppm
  - ✓ SSCLK +0/-5000 ppm
- CLK compensation is achieved by add/delete of SKP symbols in PCS
- Each lane is independent, however the add/delete must be coordinated across all lanes of the link

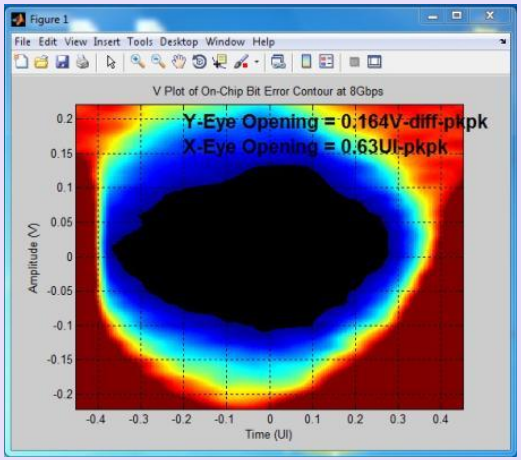
Lane Deskew

- The output skew is specified as 500ps (+ a few UI) in 3.0 base spec
- Due to clock uncertainty in SERDES/PCS lane deskew must be performed by a Retimer
  - ✓ Repeaters do not perform deskew, and must be considered in overall skew budget

Repeater Vs Retimer

Repeater

- Lowest latency
- Lowest power



Retimer

- Support for phase 0/1/2/3
- Better Tx
  - ✓ Full coefficient matrix
- Better Rx
  - ✓ CTLE + DFE
  - ✓ CDR, resets DDJ, and RJ
- Analog + digital EI detect
- Possible Debug Features
  - ✓ On die scope
  - ✓ Error detection
  - ✓ Loopbacks, PRBS

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