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PCI Express® 2.0 Electrical Compliance Tools and Demos

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Work In Progress

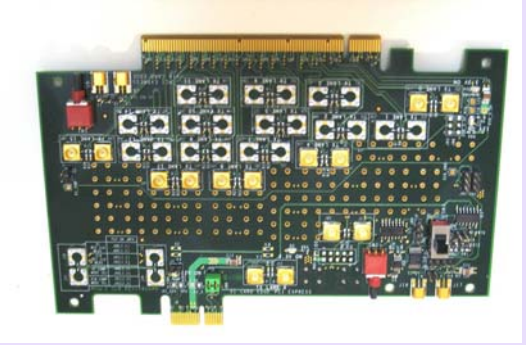
NOTE: The information in this presentation refers to .7 PCI Express test specifications still in the development process. This presentation reflects the current thinking of the Serial Enabling workgroup, but all material is subject to change before the specifications are released.

Agenda

- Review Motherboard Electrical Test Methodology
- Review Add-in Card Electrical Test Methodology
- Test Fixtures
  - ✓ Compliance Load Board 2.0
  - ✓ Compliance Base Board 2.0
- Electrical Analysis Algorithms
  - ✓ Add-in Card
  - ✓ Motherboard (dual port)
- Demonstrations of Electrical Tools

PCIe 2.0 Motherboard Electrical Tools Review

- **Motherboard Test Procedure**
  - ✓ CLB 2.0 Standard Test Fixture connected to slot under test.
  - ✓ Lane under test and clock connected through fixture to oscilloscope.
  - ✓ Motherboard under test enters compliance mode.
    - – Fixture provides features to select different compliance speeds and de-emphasis levels.
  - ✓ Data lane and reference clock sampled simultaneously
    - – 25 ps or smaller sample interval. ~ 1 million UI.
  - ✓ Standard Post Processing Analysis Software (Sigtest 3.0)
    - – Supports All Common RT Scope Data Formats
  - ✓ Standard Test Procedures For Specific Test Equipment



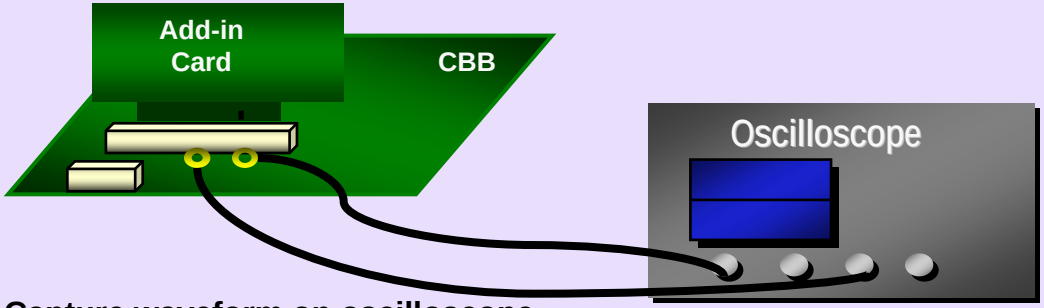
•Capture waveform on oscilloscope
•Run signal analysis software

Same Basic MB TX Test Setup/Process Used For 1.1 Program

RT Scope, Post Processing Software, Compliance Mode, etc . .

PCIe 2.0 Adapter Electrical Tools Review

- **Add-in Card Test Procedure**
  - ✓ CBB 2.0 Standard Test Fixture with add-in card to test connected.
  - ✓ Lane under test connected through fixture to oscilloscope.
  - ✓ Add-in card under test enters compliance mode.
    - – Fixture provides features to select different compliance speeds and de-emphasis levels.
  - ✓ Data lane sampled.
    - – 25 ps or smaller sample interval. At least 1 million UI.
  - ✓ Standard Post Processing Analysis Software (Sigtest 3.0)
    - – Supports All Common RT Scope Data Formats
  - ✓ Standard Test Procedures For Specific Test Equipment



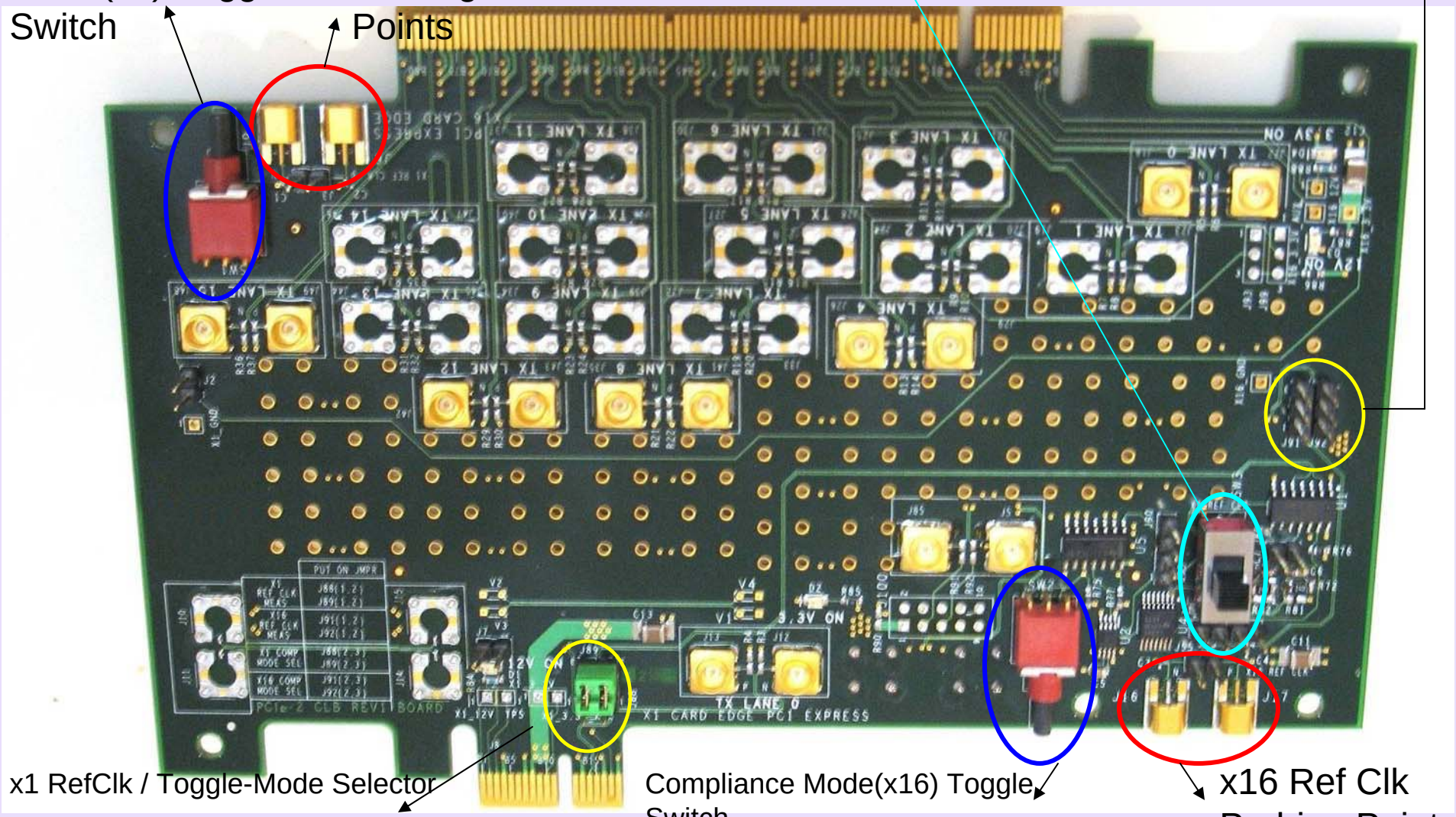
•**Capture waveform on oscilloscope**
•**Run signal analysis software**

Revised CBB for PCIe 1.1

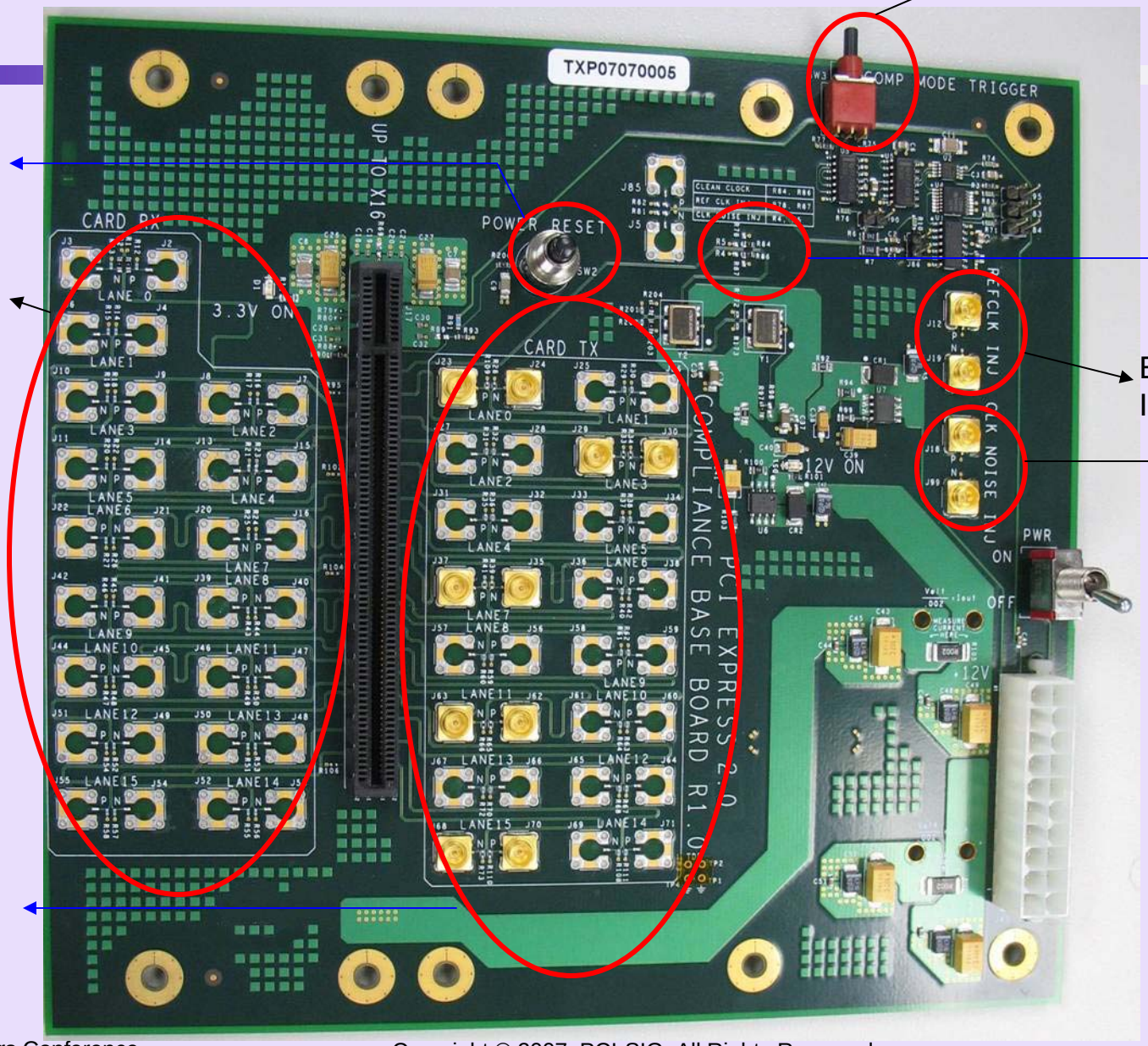
Same Basic AIC TX Test Setup/Process Used For 1.1 Testing

RT Scope, Post Processing Software, Compliance Mode, etc . .

CLB 2.0 (compliance) Features



CBB Features



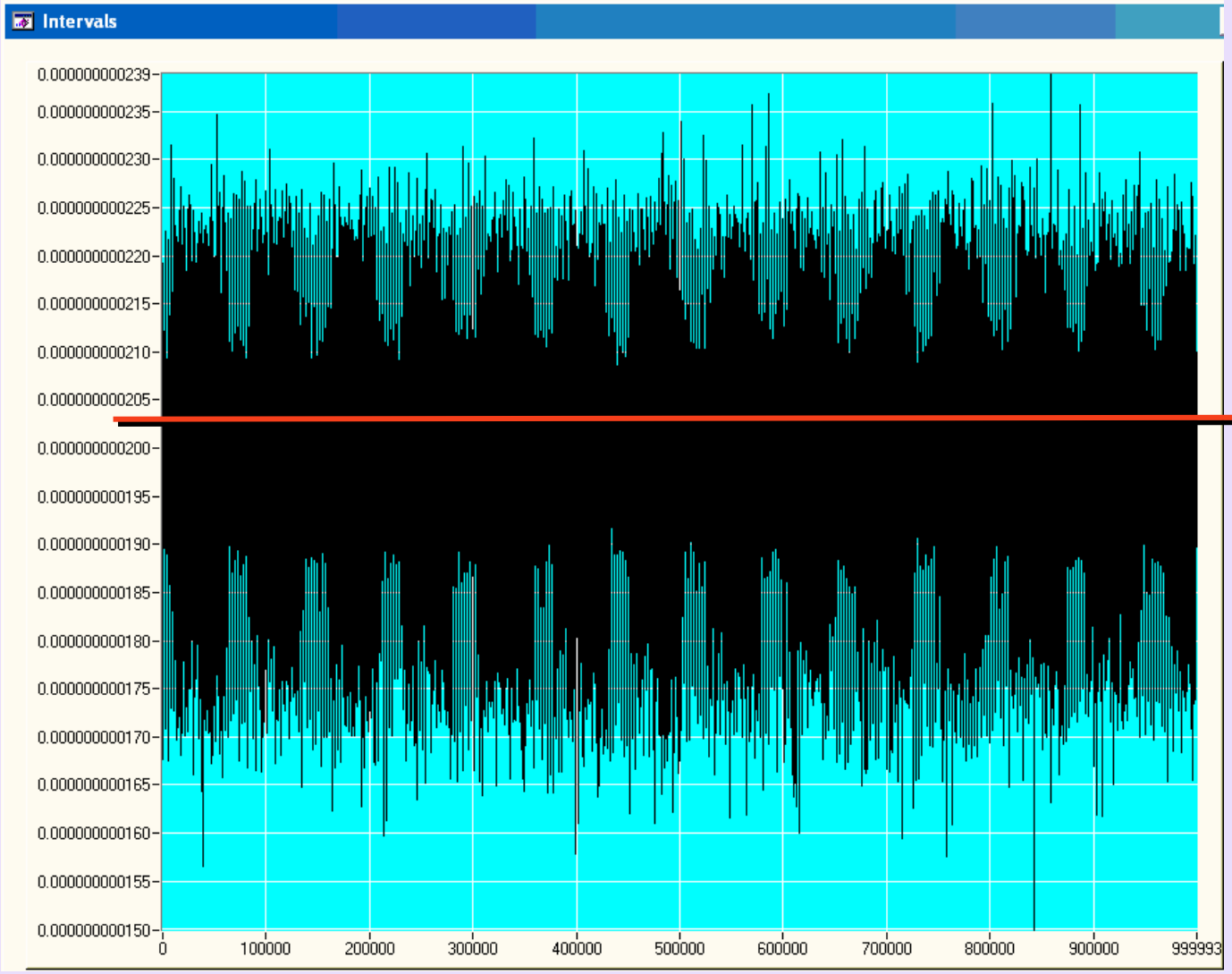
Analysis Overviews

- Add-in Card
  - ✓ Rj and Dj separation
  - ✓ Total jitter @ E-12 BER
- Motherboard
  - ✓ Dual Port

Jitter Analysis – Add-in Card

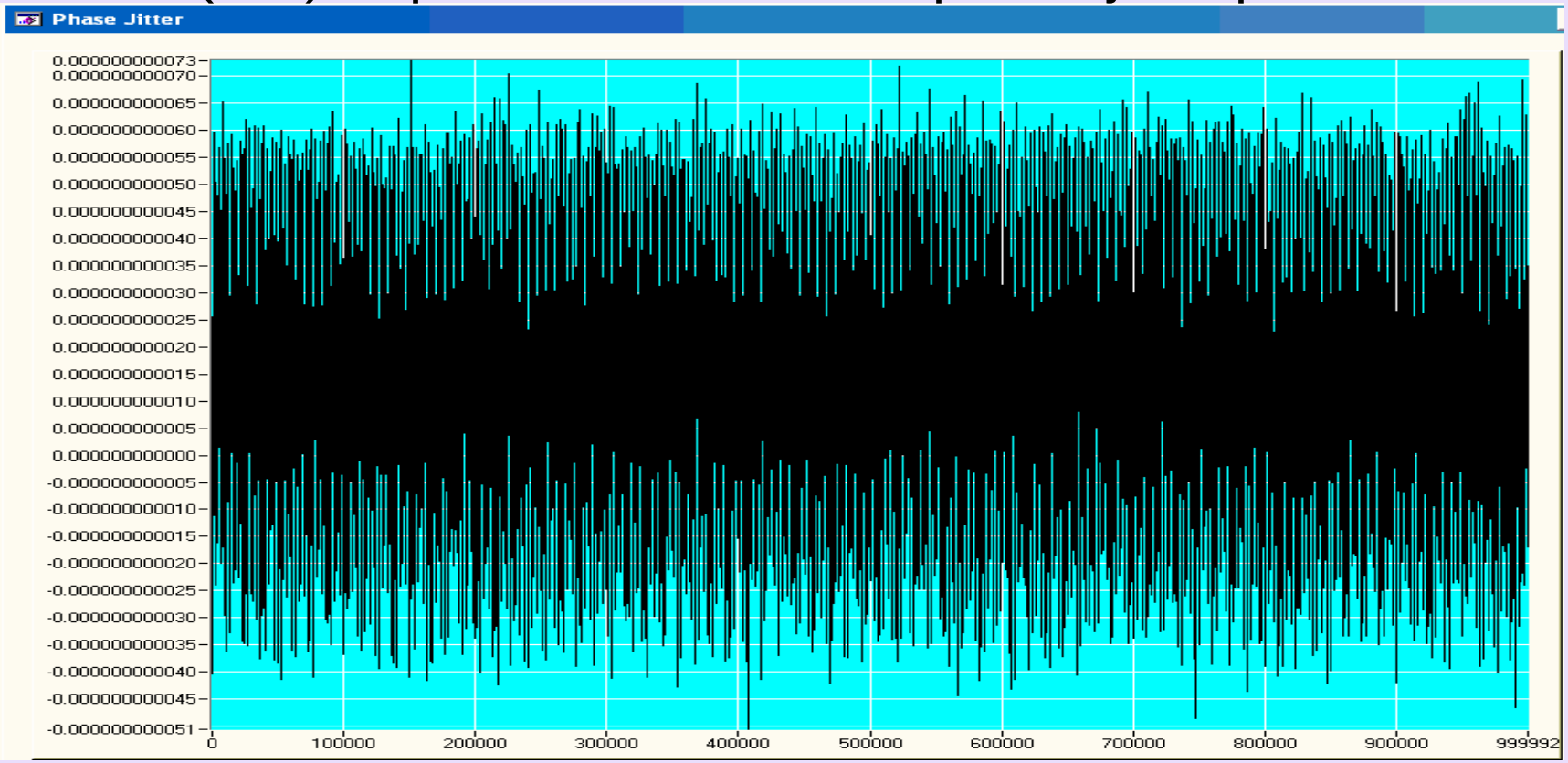
- Capture ~ 1 million UI of data (or equivalent) with sample interval of <= 25 ps.
- Find crossover locations using linear interpolation.
- Add additional crossovers to create 1010 signal
- Compute intervals between each crossover

Intervals

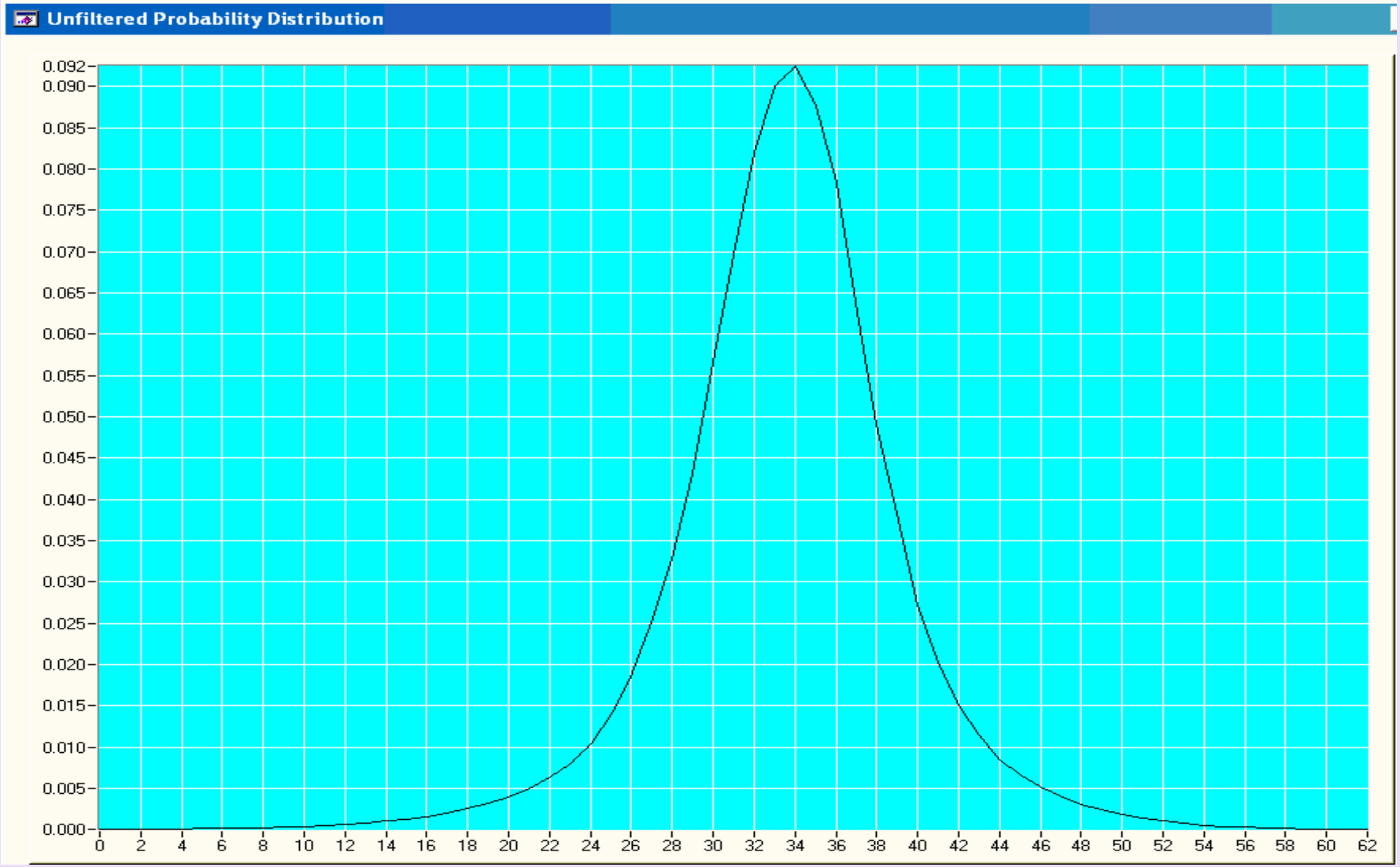


Calculate Accumulated/Phase Jitter

- Subtract average interval from each interval.
- Accumulate interval error across all data, gives Time Interval Error (TIE) or phase/accumulated phase jitter per interval.

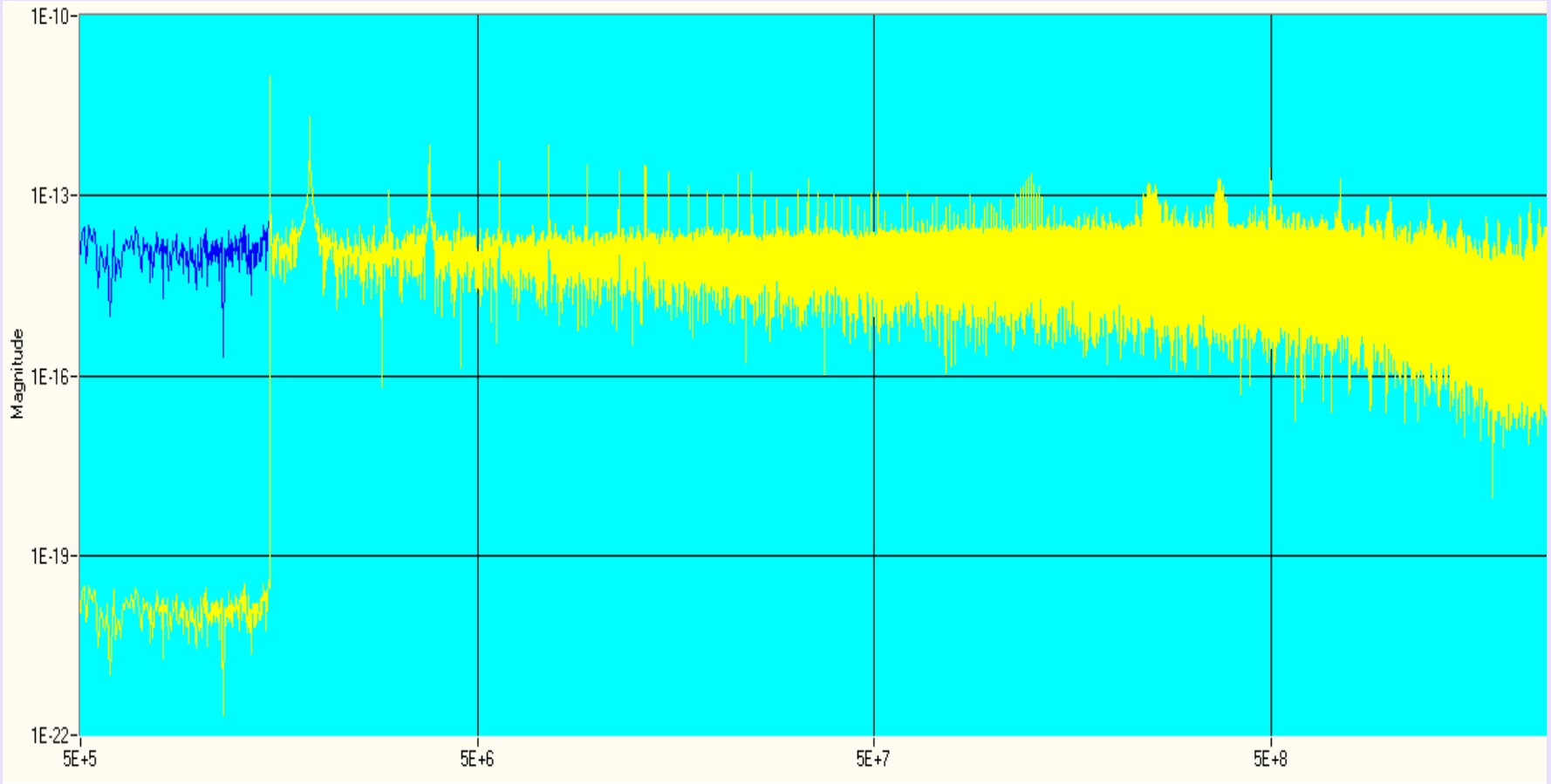


Phase Jitter Probability Distribution

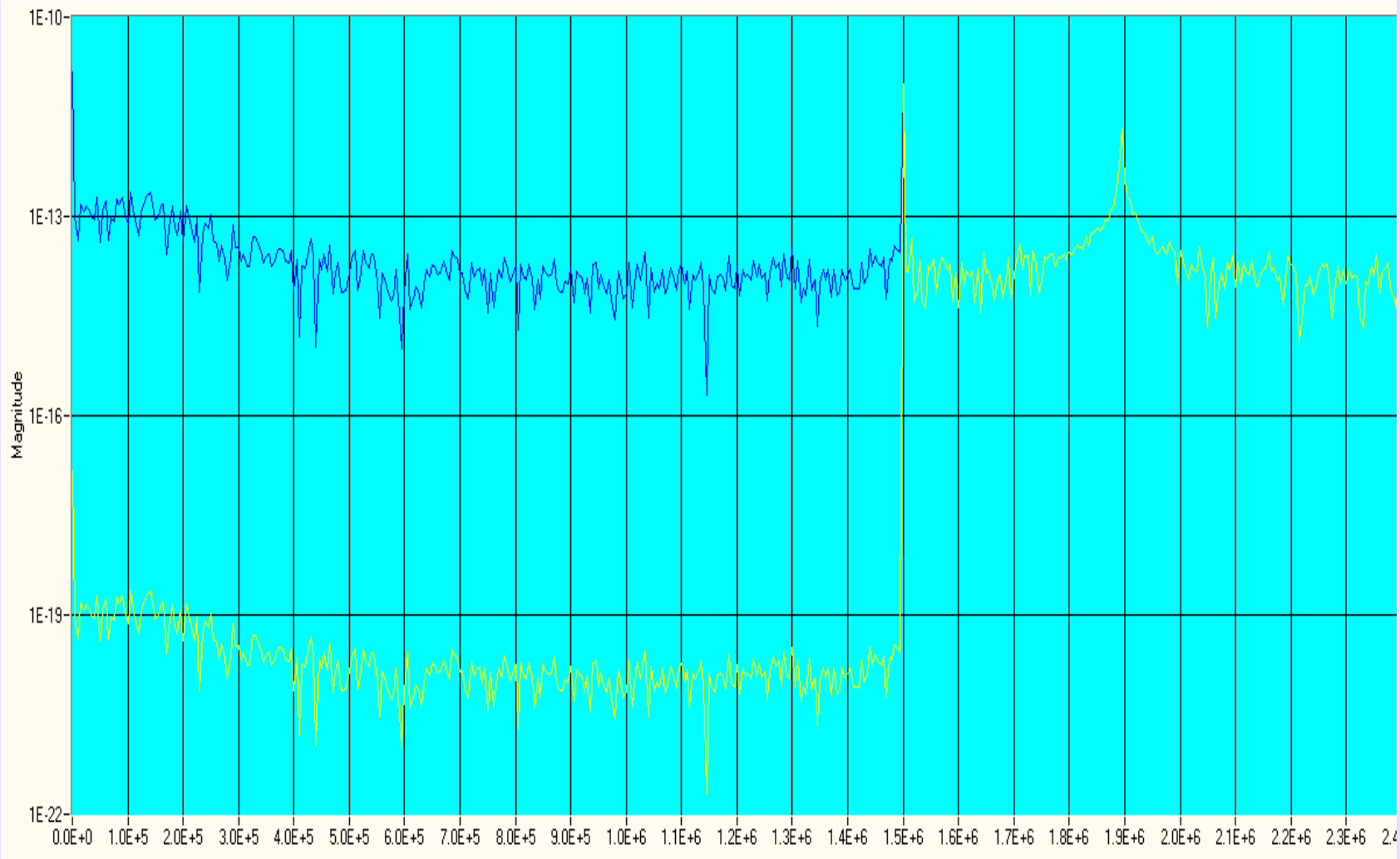


Frequency Domain Filter

- Compute FFT of phase jitter.
- Apply 1.5 Mhz Step High Pass Filter
  - ✓ Simple multiplication in frequency domain.

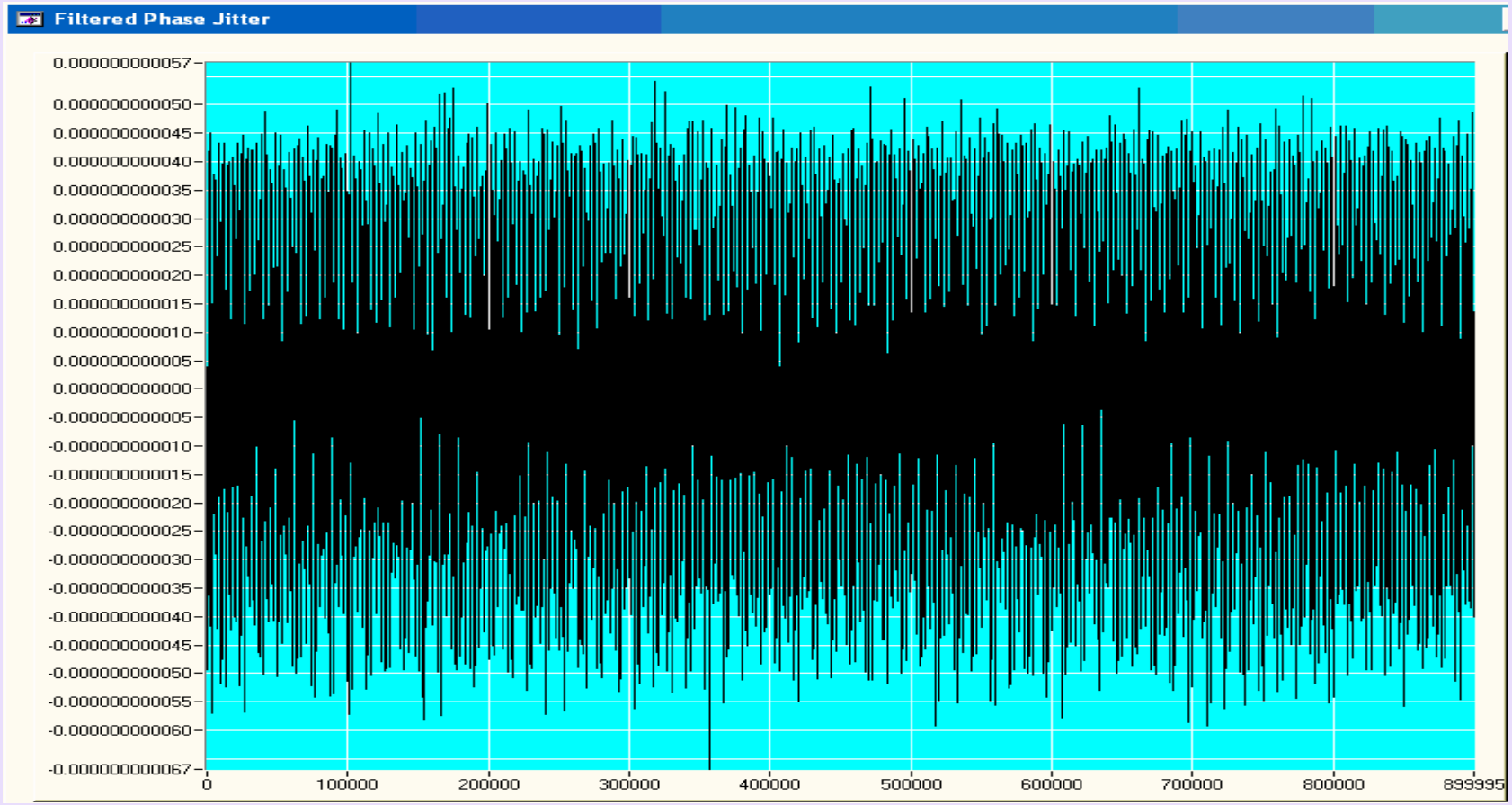


Frequency Domain Filter Non Log Plot – Low Frequency



Filtered Phase Jitter

- Convert filtered phase Jitter (Tj) back to time domain (IFFT).



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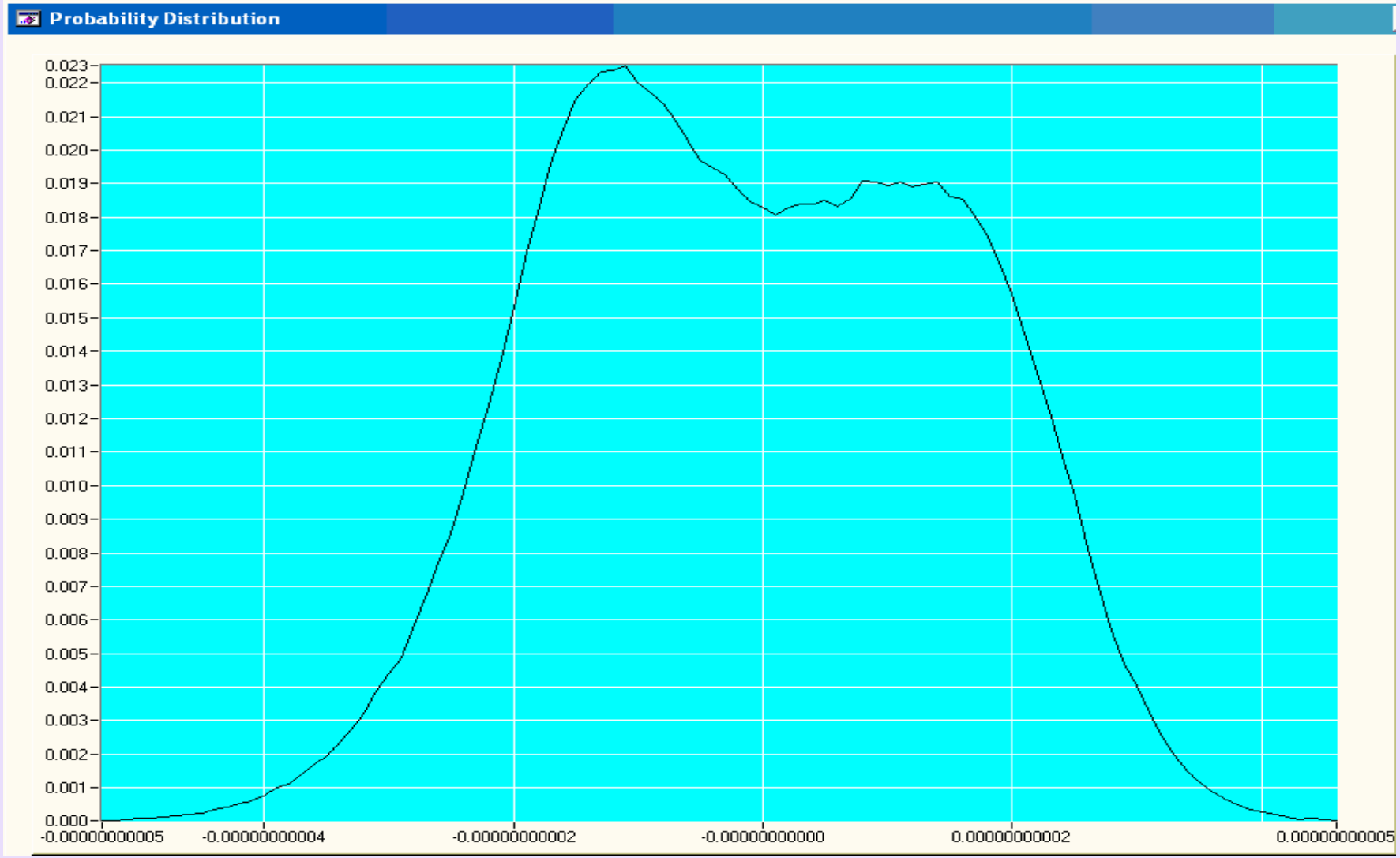
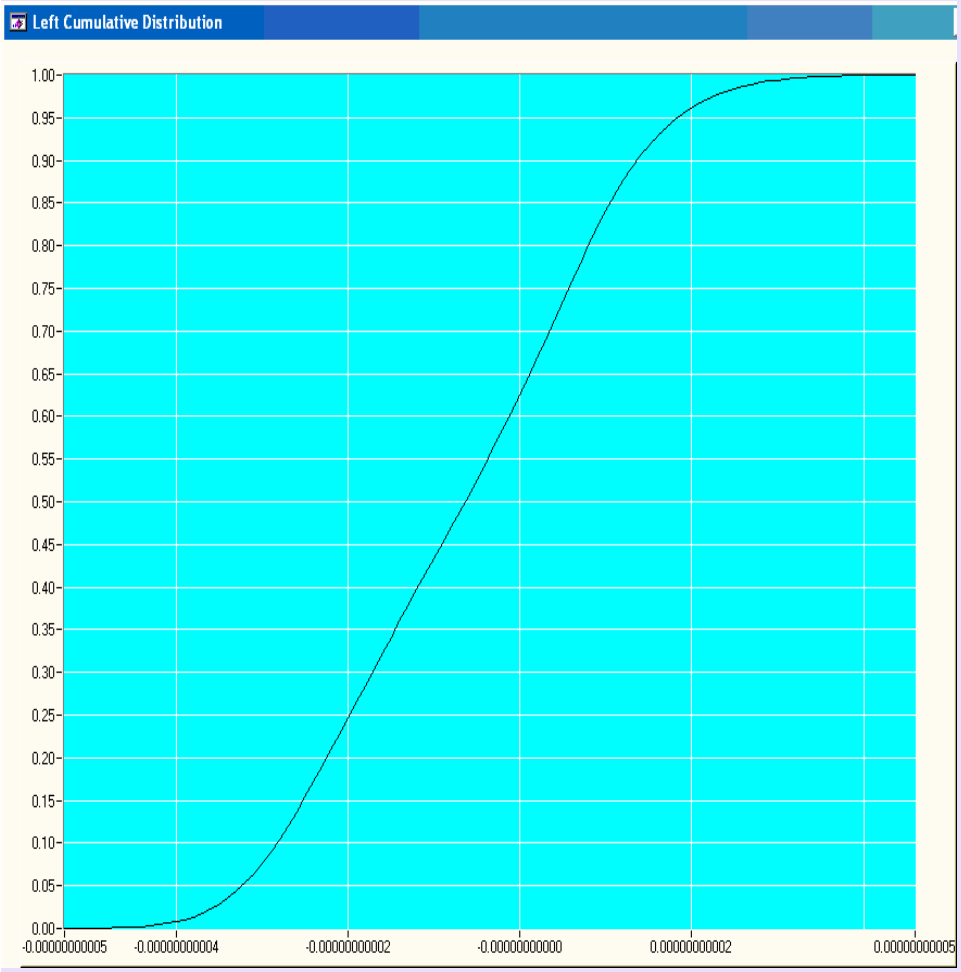
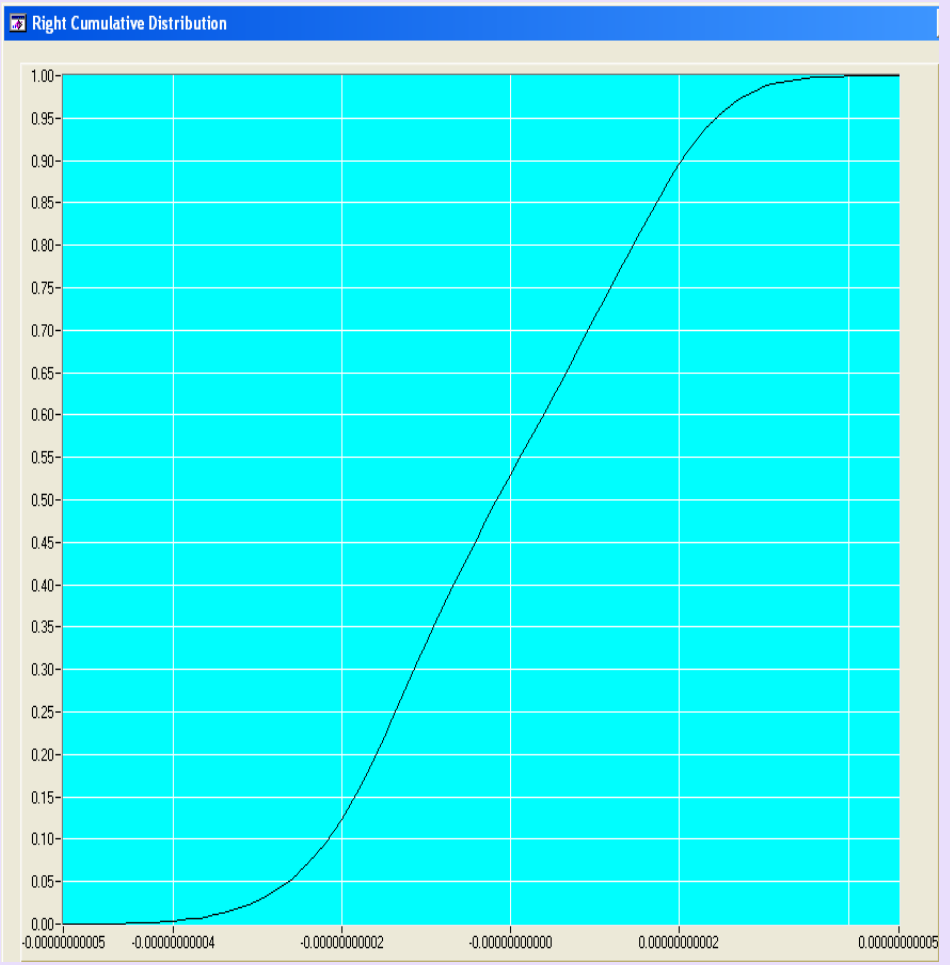


Cumulative Distributions

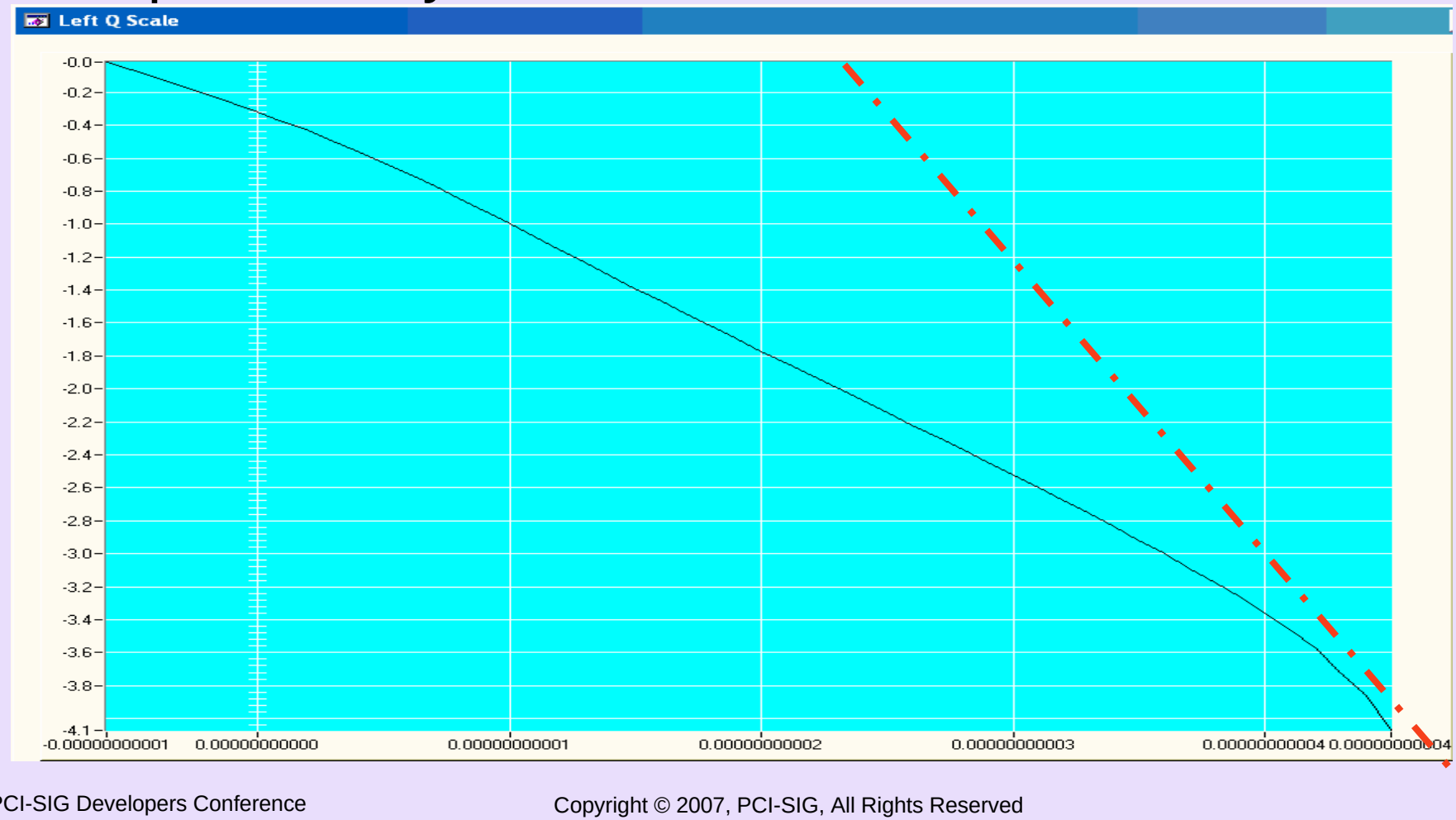
- Find left and right cumulative distribution functions (CDF)





Q Scale Cumulative Distribution

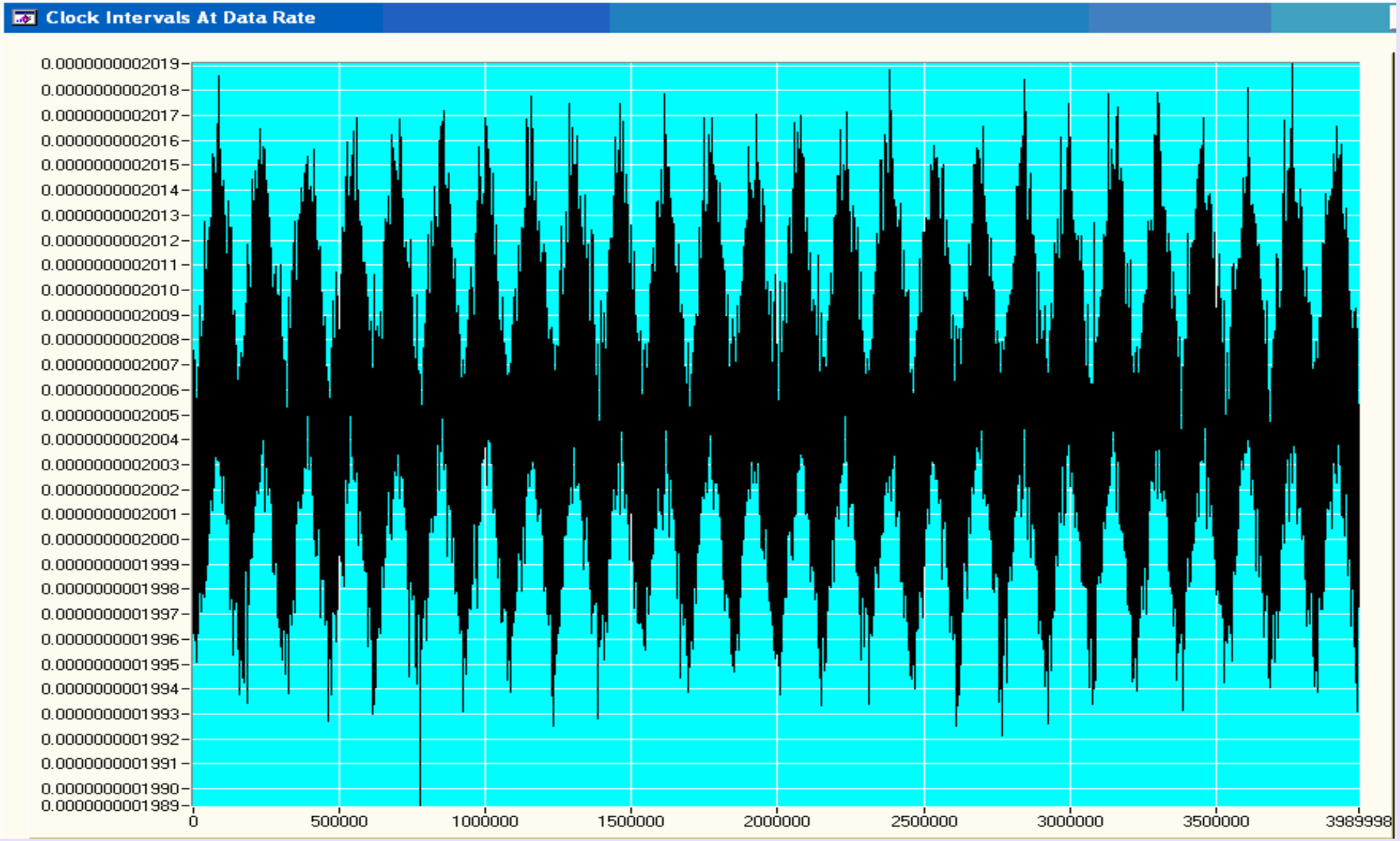
- Convert from CDF to Q Scale by applying complementary inverse error function.



Jitter Analysis – System Board

- Capture ~ 1 million UI of data and clock simultaneously (or equivalent) with sample interval of <= 25 ps.
- Find clock and data crossover locations using linear interpolation.
- Add additional crossovers to create 1010 signal
  - ✓ For clock – add crossover to convert to data rate signal
- Compute intervals between each crossover

Clock Intervals



Calculate Clock Accumulated/Phase Jitter

- Subtract average interval from each interval.
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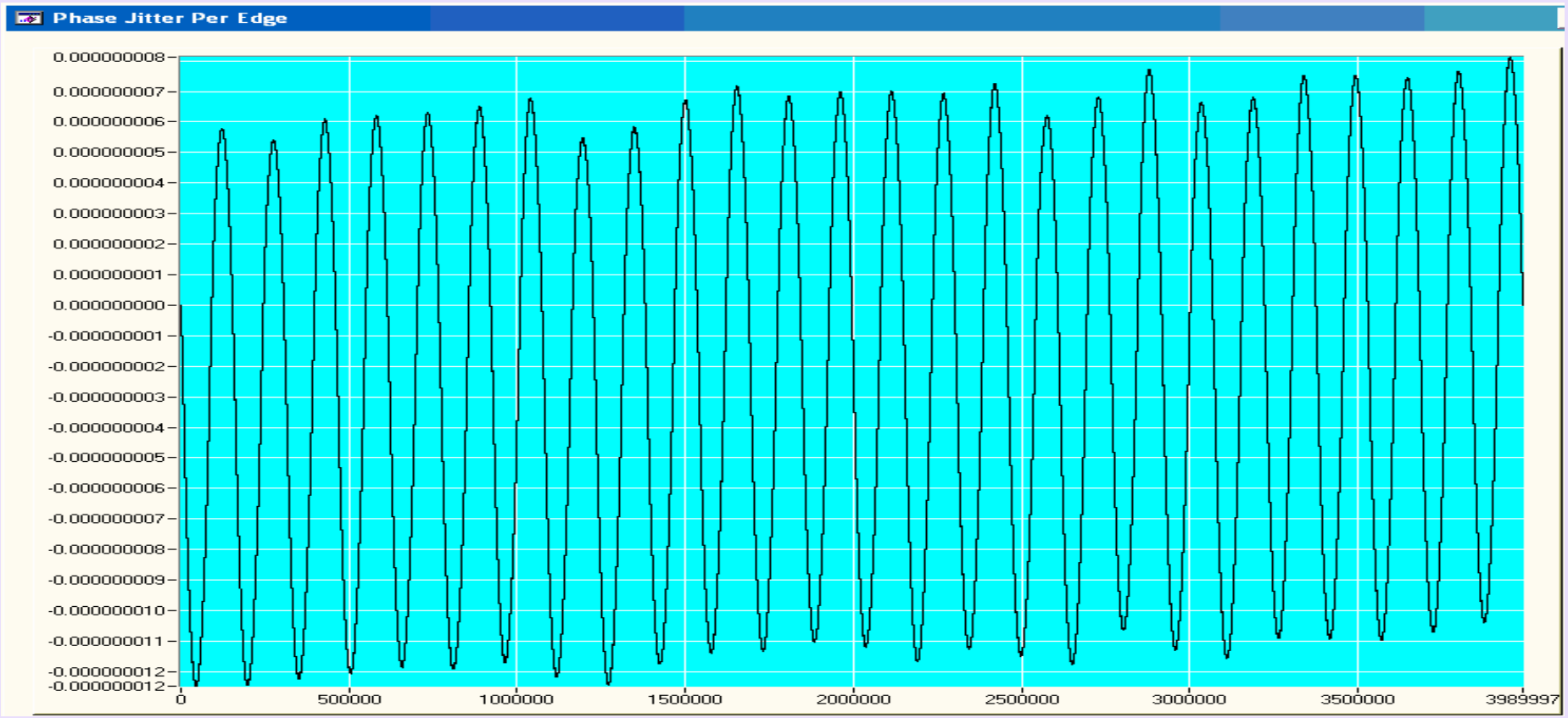
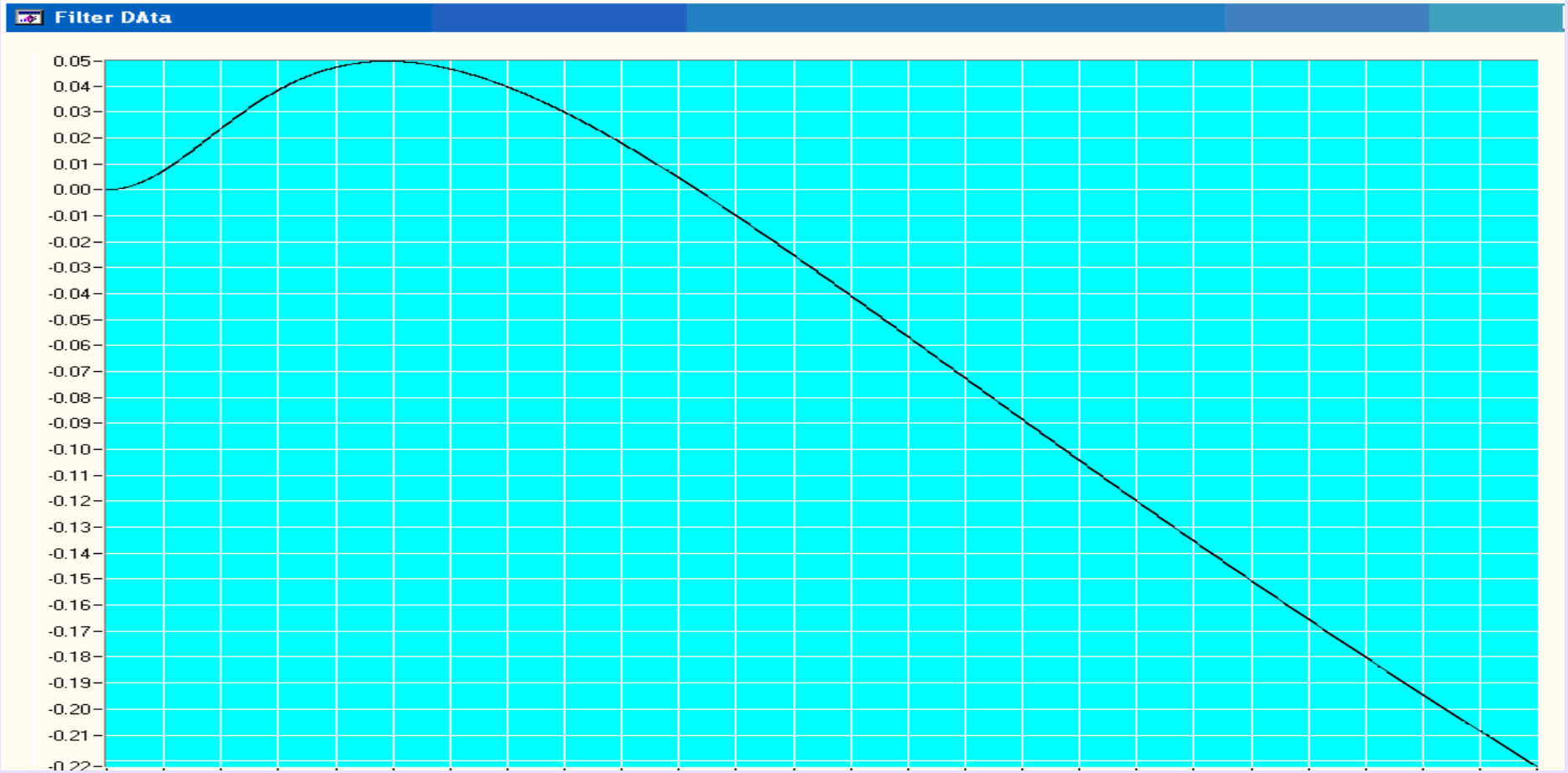


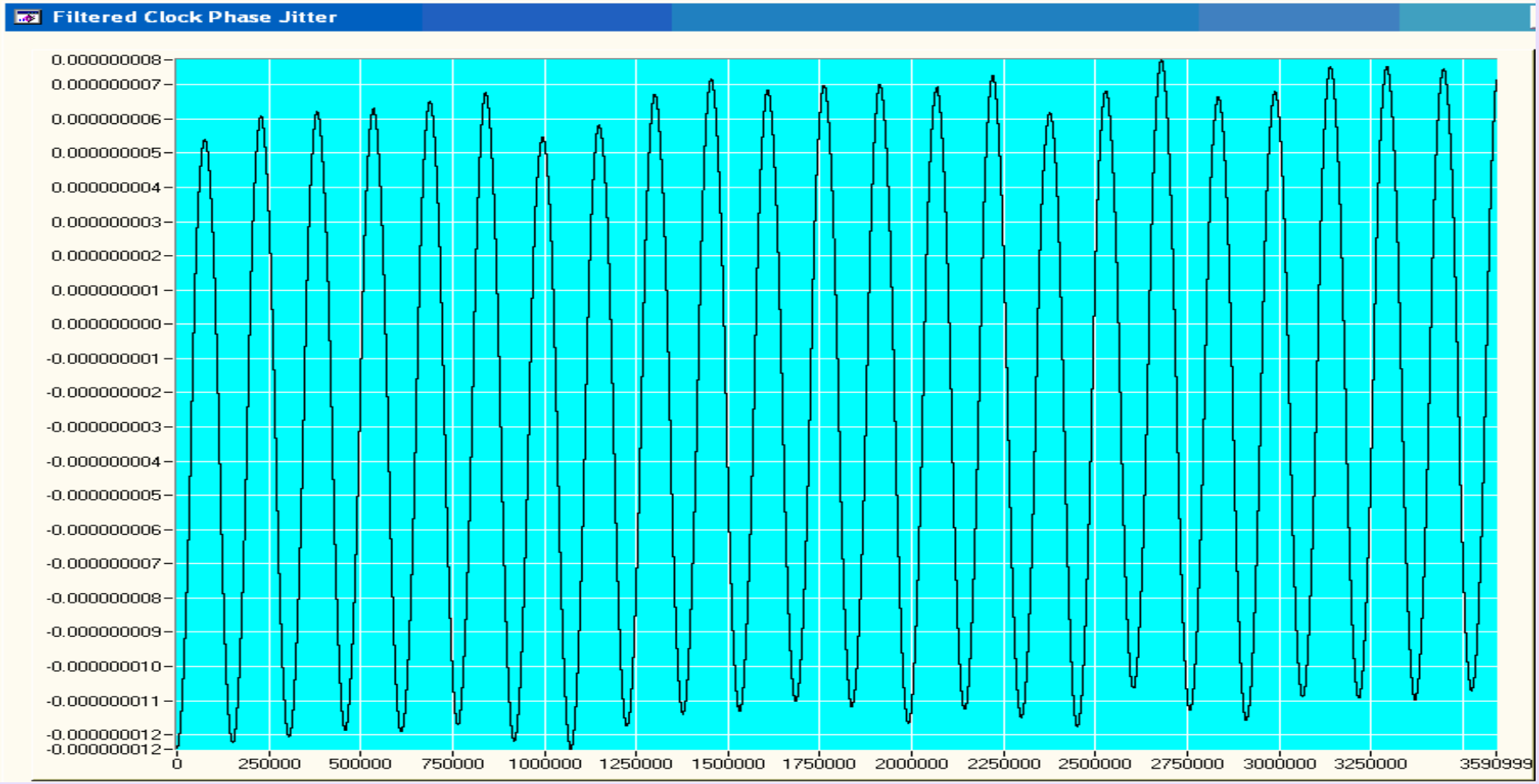
Frequency Domain Filter

- Compute FFT of clock phase jitter.
- Apply 5 Mhz, 1 dB Peaking PLL Filter
  - ✓ Simple multiplication in frequency domain.



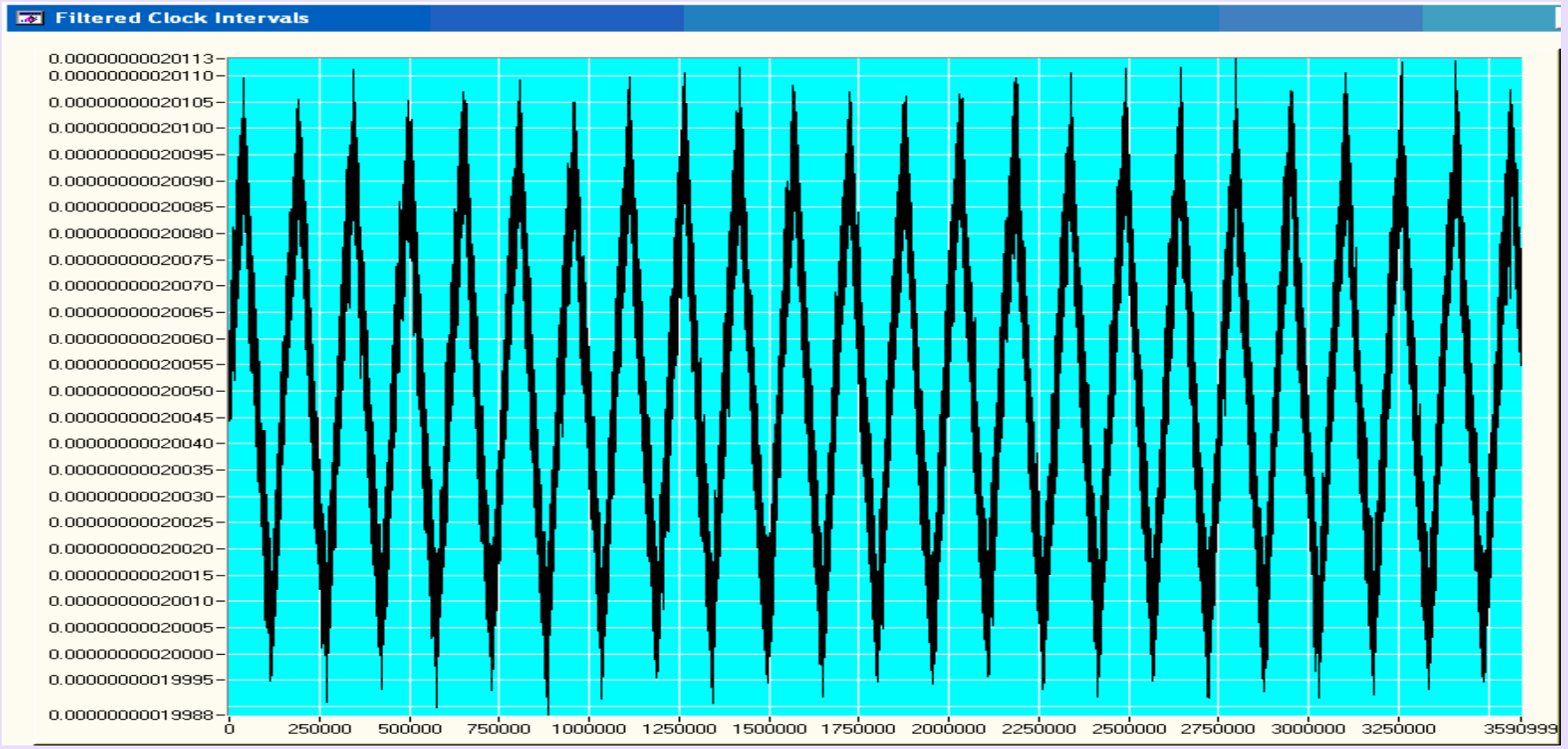
Filtered Phase Jitter

- Convert filtered clock phase Jitter (Tj) back to time domain (IFFT).



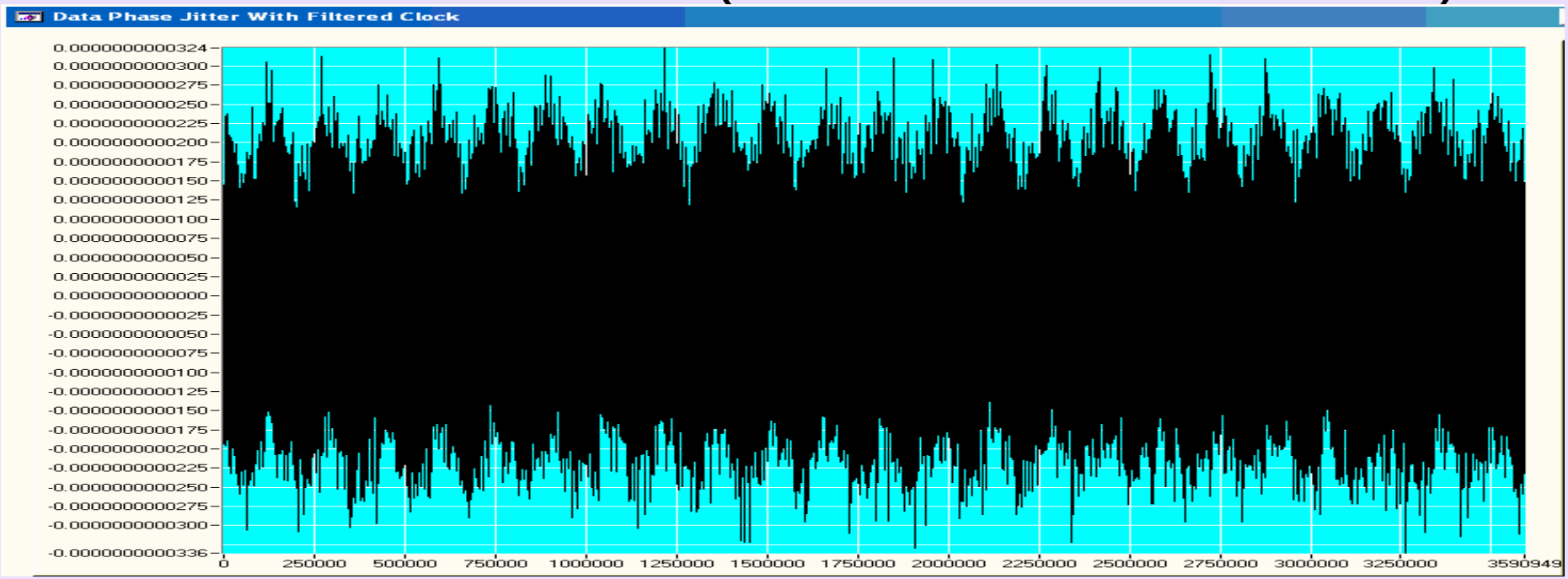
Convert Filtered Clock Phase Jitter to Intervals

- Decimate clock phase jitter array.
- Add average interval to each entry.



Calculate Data Jitter With Filtered Clock

- Subtract filtered clock intervals from data intervals.
- Accumulate result to get data phase jitter based on filtered clock.
- Repeat for different alignments between data and filtered clock intervals (+/- 3 ns -- +/- 15 intervals)



Dual Port – Final Steps

- Select data phase jitter based on filtered clock with alignment that give highest peak to peak jitter.
- Repeat the rest of the steps for add-in card analysis with the selected data phase jitter based on the filtered clock.
  - ✓ Obtain Djdd, TJ @E-12, and RJ RMS.
- Repeat process with two different PLL filter functions
  - ✓ 8 Mhz – 3 dB Peaking.
  - ✓ 16 Mhz – 3 dB Peaking.
- Final jitter numbers (Dj dd, TJ@E-12, RJ RMS) are the highest obtained with any of the different clock PLL filters.

Dual port method reclaims up to 20 ps+ Peak to Peak jitter lost with single port methods.

PCIe 2.0 Compliance Tool Demos

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