PCI Express® 2.0 Electrical Specification Overview

Dan Froelich
Intel Corporation

Agenda

- Jitter overview
- Gen2 PCI-e Electrical Layer Spec
  - ✓ Transmitter
  - ✓ Refclk
  - ✓ Channel
  - ✓ Receiver
- PCIe2 Physical Design Challenges

Jitter Overview

- System jitter must meet following relationship:

$$System\ T_J \equiv \sum Dj_{DD} + 2Q_{BER}\sqrt{\sum Rj_{DD}^{\ 2}} \leq 1.0UI$$

$$Component\ T_J \equiv Dj_{DD} + 2Q_{BER}Rj_{DD}$$

- Jitter is separated into two bins at 1.5 MHz
  - ✓ Below 1.5 MHz it is assumed that Rx CDR can track the jitter, up to some max
  - ✓ Above 1.5 MHz, it is assumed that CDR cannot track the jitter
  - ✓ Jitter > 1.5 MHz is counted in system jitter budget
- Binning is utilized for Tx, Rx, and Refclk
  - ✓ Spec places upper limit on jitter for both bins

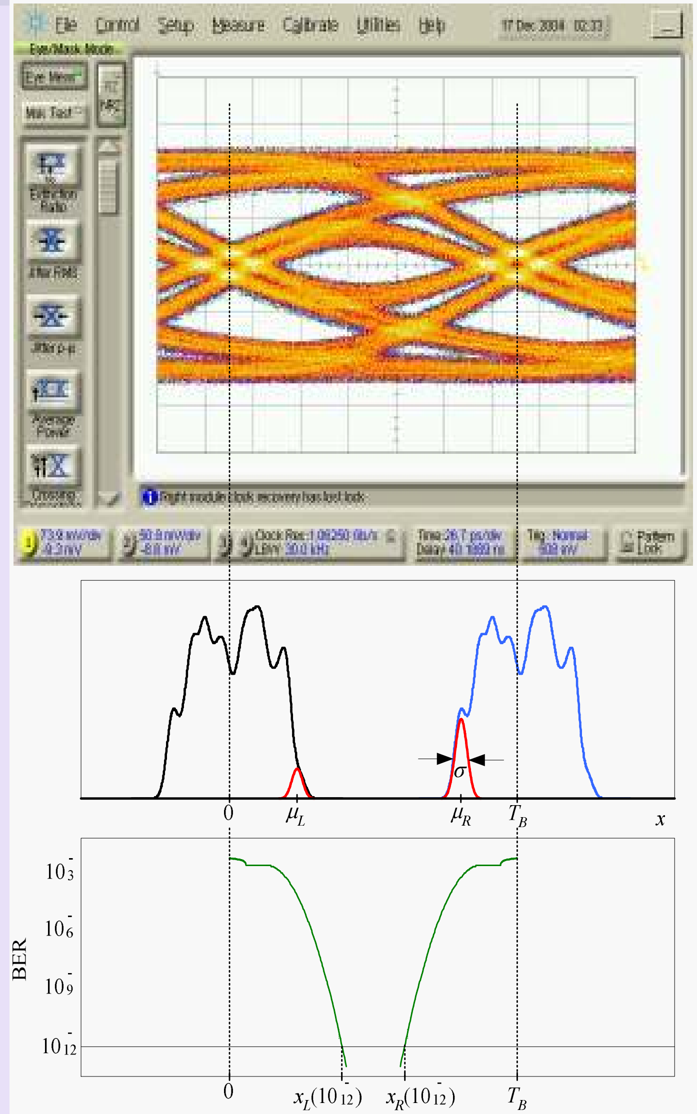
Dual Dirac Jitter Model

- Eye diagram measurement
  - ✓ This data can be obtained from many different instruments
- The PDF of left and right tail are plotted and a Gaussian distribution fitted to the tails

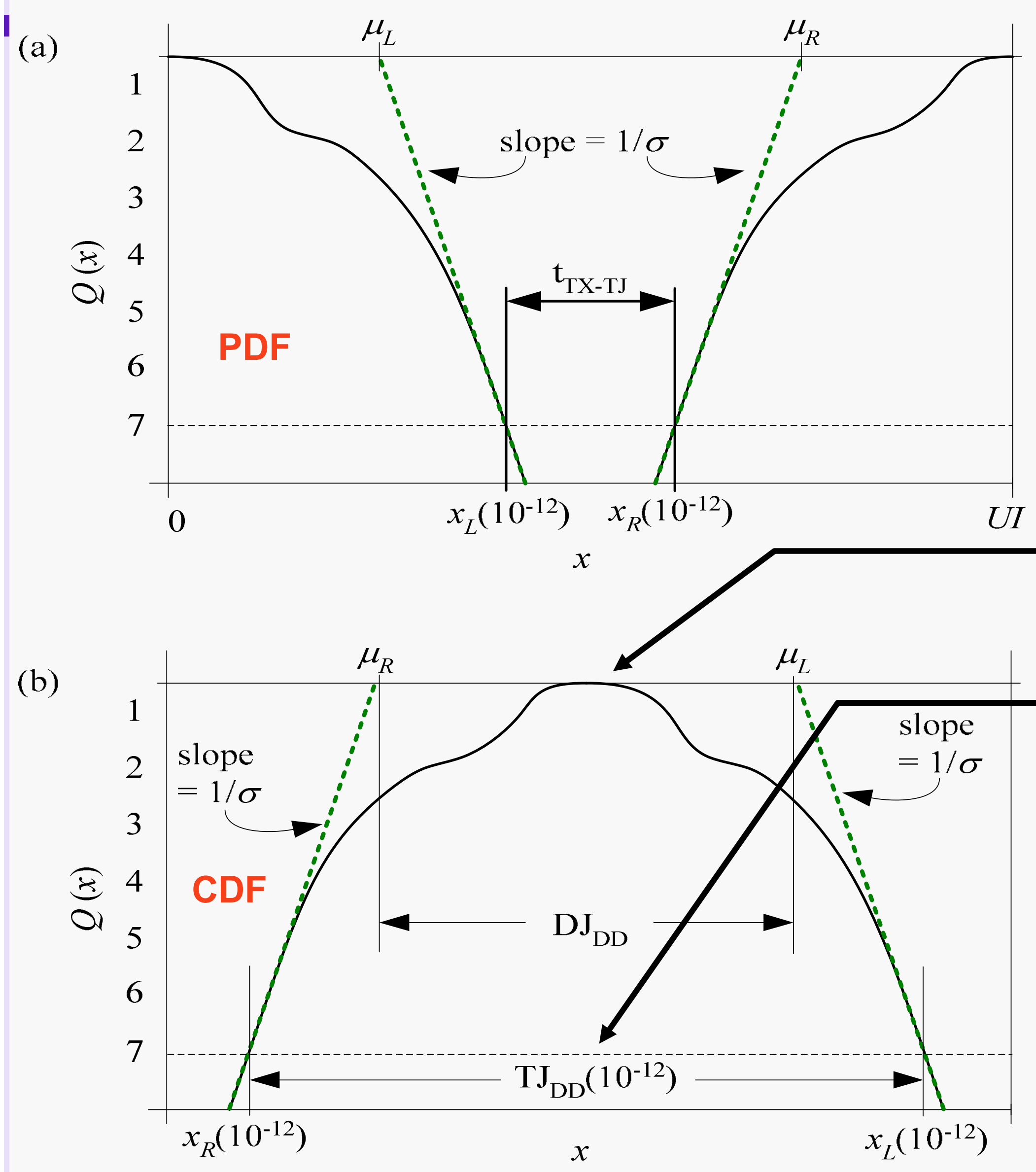
$$PDF = p(x) \equiv \frac{dF(x)}{dx} \qquad -\infty \;\; x < \infty$$

$$CDF = F(x) \equiv \int_{-\infty}^{x} p(u)\,du \qquad -\infty \;\; x < \infty$$

- The CDF is then calculated from the PDF, with the tails extrapolated with the fitted Gaussian to the BER limit of 10-12



Dual Dirac Jitter Extrapolation



The Dual Dirac methodology permits separation of jitter into random and deterministic components based on a sample size much smaller than that required if a direct BER measurement were done

Extrapolation of CDF to Q(x) = 1 yields DJ_{DD}

Extrapolation of CDF to Q(x) = 7 yields TJ_{DD}

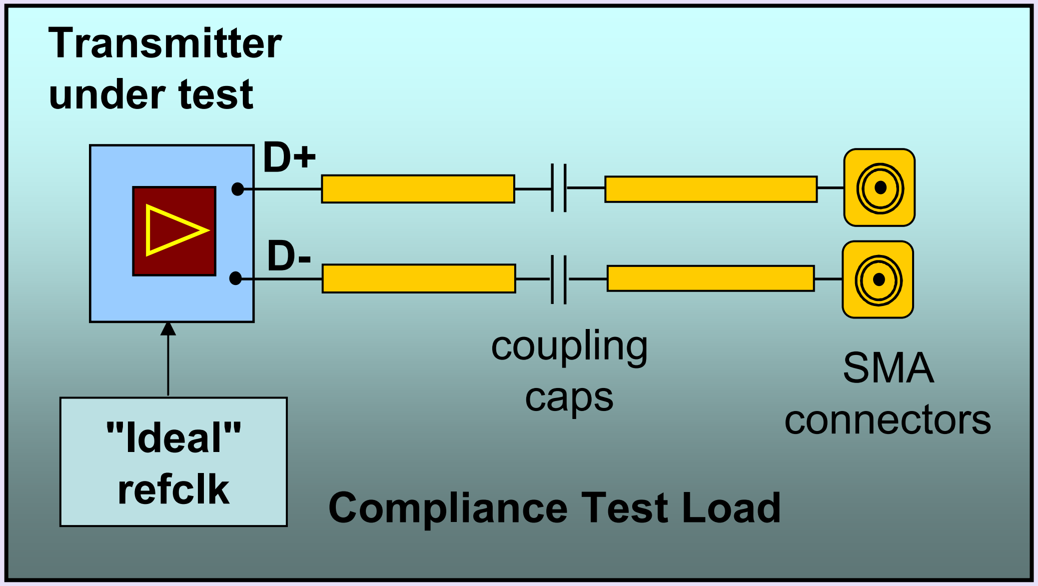
Reference JWG white papers

Gen2 Tx Spec Subsection

- Transmitter Electrical parameters
  - ✓ Compliance test load
  - ✓ Jitter filtering
  - ✓ Transmit PLL characteristics
  - ✓ Tx timing specifications
  - ✓ Tx Margining

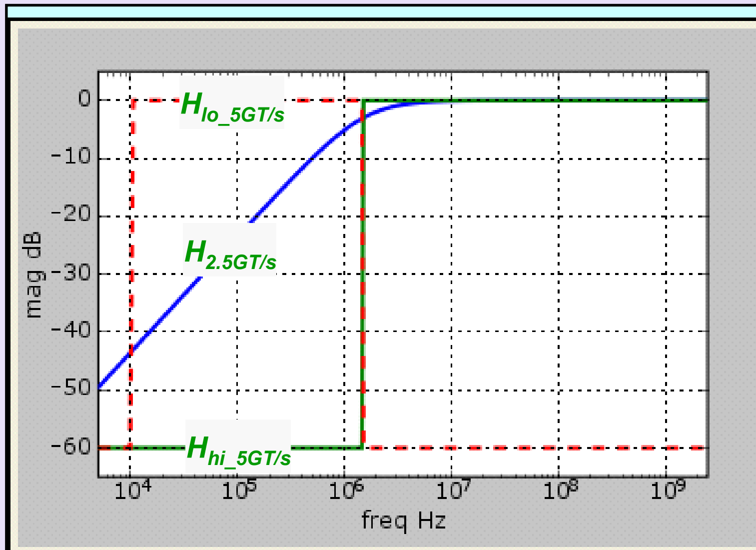
Transmitter Test Load

- Transmitter measurements referenced to the package pins
- Test configuration
  - ✓ “Ideal” Refclk generates negligible jitter, allowing Tx only jitter characterization
  - ✓ Traces and SMA connectors must be de-embedded from measurement



Tx Jitter Filtering

- Tx under test driven by “ideal”, very low jitter Refclk
- Different Tx filters applied for 2.5 vs. 5.0 GT/s
  - ✓ 2.5 GT/s utilizes a 1-pole HPF with fC of 1.5 MHz
  - ✓ 5.0 GT/s uses 2 filters
    - – 10 KHz – 1.5 MHz brick wall BPF
    - – 1.5 MHz brick wall HPF
- Filters remove jitter that is either a measurement artifact or otherwise trackable by Rx



$$H_{2.5GT/s} = \frac{s}{s + w_c} \qquad w_c = 2\pi f_T$$

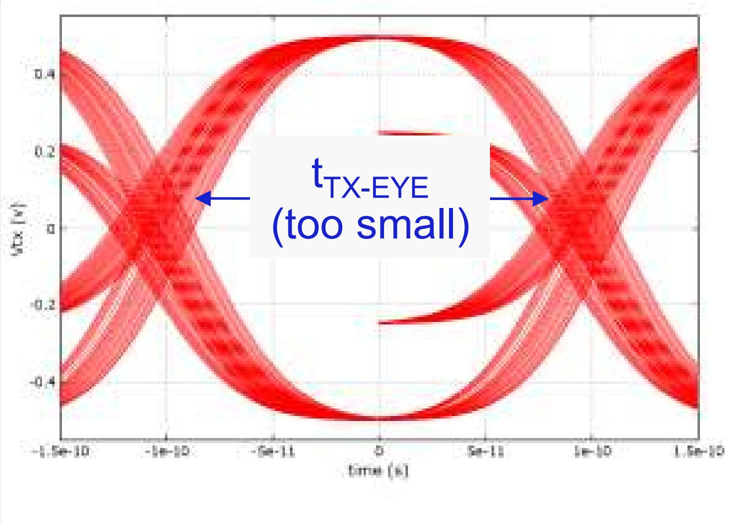
$$H_{hi\_5GT/s} = if\,(f >= f_T)\ then\ 1.0\ else\ 10^{-3}$$

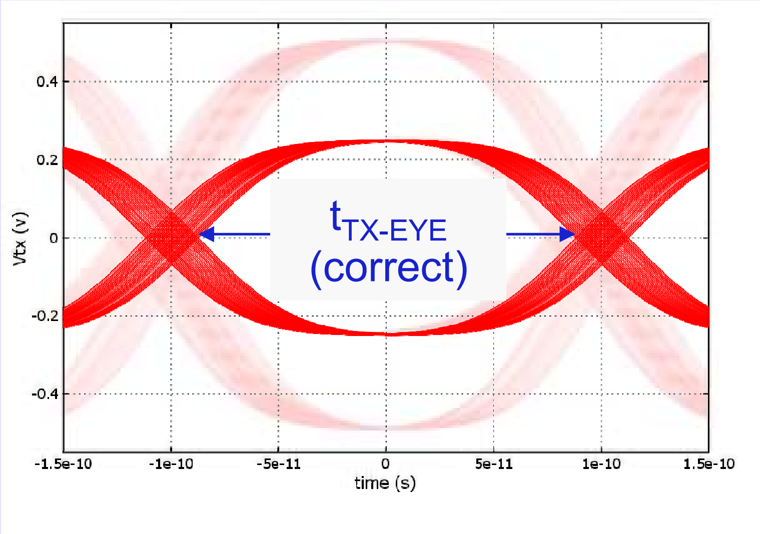
$$H_{lo\_5GT/s} = if\,(f < f_{10kHz})\ then\ 10^{-3}$$
$$elseif\ (f < f_T)\ then\ 1.0$$
$$else\ 10^{-3}$$

$$f_T = 1.5MHz$$

De-emphasis Induced Jitter

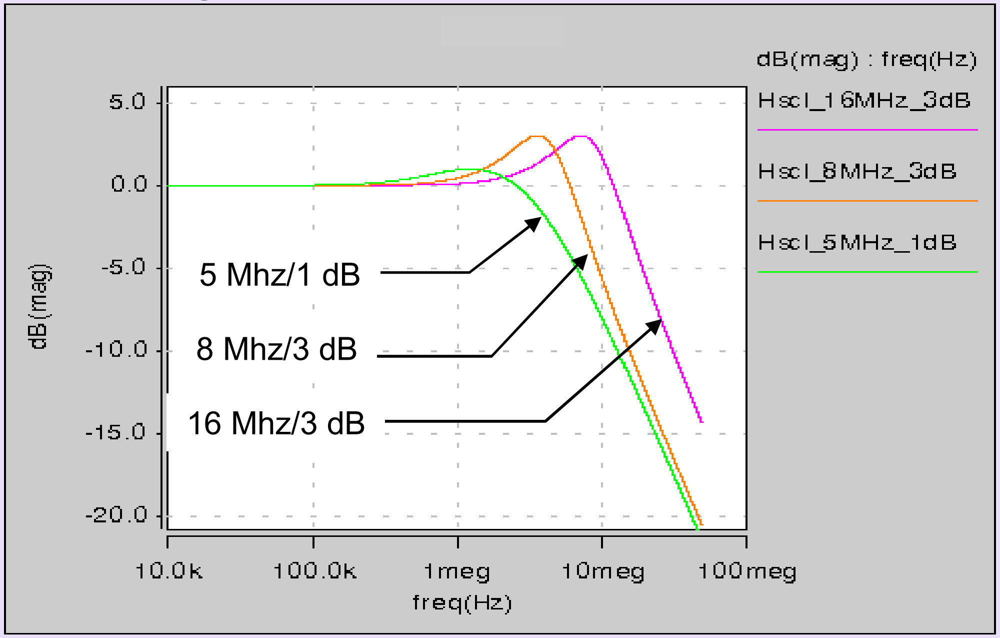
- Gen1 has -3.5dB of de-emphasis and more margin, so this effect was ignored
- Cannot be ignored in Gen2 with 6.0 dB
- De-emphasis causes a timing error in cumulative eye measurement
  - ✓ 10-17ps error (5-9% margin loss)
- Timing error can be removed by applying a form of measurement DFE





Transmit PLL Characteristics

- 5.0 GT/s requires Tx PLL bandwidth and jitter peaking to be more tightly controlled than for 2.5 GT/s
  - ✓ 2.5G had sufficient margin to allow a wide (1.5-22 MHz) PLL range
- Two combinations of min PLL peaking/BW defined
  - ✓ 5.0 MHz with 1.0 dB or 8.0 MHz with 3.0 dB
  - ✓ Max PLL BW/pkg = 16 MHz/3.0 dB



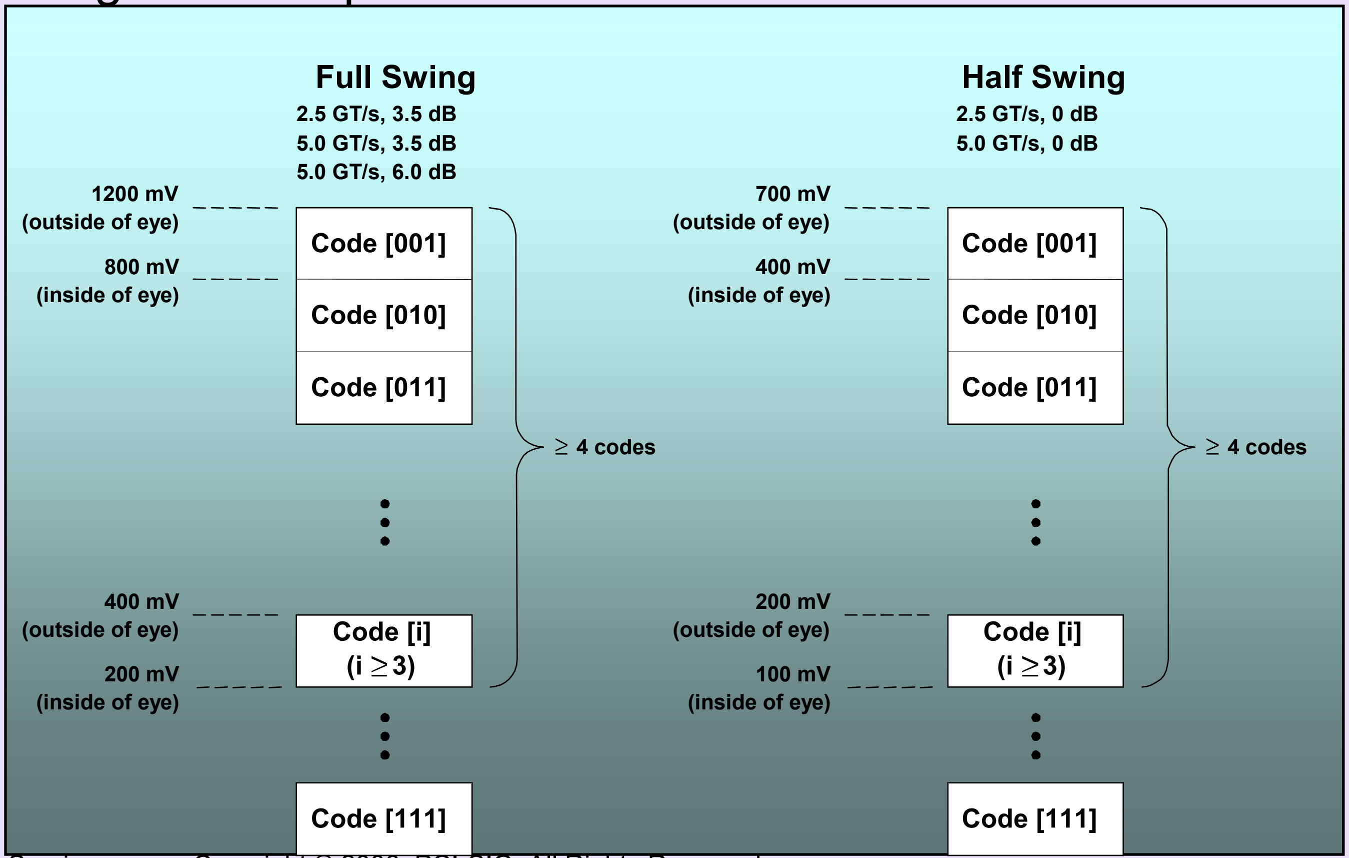
Transmitter timing specs

Parameter	Description	2.5 GT/s	5.0 GT/s
UI	unit interval	400 ps ±300 ppm	200 ps ±300 ppm
T_{TX-EYE}	Eye closure from all jitter sources	0.75 UI	0.75 UI
$T_{TX-MED-MAX}$	Max time between median and max Δ from median	0.125 UI	--
$T_{TX-HF-DJ-DD}$	> 1.5 MHz Dj	--	0.15 UI max
$T_{TX-LF-RMS}$	< 1.5 Mhz RMS jitter	--	3.0 ps RMS max
$T_{TX-RISE-FALL}$	Tx rise/fall time	0.125 UI max	0.15 UI max
$T_{RF-MISMATCH}$	Rise/Fall Mismatch	--	0.1 UI
$T_{MIN-PULSE}$	Minimum single pulse	--	0.9 UI min

Substantial differences between 2.5 and 5.0 GT/s based on need to account for additional jitter effects (jitter amplification) and differences in jitter budgeting methodology.

Transmitter Margining

- Required for all devices adhering to 0.9 spec (both 2.5 and 5.0 GT/s
- Spec requires voltage margining; jitter margining is optional
- Min of 4 codes must map into min/max voltage levels below
- Margining set by config bits on a per link basis

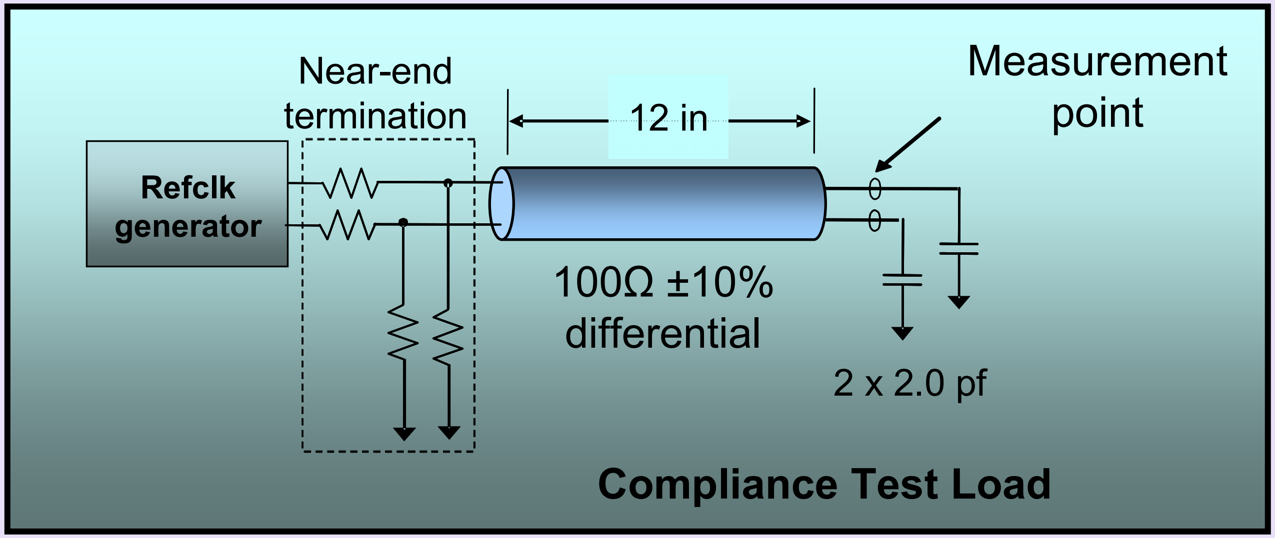


Refclk Spec Subsection

- Reference Clock Electrical parameters
  - ✓ Compliance test load
  - ✓ Refclk Architectures
  - ✓ Post processing steps
  - ✓ Jitter definitions
  - ✓ PLL difference function

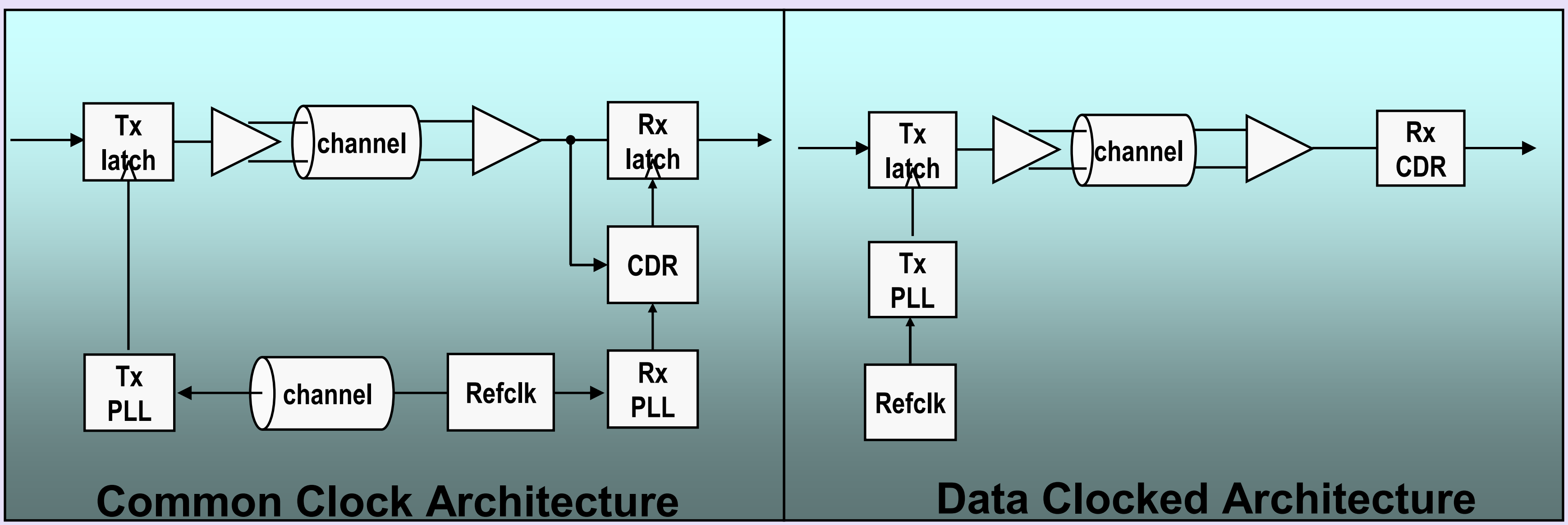
Test Load for Refclk

- The test setup for refclk measurement is the same as the Gen1 CEM specification
  - ✓ Represents worst case signal integrity scenario likely to be encountered in an actual system
  - ✓ Setup assumes near-end termination and high-Z probes

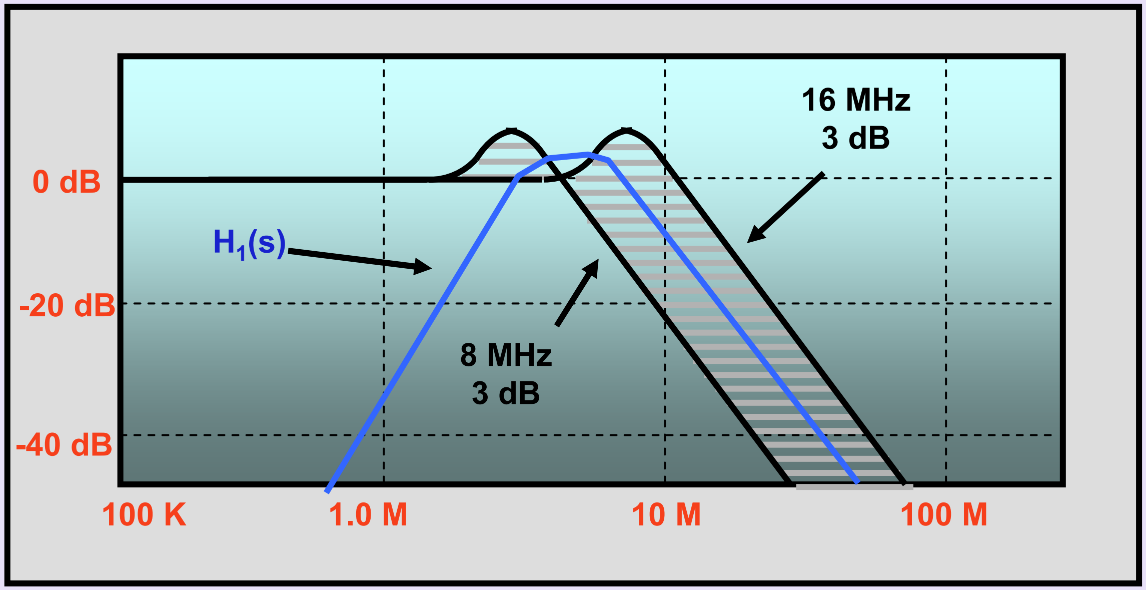


Clock Architectures

- PCIe Base spec defines two distinct Refclk architectures at 5.0 GT/s: common clock and data clocked
  - ✓ At 2.5 GT/s spec does not differentiate between 2 cases, but implicitly supports both
- Jitter margins for the two differ
- Post processing methods differ due to PLL difference function and CDR low freq jitter tracking requirements



PLL Difference Function



PLL difference function is defined as the difference in the areas under the passband curves between the min (8 MHZ, 3 dB) and max (16 MHz, 3 dB) PLL bandwidths. A similar curve may be generated between 5 MHz, 1 dB and 16 MHz, 3 dB curves.

Applicable only for common clock architecture.

Precise description of PLL difference function is given by following formula and includes both BW/peaking as well as the transport delay difference

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_D} - \frac{2s\zeta_2\omega_{n1} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right]$$

$$\textit{where} \quad T_D = 12\ ns\ (\max)$$

f_{3dB} (MHz)	Peaking	$\omega_{natural}$ (rad/sec)	ζ (damping factor)
ω_2 16.0 (f_{MAX})	3 dB	8.61e6*2π	0.54
ω_1 8.0 (f_{MIN2})	3 dB	4.3e6*2π	0.54
ω_1 5.0 (f_{MIN1})	1 dB	1.82e6*2π	1.16

Refclk Post Processing for 5.0 GT/s

- Post processing removes jitter components that are measurement artifacts or otherwise irrelevant
- Above process is clock architecture dependent

	Common Clocked	**Data Clocked**
< 1.5 MHz jitter components	SSC removal PLL difference function 0.01- 1.5 MHZ step BPF	No SSC removal Max PLL BW fcn 0.01 - 1.5 MHz step BPF
> 1.5 MHz jitter components	PLL difference function 1.5 MHz step HPF Edge filtering	Max PLL BW fcn 1.5 MHz step HPF Edge filtering

- SSC removal: Done in frequency domain by removal of spurs at $N*f_{SSC}$ Requires FFT and IFFT operations on time domain data
- PLL Diff fcn: Already covered
- Edge filtering: Smoothing function to reduce effects of sampling aperture inaccuracy
- Step filter: Separates jitter into <1.5 MHz and ≥1.5 MHz bins

Refclk Jitter Budget

Jitter budget for Common Clock Architecture

	Rj	Dj	Comments
Transmitter	1.4 ps RMS	30 ps	
Channel	0 ps	58.1 ps	Channel introduces no Rj
Refclk	3.1 ps RMS	0 ps	Refclk jitter is ~100% Rj
Receiver	1.4 ps RMS	60 ps	
Total	51.8 ps @ 10^{-12}	148.1 ps	Tj = Dj + Rj = 199 ps

Jitter budget for Data Clocked Architecture

	Rj	Dj	Comments
Transmitter	1.4 ps RMS	30 ps	
Channel	0 ps	58.1 ps	Channel introduces no Rj
Refclk	4.0 ps RMS	0 ps	Refclk jitter is ~100% Rj
Receiver	1.4 ps RMS	48 ps	
Total	62.9 ps @ 10^{-12}	136.1 ps	Tj = Dj + Rj = 199 ps

$$Rj = 2Q_{BER}\sum\sqrt{Rj^2}$$

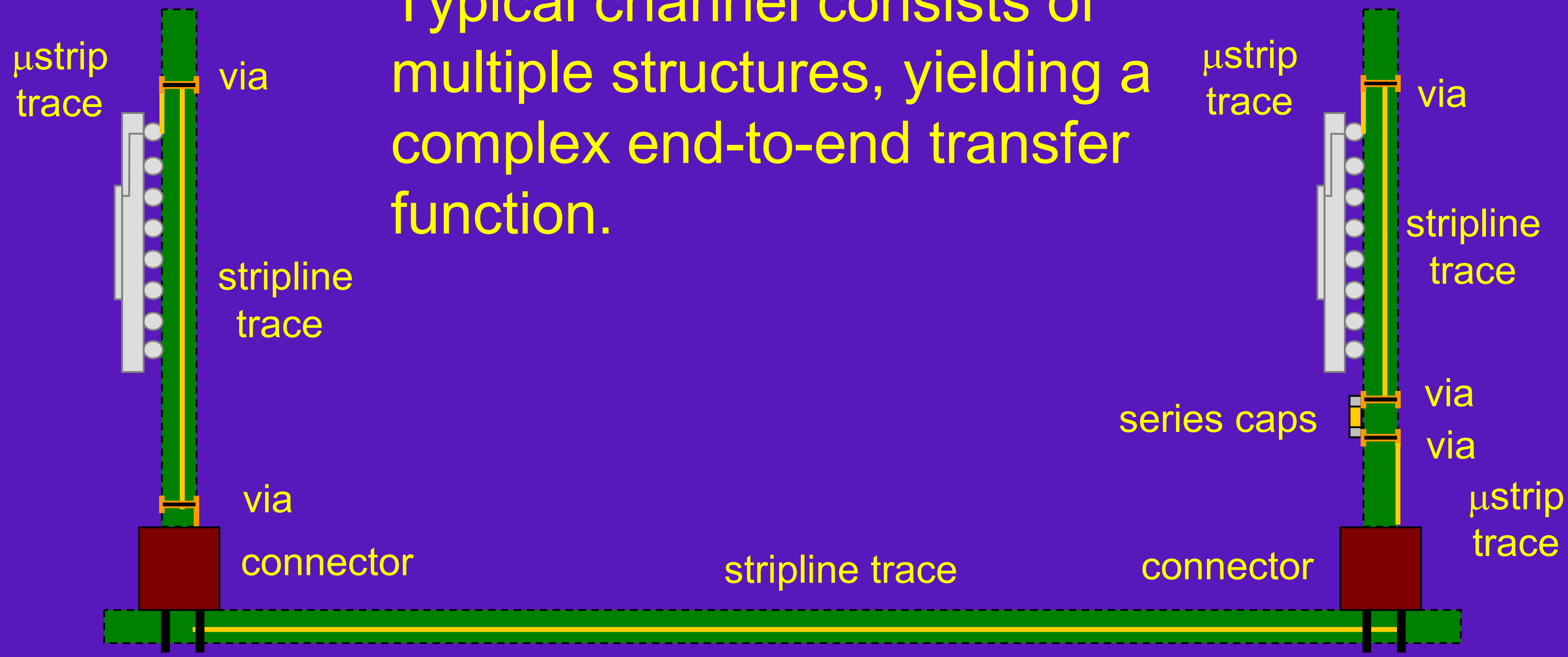
$$Q_{BER} = 7.03 \ at \ 10^{-12}$$

Gen2 Channel Spec Subsection

- PCI-e Gen2 Channel Specification
  - ✓ Characterizing the channel
  - ✓ s-parameter review
  - ✓ Extracted channel approach
  - ✓ Selecting worst case Tx sim parameters
  - ✓ Accounting for non-simulated jitter effects

Characterizing the Channel

Typical channel consists of multiple structures, yielding a complex end-to-end transfer function.

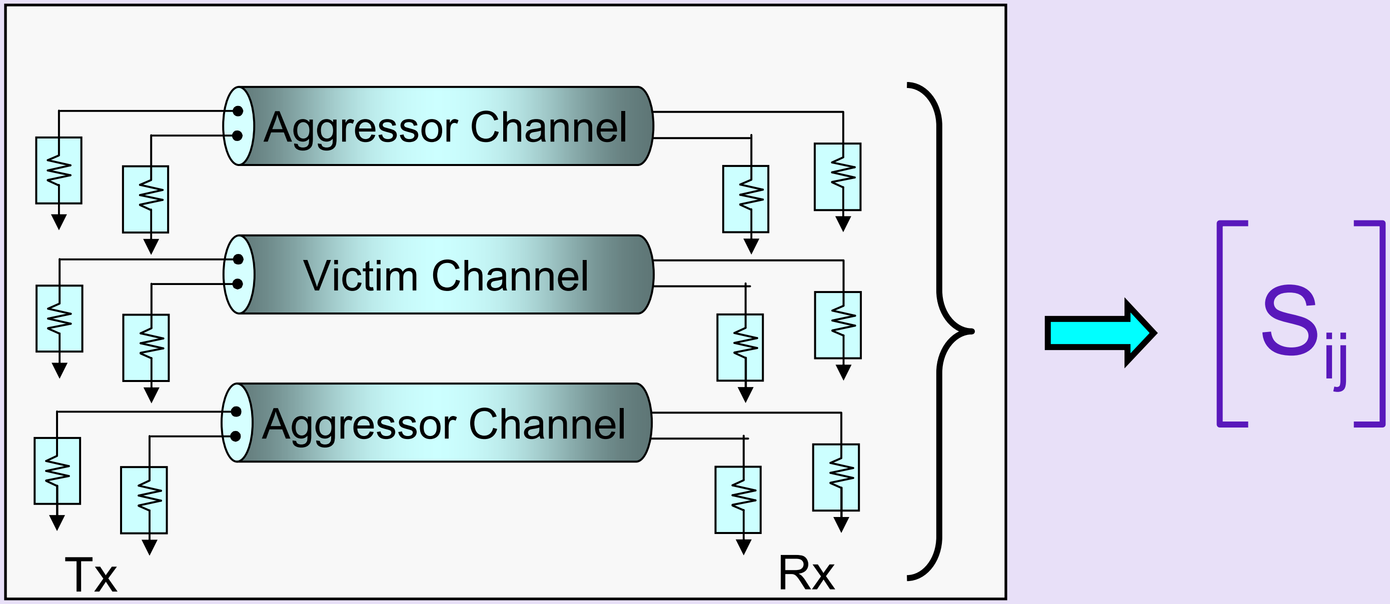


- Key channel effects:
  - Dielectric and conductor loss
  - Impedance discontinuities
  - Crosstalk
  - Mode conversion effects

s-parameters capture all of these

Channel "Black Box" Equivalent

- Channel may be reduced to a "black box" s-parameter equivalent.
- All phenomena affecting channel performance are captured
  - ✓ Dielectric and conductor loss, internal impedance mismatch
  - ✓ Tx/channel mismatch
  - ✓ Rx/channel mismatch
  - ✓ Forward and reverse crosstalk
  - ✓ Mode conversion

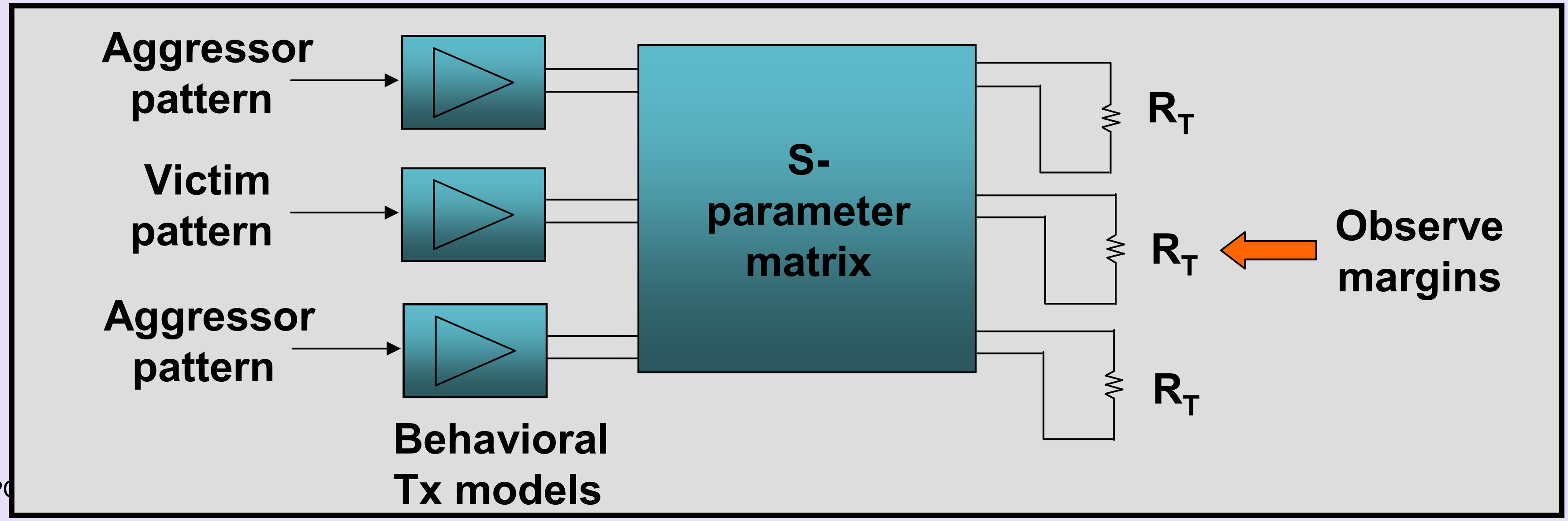


Extracted Channel Approach

- A channel's measured s-parameters provide a complete electrical description, but:
- Direct correlation between s-params, Rx eye margins not feasible.
- Use a so called <u>Extracted Channel Approach</u>
  - ✓ Measured channel s-parameters imported into sim environment
  - ✓ Tx model and Rx reference load are added
  - ✓ Margins seen at ref load compared against Rx spec parameters
- Advantages of method
  - ✓ Approach is mathematically rigorous
  - ✓ Minimizes guardbanding
  - ✓ Captures worst case interactions between Tx and channel
  - ✓ Allows comparison of results against Rx eye margins

End to End Simulation Model

- Tx characteristics included in simulation
  - $V_{TX\text{-}SWING}$, $V_{TX\text{-}DE\text{-}RATIO}$, $T_{MIN\text{-}PULSE}$ $T_{TX\text{-}RISE\text{-}FALL}$, $T_{RF\text{-}MISMATCH}$
  - $T_{RL\text{-}TX\text{-}DIFF}$, Aggr-Victim skew
- Typically a DOE is run to identify worst case combination of Tx parameters
- Measurement into reference load (R_T) eliminates any channel/Rx interactions

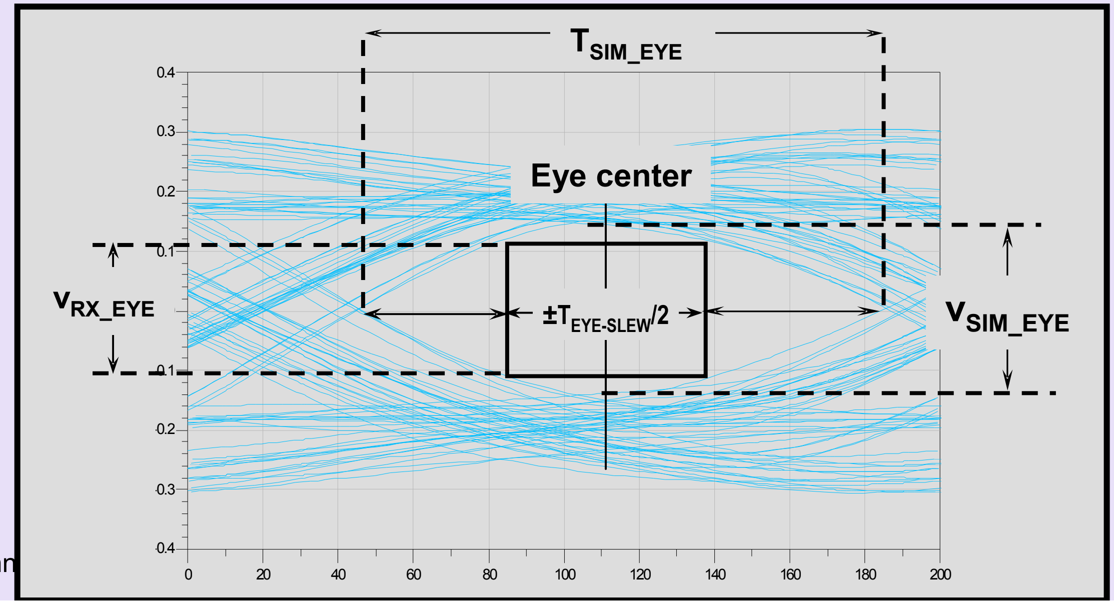


Identifying W/C Tx Parameter Values

- Most Tx parameters can be fixed via inspection
  - ✓ VTX-SWING (min), VTX-SWING-LOW (min), TMIN-PULSE (min), TRF-MISMATCH (max)
- Some parameters will need to be swept
  - ✓ VTX-DE-RATIO: (min and max)
  - ✓ TTX-RISE-FALL, (min and max)
  - ✓ RLTX-DIFF: (max CTX, min and max RTX)
- Aggressor, victim data patterns
  - ✓ Must be 8b/10b compliant
- Some Tx parameters need not be simulated
  - ✓ Example: low frequency Dj and Rj

Accounting for Non-Simulated Jitter

- Determining channel induced jitter is straightforward
  - Tx simulates a worst case 20ps of duty cycle distortion jitter: $T_{TX\text{-}MIN\_PULSE}$
  - Channel may introduce a maximum of 58.1 ps additional jitter
  - $T_{CH\text{-}SIM\text{-}EYE} \geq 200 - 58.1 - 20 = 121.9$ ps
- Correlating channel-induced voltage requires slewing eye by sum of all non-simulated Tx and Refclk jitter terms and measuring resulting voltage
  - ± 28.9 ps slew for common clock architecture to meet 120 mV $V_{RX\text{-}DIFF\text{-}PP\text{-}CC}$
  - ± 34.7 ps slew for data clocked architecture to meet 100 mV $V_{RX\text{-}DIFF\text{-}PP\text{-}DC}$



Gen2 Rx Spec Subsection

- PCI-e Gen2 Receiver Specification
  - ✓Tolerancing methodology
  - ✓Key AC parameters
  - ✓Calibration channel
  - ✓Calibrating test setup
  - ✓Interpreting results

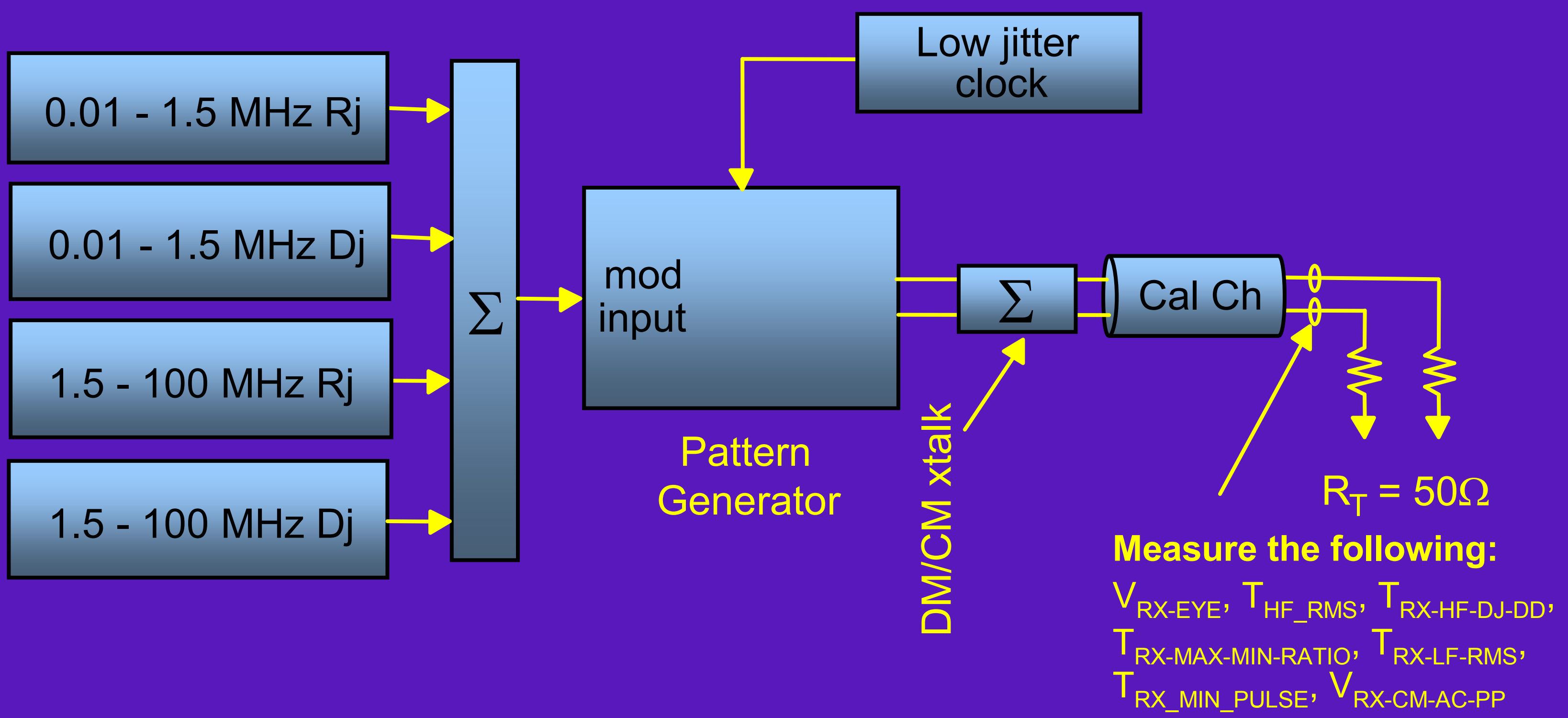
Characterizing the Receiver

- Advantages of a Tolerancing-based Rx spec
  - ✓Minimizes guardbanding
  - ✓Only output an Rx can provide is BER as function of inputs
  - ✓Proven in other high speed Comm interfaces
- Procedure
  - ✓Build test setup capable of injecting into receiver worst case margins as defined in Rx spec table
  - ✓Calibrate setup into precision reference load
  - ✓Replace reference load with Rx under test and observe BER

Calibration Channel

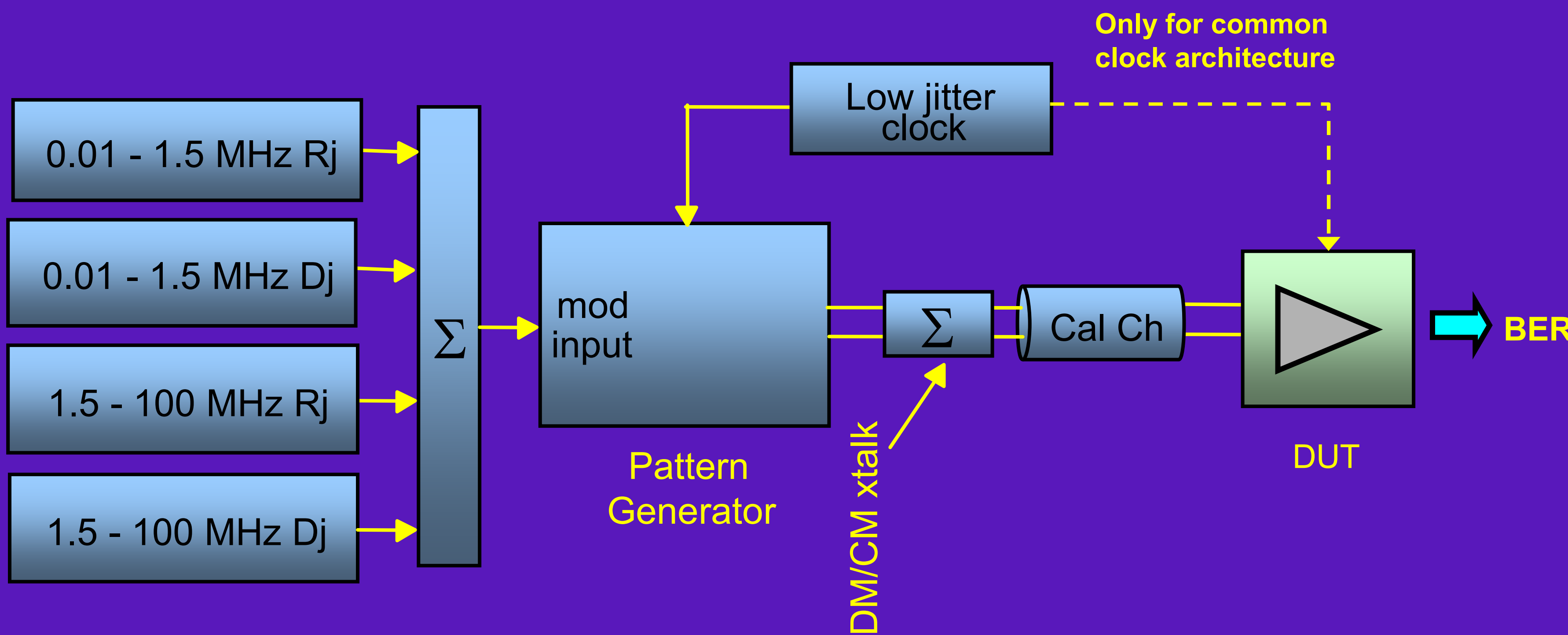
- The purpose of the calibration channel is to generate the maximum ISI that sets max limit for VRX-MIN-MAX-RATIO
  - ✓ Calibration channel is defined to yield 5:1 voltage ratio.
  - ✓ Ratio value empirically determined
  - ✓ Channel length: ≅20" for FR4 material and 5 mil wide traces
  - ✓ Pattern generator may drive a binary output, instead of requiring a de-emphasized output
  - ✓ From receiver's point of view, Tx de-emphasis is irrelevant as long as Rx is driven with simultaneous w/c margins
- Calibration channel characterized in terms of its transient response, and return loss

Calibrating Rx Margining Setup



- Test setup shown represents functionality only, not actual instruments
- Inputs adjusted until parameters at R_T are at minimum values defined in spec

Characterizing Rx to Spec



- Low jitter Refclk obviates need for 2-port measurement
- Direct measurement of 10^{-12} BER is possible in <20 minutes
- Other lanes within same Rx under test need to be driven

PCIe2 Key Design Challenges

- TX Jitter compliance
  - ✓ Requires very low jitter PLL
  - ✓ Requires very low jitter Refclk source
  - ✓ Requires delicate clock network design and layout
  - ✓ Requires very low noise supply
    - Needed to design Power Delivery which would reduce supply noise by more than 30% from Gen1
    - Accurate Power Delivery model which would take into account data dependent noise pattern
- RX Jitter compliance
  - ✓ Requires low latency clock recovery loop
    - Had to reduce loop latency by ~50% from Gen1
  - ✓ Requires very delicate and careful clock distribution design with accurate phase relationship.
  - ✓ Need to pay close attention to Rx input CAP (<1 pF) to avoid jitter penalty.
- Squelch
  - ✓ Difficult to limit threshold variation of the detector and detect both EI entry & Exit

Summary

- Rev 0.9 Base Spec approved by EWG and posted on PCI-SIG website for member review
  - ✓ Content is stable: go ahead and design to it
- Designing 5.0 GT/s compliant is a challenge, but achievable with careful design

For more information please go to www.pcisig.com

PCI Express® 2.0 Electrical Specification Overview

Dan Froelich
Intel Corporation