
PCI
SIG®

PCI Express® 2.0 Electrical specification

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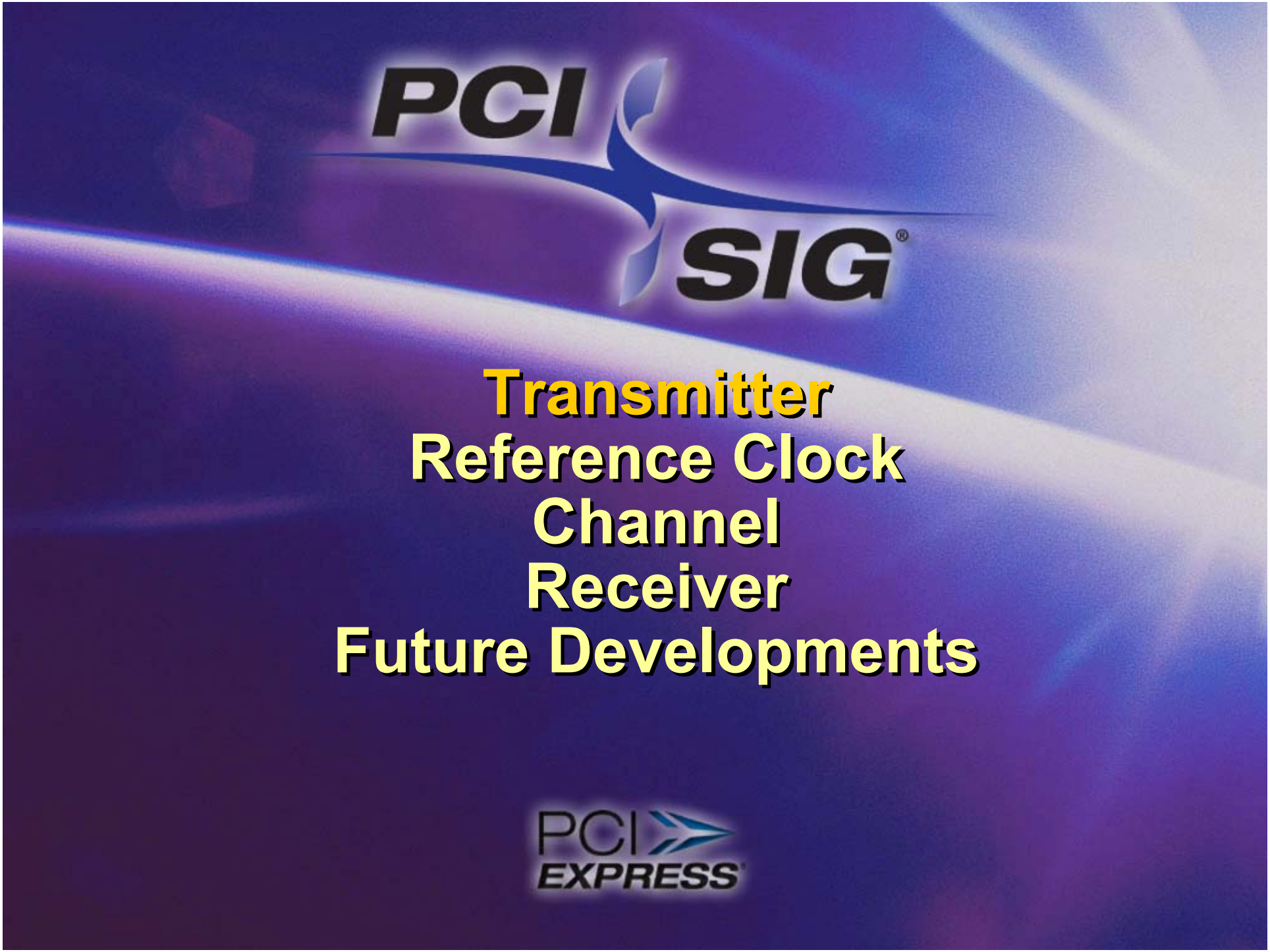
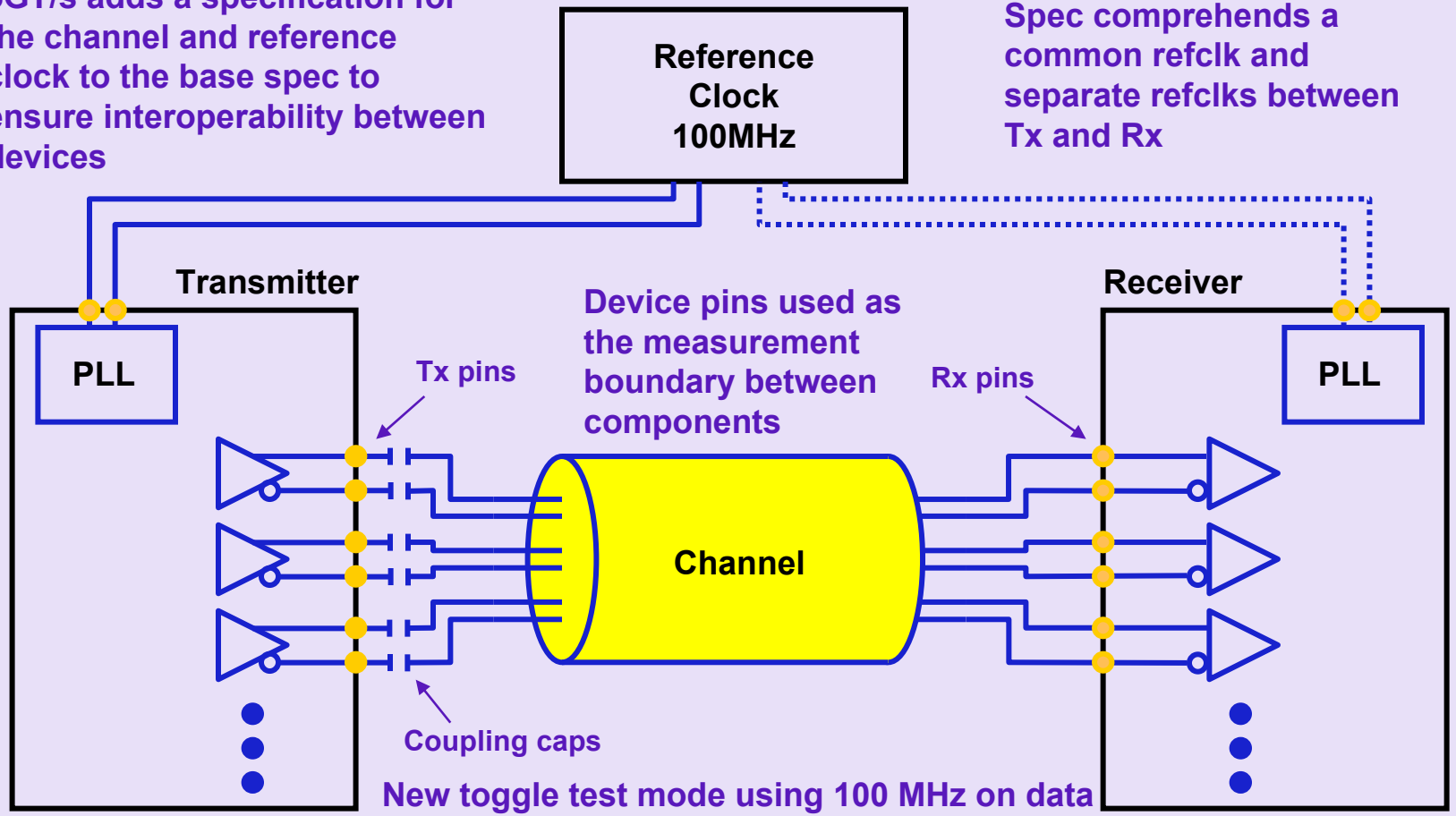
Member of EWG


PCI SIG
Transmitter
Reference Clock
Channel
Receiver
Future Developments
PCI EXPRESS

Physical layer components

5GT/s adds a specification for the channel and reference clock to the base spec to ensure interoperability between devices



New toggle test mode using 100 MHz on data pin(s) to select rate and de-emphasis level for test, but not loop back mode, which must be initiated through training pattern sequence

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5GT/s Transmitter

- Same basic signaling as 2.5GT/s
  - ✓ UI 200ps ±300ppm
  - ✓ $V_{TX-DIFF-PP}$ 800-1200mV diff pk-pk
  - ✓ $V_{TX-DIFF-PP-LOW}$ 400mV (min) diff pk-pk for low power
    - – Was in low-power addendum, now in base spec
- AC coupled at transmitter
  - ✓ C_{TX} 75-200nF
  - ✓ Receiver Detect by measuring coupling cap time constant
  - ✓ $V_{TX-DC-CM}$ 0–3.6v
    - – Only required to bound surge current during hot-plug
- AC common-mode changed to pk-pk
  - ✓ $V_{TX-CM-AC-PP}$ 100mV
    - – Is a RMS measurement in 2.5GT/s
    - – Bounds peak AC common-mode excursions Rx has tolerate

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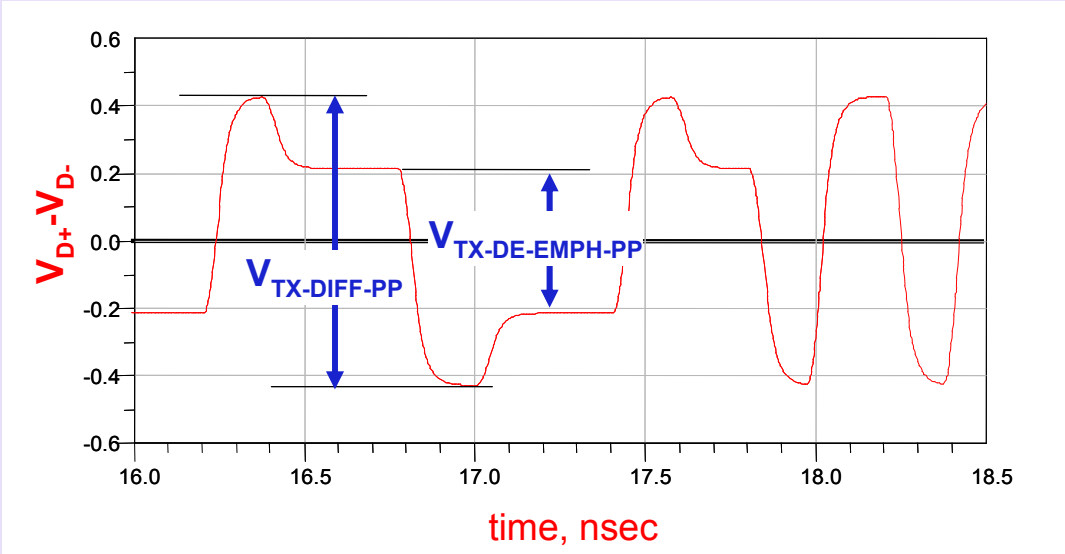
Full swing signaling



- Definitions for transmit de-emphasis same as 2.5GT/s
  - ✓ First transition of logic value at full swing
  - ✓ If logic value constant drop to de-emphasized amplitude
- De-emphasis ratio is specified to be measured on the averaged waveform

  $V_{TX-DE-RATIO} \equiv -20\log_{10}(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$
  - ✓ 5GT/s is -6dB ±0.5dB to compensate for long channels or -3.5dB ±0.5dB
  - ✓ 2.5GT/s is -3.5dB ±0.5dB
- Note: All peak measurements are statistical in nature because of various sources of noise. Minimum sampling size for these measurements is defined as 10^6 UI to improve the repeatability of the measurement.

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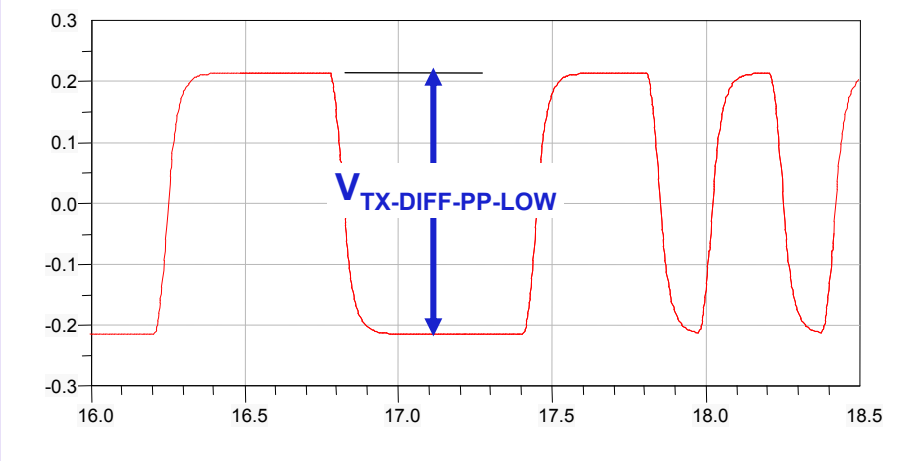
Low swing signaling



- Low swing mode same as 2.5GT/s low power addendum
  - ✓ No de-emphasis
  - ✓ ~50% of full swing amplitude (same as de-emphasis)
- Suitable for short channels were HF loss is minimal
  - ✓ Note only one Rx spec
- All other timing parameters the same as full swing

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Margining

- Tx is required to support signaling at reduced signal amplitude at both 2.5GT/s and 5GT/s
  - ✓ Support for system level margining
  - ✓ Used for system characterization, debug and test
- Voltage margining in the Rx and/or time margining in Tx or Rx is optional
- Two modes of margining are defined
  - ✓ All Tx must implement full swing margining
  - ✓ Tx's that implement half swing must implement half swing margining
- De-emphasis levels must be maintained
  - reduced accuracy allowed of ±1dB across margin levels

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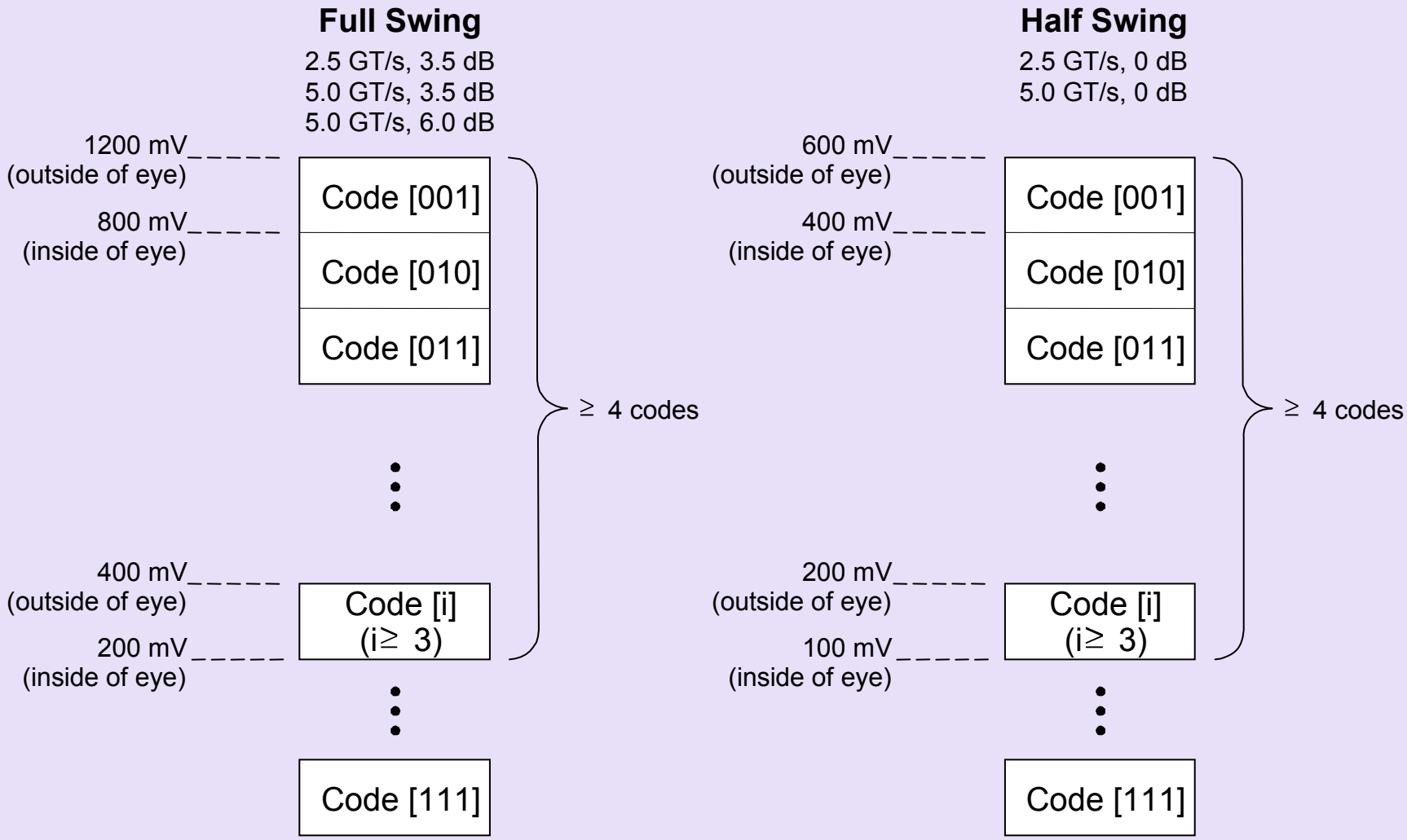
Margin configuration register



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Transmitter timing specifications

- Overall Tx cumulative eye width defined at 10^{-12} BER similar to 2.5GT/s
  - ✓ T_{TX-EYE} 0.75UI
- Additional 5GT/s timing parameters
  - ✓ $T_{TX-DJ-DD}$ 0.15UI
    - Measurement method defined to extrapolate from T_{TX-EYE} jitter distribution
  - ✓ $T_{MIN-PULSE}$ 0.9UI
    - Minimum instantaneous data pulse width measured over 10^6 samples with worse case data pattern with all lanes active
  - ✓ $T_{TX-LF-RMS}$ 3.0ps
    - Transmit LF RMS jitter from 10kHz to 1.5MHz
  - ✓ $T_{TX-RISE-FALL}$ 0.15UI (min)
    - Bounds max HF energy for short reflective channels
    - Max constrained by T_{TX-EYE}
  - ✓ $T_{RF-MISSMATCH}$ 0.1UI
    - Bounds worse case asymmetry (rise and fall time) of transmit waveform

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Transmit timing enhancements

- Key differences from 2.5GT/s to improve accuracy:
  - ✓ Total jitter and a deterministic jitter measurement defined
    - Allows a minimum RJ estimate to be assumed which can be RSS with other RJ sources in timing budget
  - ✓ Minimum transmit pulse width defined
    - Required by channel compliance to bound maximum pulse compression by the channel
  - ✓ Effects of de-emphasis on eye width measurements compensated in measurement methodology
    - Avoids conservative Tx eye closure penalty
  - ✓ Low and high frequency jitter on recovered clock separated and measured
    - Avoids Tx eye closure from LF jitter that will be mostly tracked by Rx
    - LF jitter applied to Rx during compliance testing

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Jitter model

- 5GT/s uses a Dual Dirac jitter model to calculate total system jitter:

$$System\ T_J \equiv \sum DJ_{DD} + 2Q_{BER}\sqrt{\sum RJ_{DD}{}^2} \leq 1.0UI$$

  - ✓ Summation of all DJ sources plus RSS of all RJ sources
  - ✓ Q_{BER} is 7.03, the scaling factor of the RSS of the RMS jitter in the system for a BER of 10^{-12}
- To avoid confusion about the various definitions of DJ, 5GT/s defines a method for DJ_{DD} extrapolation from the jitter distribution
  - ✓ Note DJ_{DD} is a model parameter that simplifies the separation of RJ_{DD} from a jitter distribution that contains significantly less than 10^{12} samples

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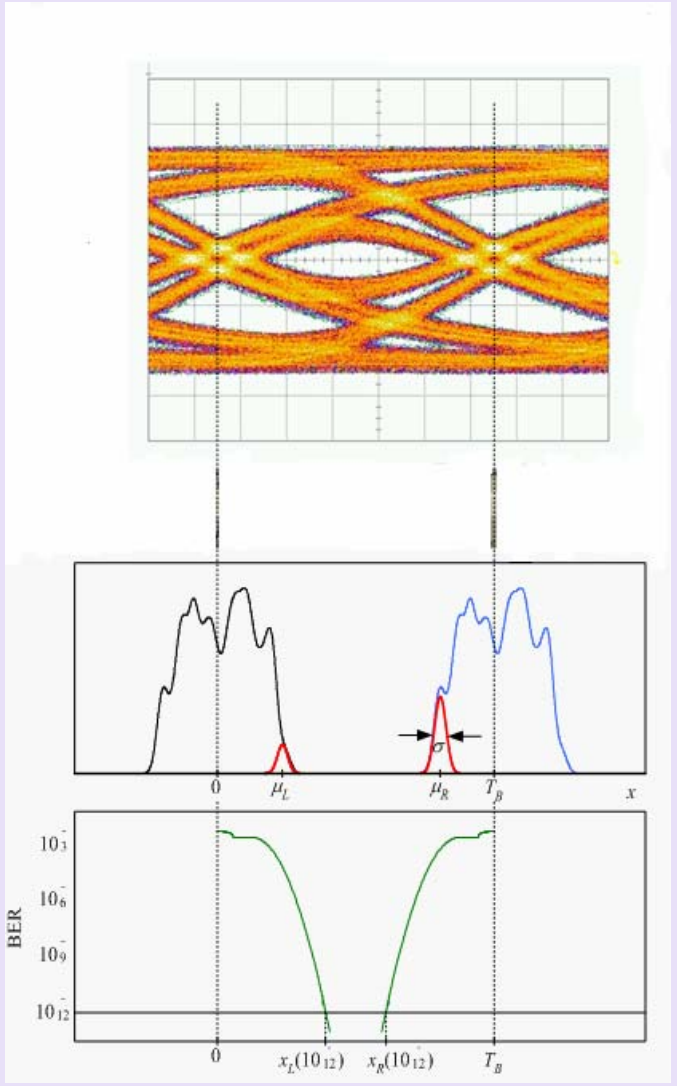
Tx Eye

- Eye diagram measurement of a transmitter
  - ✓ This can be generated from many different instruments
- The PDF of left and right tail might be plotted and a Gaussian distribution fitted to the tails
  - ✓ Many algorithms exist for tail fit yielding different results depending on spectral content and sample size of jitter.
- The CDF is either directly measured or calculated from the PDF, with the tails extrapolated to the BER limit of 10^{-12}
  - ✓ Larger sample sizes tend to provide measurements with most consistent T_J estimates.



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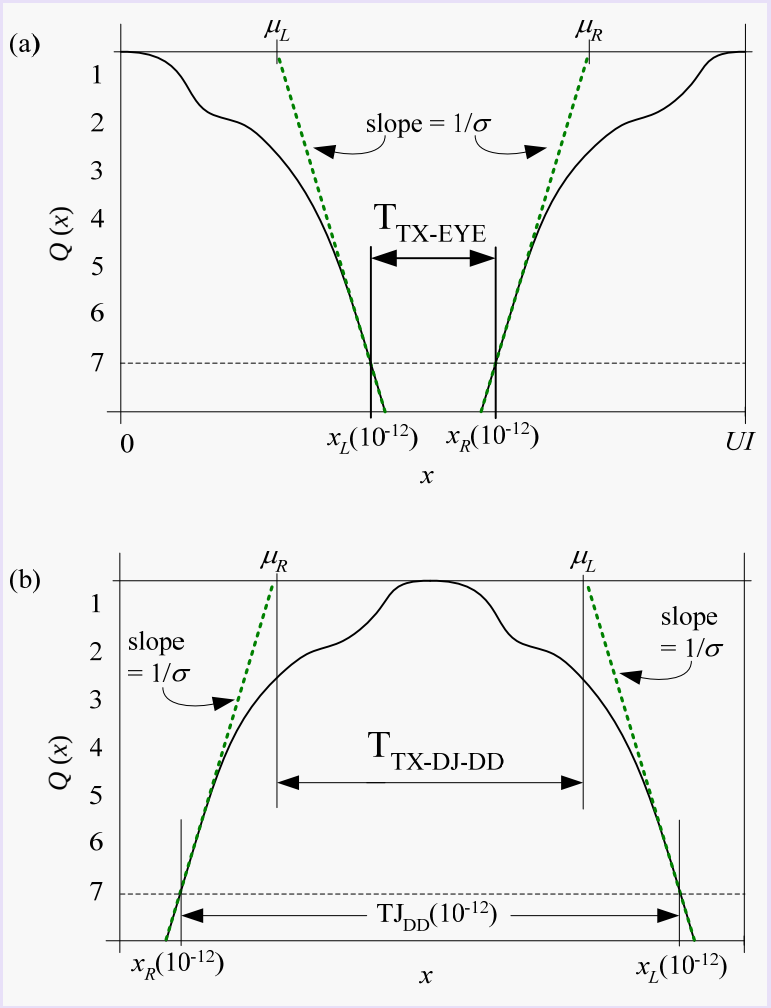
5GT/s jitter methodology

- The CDF obtained from measurement is transformed onto a Q axis
  - ✓ Q is the inverse normal CDF
  - ✓ Makes any Gaussian jitter linear on this scale where units of Q represent sigmas of the Gaussian distribution
- A linear fit is done in the tail regions of the distribution
  - ✓ Sample size has to be sufficient for the distribution to have become linear
  - ✓ Sample size required will vary depending on device, typically in the range of 10^6-10^{10}
- The straight line of slope 1/sigma is then extrapolated up to Q=0 and down to Q=7.03
  - ✓ Intersection with Q=0 is DJ_{DD}
    - Used for $T_{TX\text{-}DJ\text{-}DD}$
  - ✓ Intersection with Q=7.03 is TJ_{DD}
    - Used for UI-$T_{TX\text{-}EYE}$



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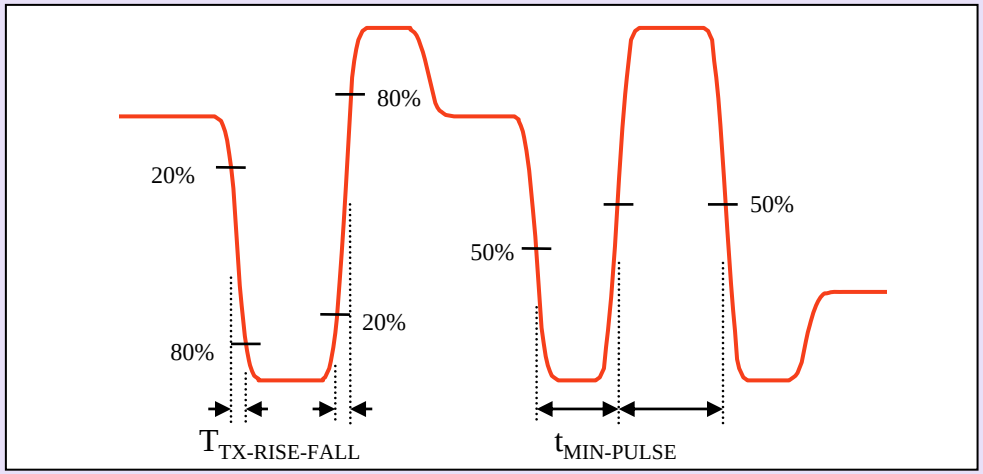
Tx transitions and pulse width

- De-emphasis complicates timing measurements as voltage swing is variable
  - ✓ Need to make measurements as if they were convolved with the inverse of the Tx equalization
- General rule is to measure based on magnitude of transition
  - ✓ Use 20-80% for rise fall time, 50% for pulse width
- Measurement levels should be based on what the driver is generating rather than the nominal levels



Note pulse width levels are not the same if de-emphasized swing

Pulse width measurement allows worse case channel induced pulse compression to be modeled

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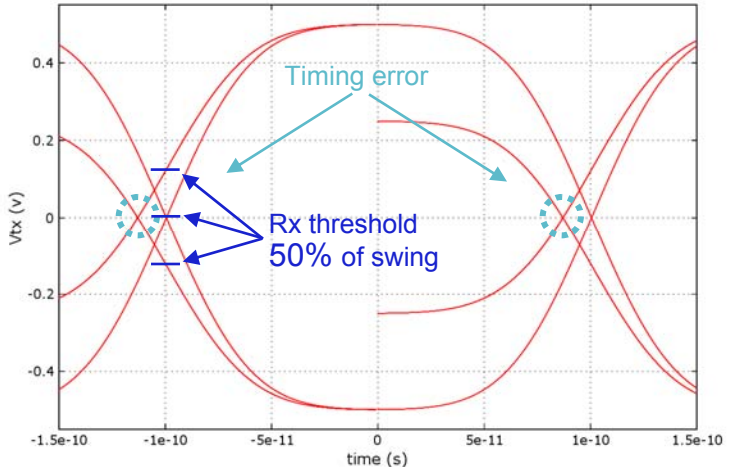
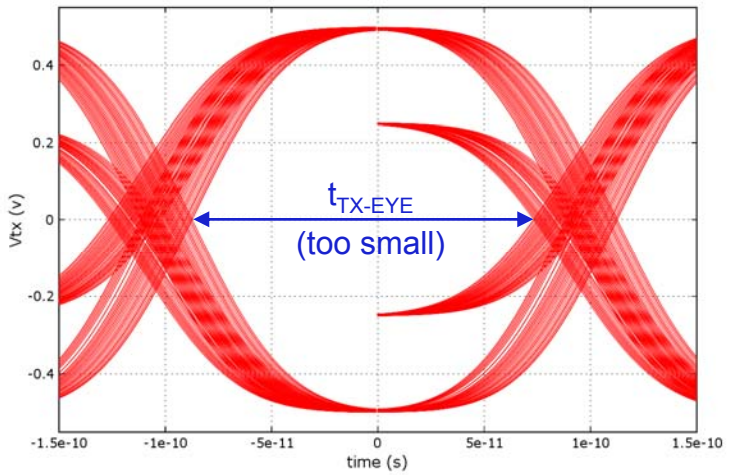
Jitter from de-emphasis

- 2.5GT/s has -3.5dB of de-emphasis and more margin so this effect was ignored
  - ✓ 5GT/s has -6dB de-emphasis and budgets are very tight
- De-emphasis causes a timing error in cumulative eye measurement
  - ✓ Closes the eye on right side
  - ✓ Overestimates eye opening on left side
  - ✓ 10-17ps error
- Channel effectively removes the de-emphasis jitter
  - ✓ Tx approximates the inverse of the HF loss of the channel
  - ✓ 0v crossing time seen by Rx is 50% of the swing





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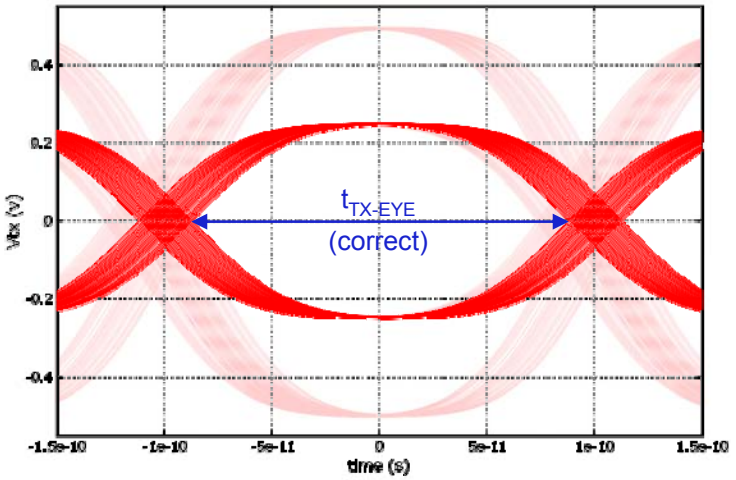
Compensation for de-emphasis

- Timing error can be removed by applying a form of measurement DFE
  - ✓ Waveform is voltage scaled and offset based on current and previous logical values
  - ✓ Scaling exactly match a Tx with -6dB de-emphasis
- Actual measurement data needs to be averaged to increase the effective sampling rate and remove noise floor of measurement equipment
  - ✓ If based on averaged "clear" eye measurement then jitter needs to be added back in and measurement jitter may be removed by RSS



IF fullswing :

$$scale = deemp; \quad offset = 0.0$$

ELSEIF previousBit $== 1$:

$$scale = \frac{2 \cdot deemp}{1 + deemp}; \quad offset = \frac{1 - scale}{4}$$

ELSE :

$$scale = \frac{2 \cdot deemp}{1 + deemp}; \quad offset = -\frac{1 - scale}{4}$$

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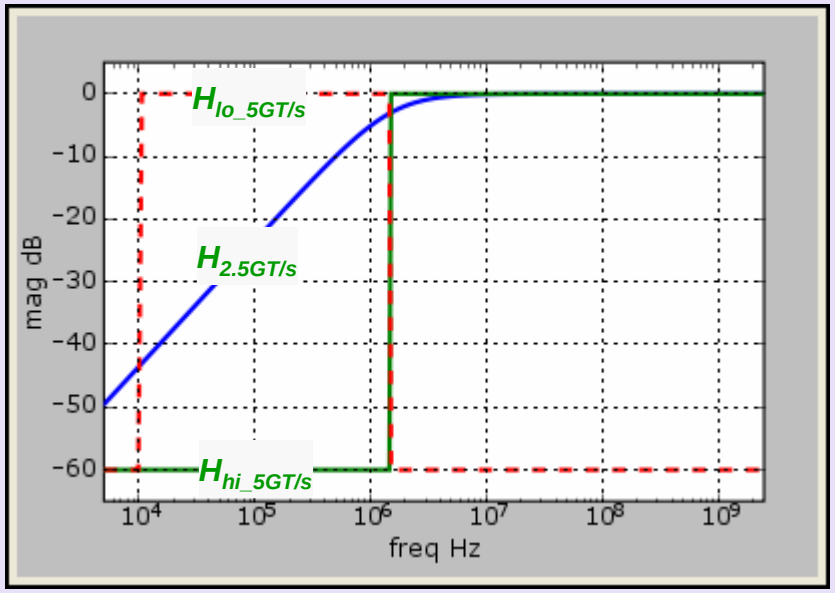
Tx jitter filtering

- Tx jitter measurement requires a clock recovery function
  - ✓ Jitter on this recovered clock contributes to eye closure
- Tx under test is driven by an "ideal" very low jitter reference clock
- Different Tx filters applied for 2.5 vs. 5.0 GT/s
  - ✓ 2.5GT/s utilizes a 1-pole HPF with fc of 1.5 MHz
  - ✓ 5.0GT/s uses 2 filters
    - 10kHz to 1.5MHz brick wall BPF
    - 1.5MHz brick wall HPF
- To avoid increasing the observed Tx jitter, recovered clock jitter is measured in above bands
  - ✓ HF jitter is not tracked by Rx and so reduces Tx eye width
  - ✓ LF jitter mostly tracked by Rx and accounted for as part of Rx testing
  - ✓ Jitter below 10kHz is considered wander/drift and tracked by Rx



$$H_{2.5GT/s} = \frac{s}{s + w_c} \qquad w_c = 2\pi f_T$$

$$H_{hi\_5GT/s} = if\,(f >= f_T)\,then\,1.0\,else\,10^{-3}$$

$$H_{lo\_5GT/s} = if\,(f < f_{10kHz})\,then\,10^{-3}$$
$$elseif\ (f < f_T)\,then\,1.0$$
$$else\,10^{-3}$$

$$f_T = 1.5MHz$$

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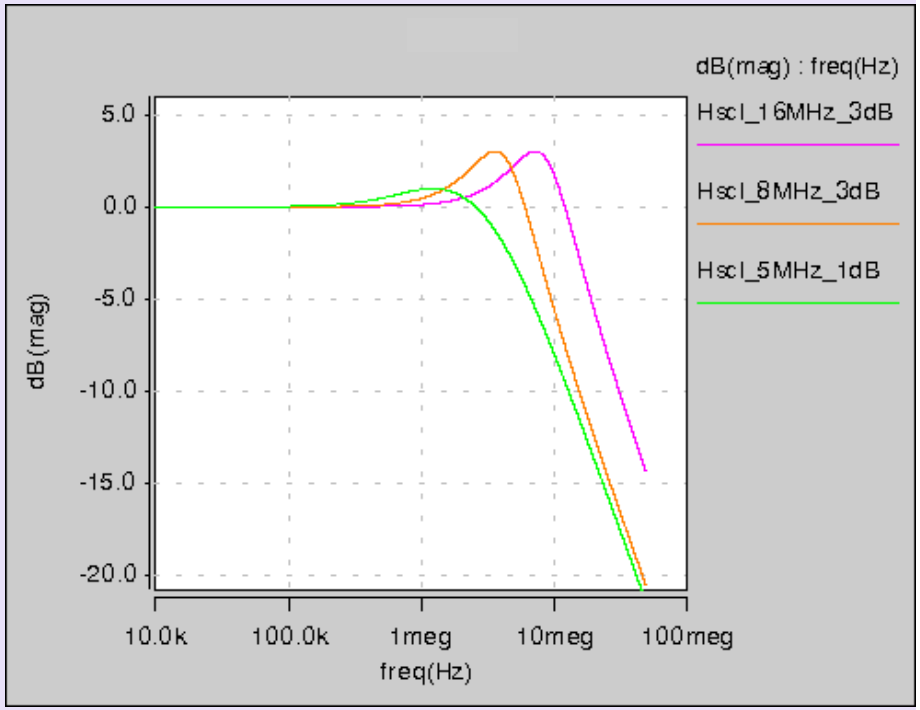
Transmit PLL requirements

Range of PLL bandwidths and jitter peaking are allowed

- 2.5GT/s had sufficient margin to allow very wide PLL bandwidth range:
  - ✓ 1.5 MHz to 22 MHz with up to 3 dB peaking.
- 5GT/s requires Tx PLL bandwidth and jitter peaking to be more tightly controlled
  - ✓ $BW_{TX\text{-}PLL}$ 16MHz (max)
  - ✓ $BW_{TX\text{-}PLL\text{-}LO\text{-}3dB}$ 8MHz (min)
  - ✓ $BW_{TX\text{-}PLL\text{-}LO\text{-}1dB}$ 5MHz (min)
- That is: 5 to 8 MHz with up to 1 dB peaking or 8 to 16 MHz with up to 3 dB



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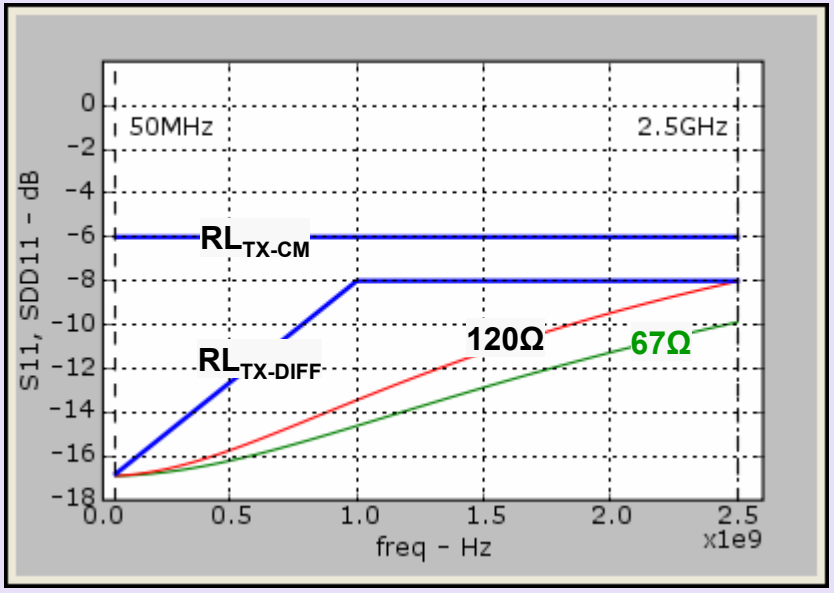
Transmit Return Loss

- 2.5GT/s constant return loss of 10dB 50MHz-1.25GHz
  - ✓ specified DC impedance ~100Ω and
- 5GT/s uses frequency dependent S-parameter mask 50MHz-2.5GHz
  - ✓ SDD11 - 16.8dB @50MHz 8dB @2.5GHz, normalized to 90Ω
  - ✓ S11 - 6dB, normalized to 45Ω
  - ✓ Measured with VNA or equivalent method whilst driving logic 1 and 0
  - ✓ No DC value required as not seen by Rx and would require an additional measurement
- Mask encompasses Rx equivalent circuit
  - ✓ Diff term 67.5Ω-120Ω with 1pF to ground on each leg



$$RL = 20\log_{10}\left(\left|\frac{Z_{TX} + Z_O}{Z_{TX} - Z_O}\right|\right)$$

Note: Return loss is the reciprocal of SDD11 or S11, in dB this means $RL=(SDD11)^{-1} \mid (S11)^{-1}$

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PCI
SIG
PCIe® 2.0 Reference Clock:
Specifications
Test Load
Clocking Modes
PLL Difference Function
SSC and RMS Jitter Separation
Measurement Noise
PCI
EXPRESS

Reference clock (refclk)

- Based on low cost reference clock using ~14MHz crystal
  - ✓ The requirement for the synthesizer to generate multiple system frequencies and use low cost crystals are contributors to their relatively high phase noise
  - ✓ 5GT/s relies on improved versions of the clock generators to lower their jitter contribution to the timing budget
- The JWG has developed a methodology for including refclk jitter into the overall link timing budget
- As the reference clock jitter is a significant contributor to the timing budget, 5GT/s now adds the reference clock into the Base Specification
  - ✓ Previously specified in the CEM Specification
  - ✓ 5GT/s specifies requirements for the clock signal at input pins of PCIe® device based on latest CEM specification

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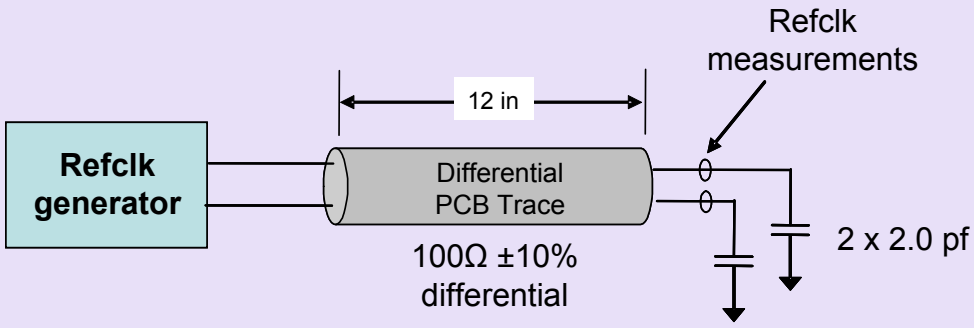
Test load for refclk

- The base spec test load for refclk measurement is the same as 2.5GT/s CEM specification
  - ✓ Provides consistent measurement method between 2.5 and 5.0GT/s
- It is anticipated that some form factors may require different refclk termination schemes
  - ✓ Such as on-die termination, voltage mode drivers for clock generators
  - ✓ Therefore no voltage signaling levels in base spec
  - ✓ These will be covered in appropriate form factor specifications



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Clocking modes

- 5GT/s supports the same clocking modes as 2.5GT/s
  - ✓ Common Reference Clock Rx architecture
    - Tx and Rx both use the same 100MHz clock
    - SSC allowed
  - ✓ Data Clocked Rx architecture
    - Rx does not use common-clock once locked
    - Both Tx must use common-clock
    - SSC allowed
  - ✓ Separate Reference Clock Rx architecture
    - Tx and Rx have different clock each with ±300ppm frequency tolerance
    - No SSC
- Most commonly used mode for 2.5GT/s is Common Refclk Rx
  - ✓ Anticipate the same for 5GT/s
  - ✓ Refclk jitter analysis mostly focused on common-clock
  - ✓ 2.0 Specification includes additional parameters to ensure interoperability between Common, Data Clocked and Separate Refclk

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Refclk Jitter measurement

- Reference clock jitter is measured after applying a PLL-difference function to account for tracking between Tx and Rx PLLs
  - ✓ Tx and Rx PLL bandwidths and peaking are more tightly controlled
- Transport delay is clarified
  - ✓ Budget allocated for worst case internal delay skews
  - ✓ Plan to add a delay spec for cable applications
- Rx CDR transfer function no longer assumed
  - ✓ As 5GT/s has a Rx jitter tolerance test CDR LF tracking can be measured
    - – Ensures non-linear tracking or peaking of bang-bang phase detectors and digital control loops taken into account in compliance testing
  - ✓ Difference function SSC is applied during Rx jitter tolerance test
  - ✓ Allows a broader range of CDR implementations
- New measurement methodology
  - ✓ SSC and RMS jitter separation
  - ✓ Validate maximum phase noise floor of measurement equipment

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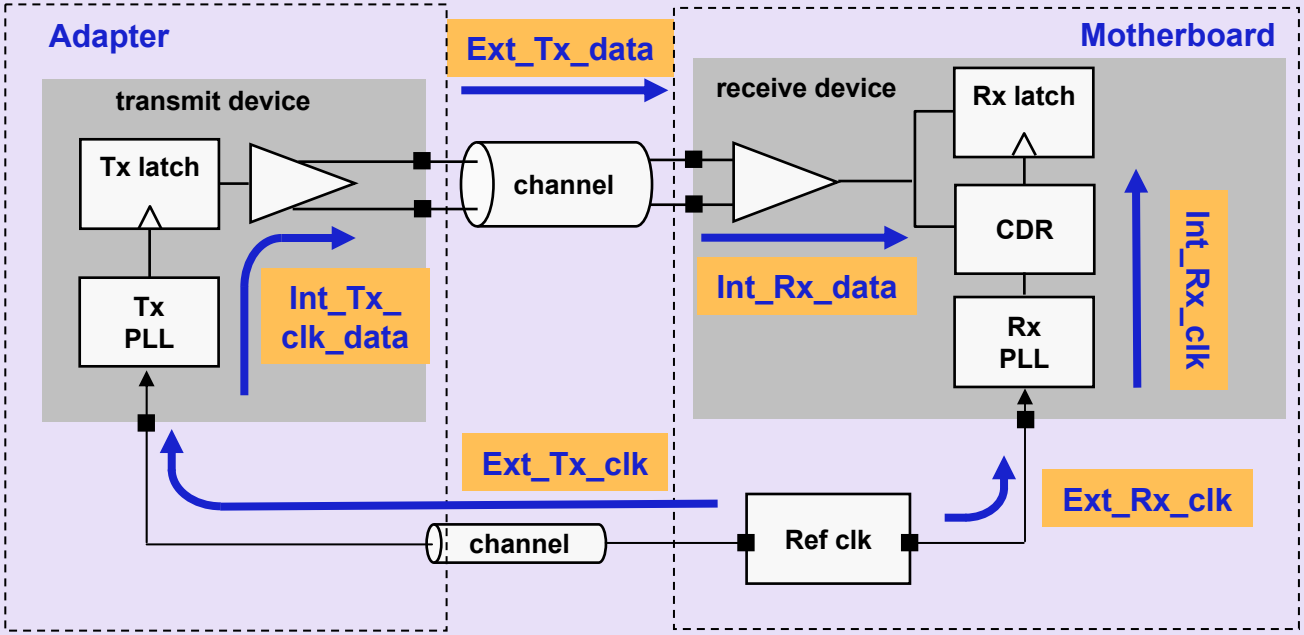
Transport delays clarified



Ext_delay	= Ext_Tx_data + Ext_Tx_clk – Ext_Rx_clk	≤10.0 ns (PCIe 1.x)
Tx_int_delay	= Int_Tx_clk_data	≤2.0 ns (PCIe 2.0)
Rx_int_delay	= Int_Rx_clk – Int_Rx_data	≤2.0 ns (PCIe 2.0)
Total delay	= Ext_delay + Tx_int_delay – Rx_int_delay	≤12.0 ns

PCIe 2.0 clarifies transport delay at device pins is max of 10ns
Also defines a maximum internal transport delay max of 2ns
Means PLL difference function must use worst case 12ns

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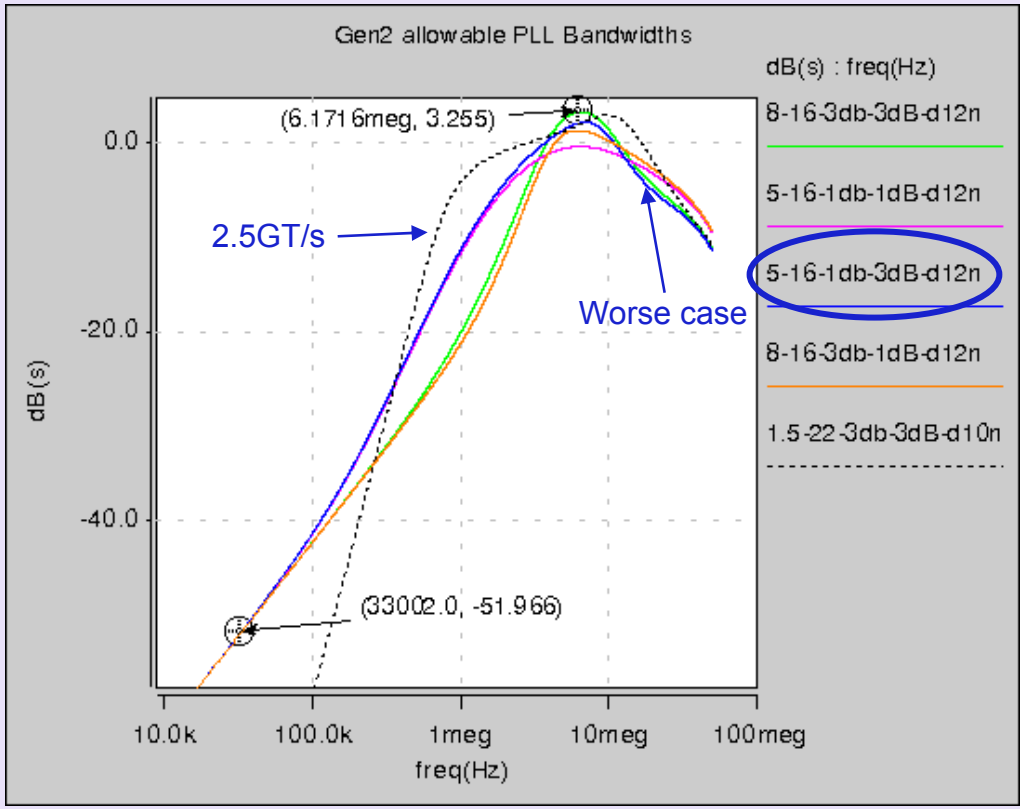
PLL difference function

$$H_1(s)=\left[\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}e^{-sT_D}-\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}\right]$$

where $T_D=12ns$

f_{3dB} (MHz)	Peaking	$\omega_{natural}$ (rad/sec)	ζ (damping factor)
ω_2 16.0 (f_{MAX})	3 dB	8.61e6*2π	0.54
ω_1 8.0 (f_{MIN2})	3 dB	4.3e6*2π	0.54
ω_1 5.0 (f_{MIN1})	1 dB	1.82e6*2π	1.16

$$2\pi\cdot f_{3dB}=\omega_n\sqrt{1+2\zeta^2+\sqrt{(1+2\zeta^2)^2+1}}$$



Simulations on clock traces show worse case to be the wide pass-band of 5MHz 1dB with 16MHz 3dB ~0.4ps RMS penalty also note with no CDR high pass we only have -52dB of SSC rejection

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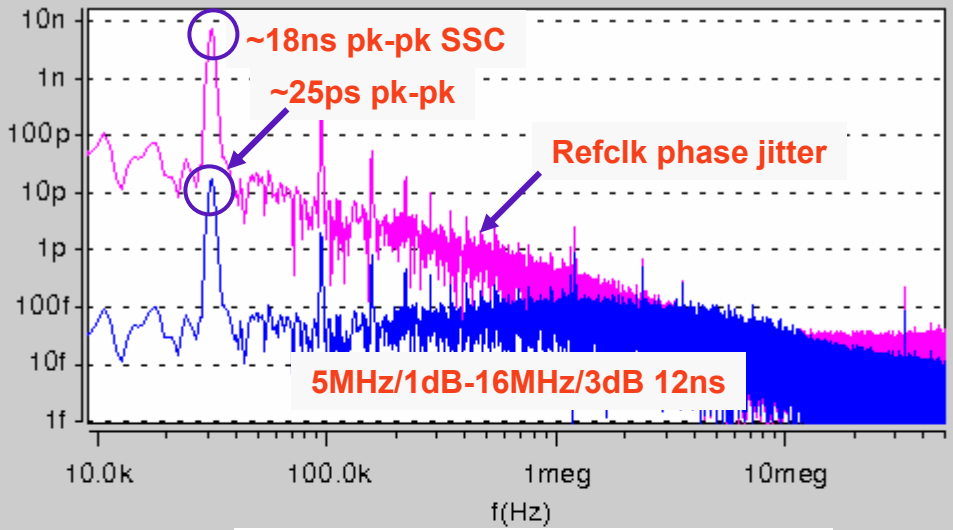
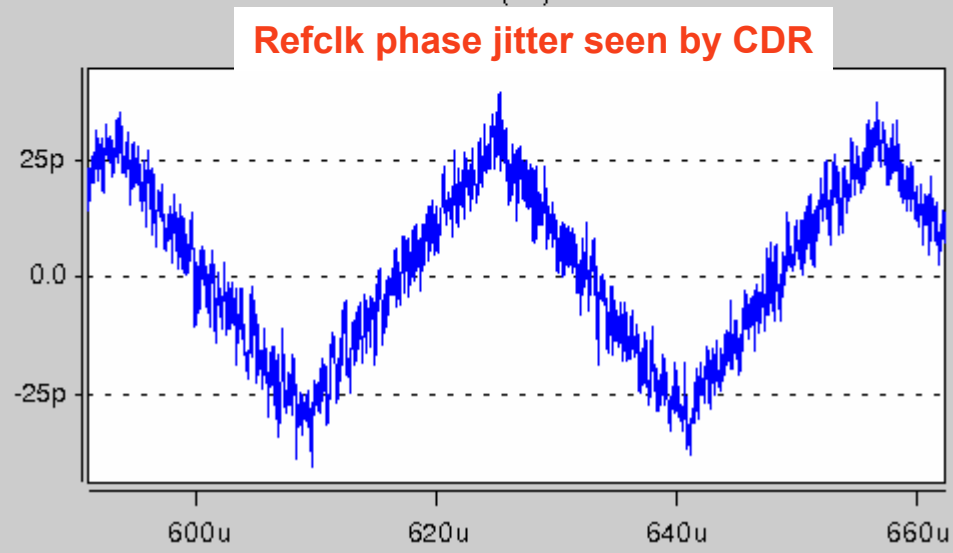
Refclk Phase jitter





- New PLL-difference function reveals phase jitter seen by the CDR
- Rx designers need to consider this refclk jitter in conjunction with HF channel jitter when designing CDR loop
  - ✓ LF tracking can be impaired by HF jitter
- Refclk needs to be measured to bound the magnitude of the SSC triangular waveform and the jitter on top of this

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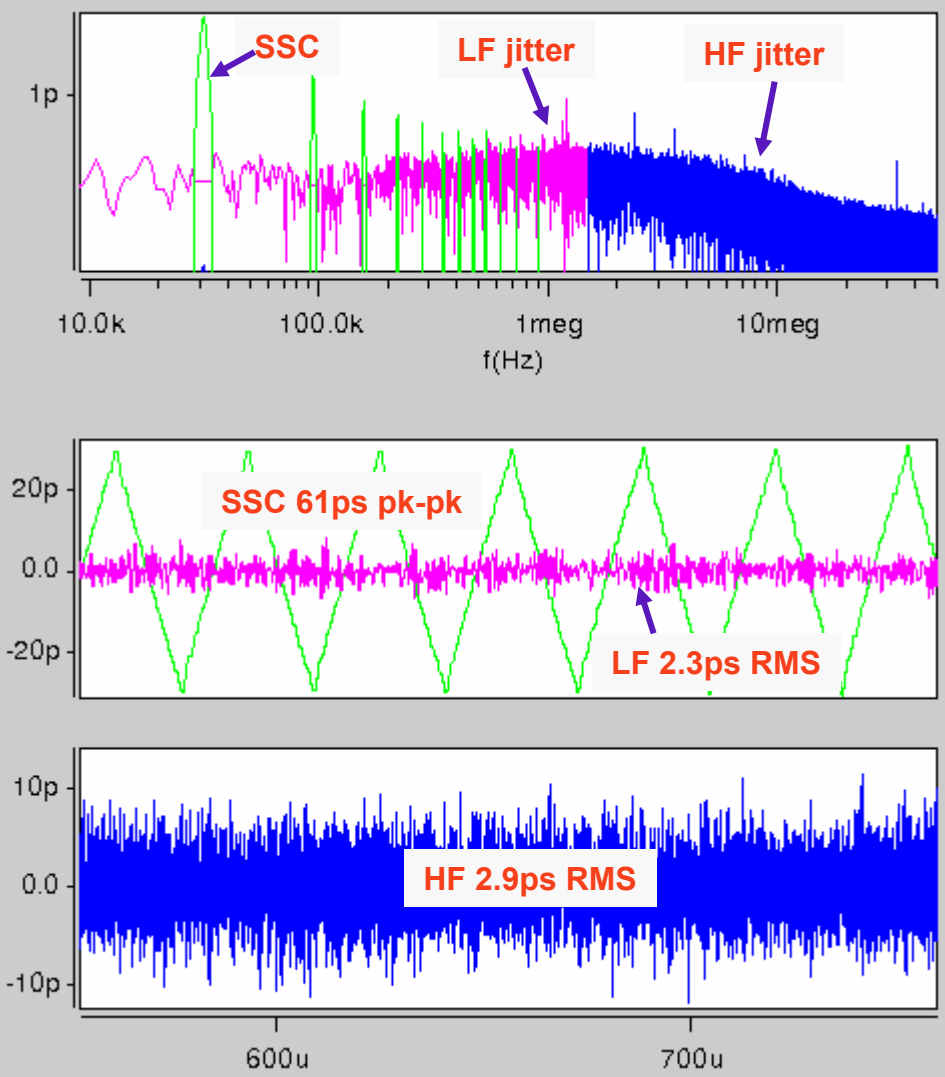
SSC and RMS jitter separation



- Search for SSC fundamental
  - ✓ Fundamental occupies multiple frequency bins
- Search for each harmonic up to when the harmonic amplitude drops below noise floor
  - ✓ This example 23rd (~905kHz)
- Create three frequency domain records by selectively attenuating frequency bins of originally record containing:
  - ✓ SSC only
  - ✓ LF jitter between 10kHz and 1.5MHz with SSC removed
  - ✓ HF jitter above 1.5MHz
- Record and measure pk-pk of SSC and RMS of LF and RF jitter

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Reference clock jitter specs

- 2.5GT/s uses a pk-pk measurement method with sample size to estimate TJ eye closure
- 5GT/s uses a SSC separation technique and an RMS estimate for residual jitter LF and HF jitter
  - ✓ HF RMS jitter is RSS with other sources of RJ_{DD} in timing budget
    - – Note RMS estimate will penalize clock generators with large spur amplitudes
  - ✓ SSC, LF and HF RMS is applied to the Rx in the jitter tolerance test
- 2.5GT/s uses 2 PLLs and CDR transfer function plus transport delay
- 5GT/s does not use CDR transfer function
- 5GT/s allows a choice of PLL bandwidths and peaking
  - ✓ All combinations should be measured and worst case used
- Refclk HF jitter is tightened considerably for 5 GT/s:

$T_{REFCLK\_HF\_RMS}$	3.1ps
$T_{REFCLK\_LF\_RMS}$	3.0ps
T_{REFCLK_SSC}	75ps
T_D	12ns

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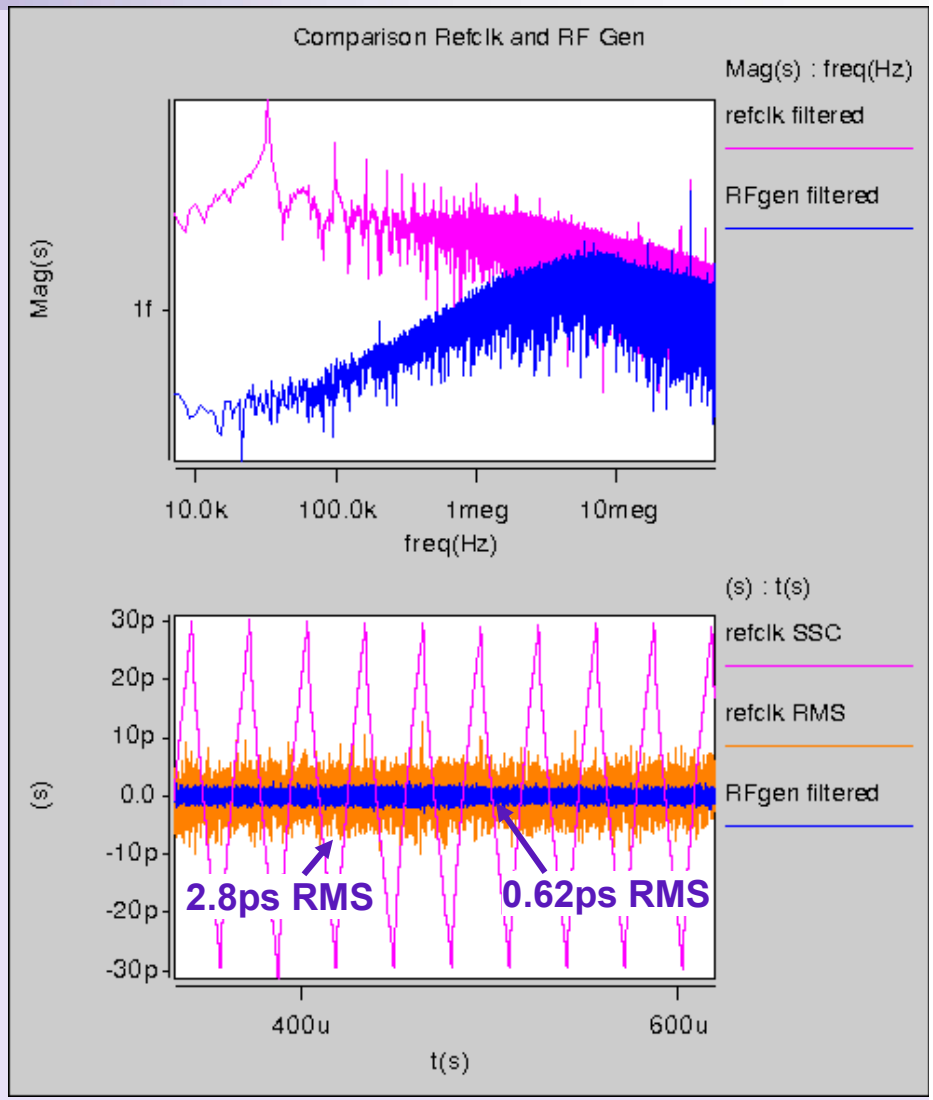
Measurement phase jitter Refclk versus RF Gen

- One way of measuring refclk phase jitter and processing the results is to use a real-time digital sampling scope
  - ✓ PCI SIG scripts and test equipment vendor support
- Unfortunately the analog noise floor of such measurement equipment can approach the RMS jitter being measured on the reference clock for 5GT/s; example 0.62 vs 2.8 ps
  - ✓ Need to bound error from measurement equipment
- If using high noise floor measurement equipment then recommended method for establishing noise floor is to calibrate equipment with a low phase noise (<500fs) RF generator and post process with software



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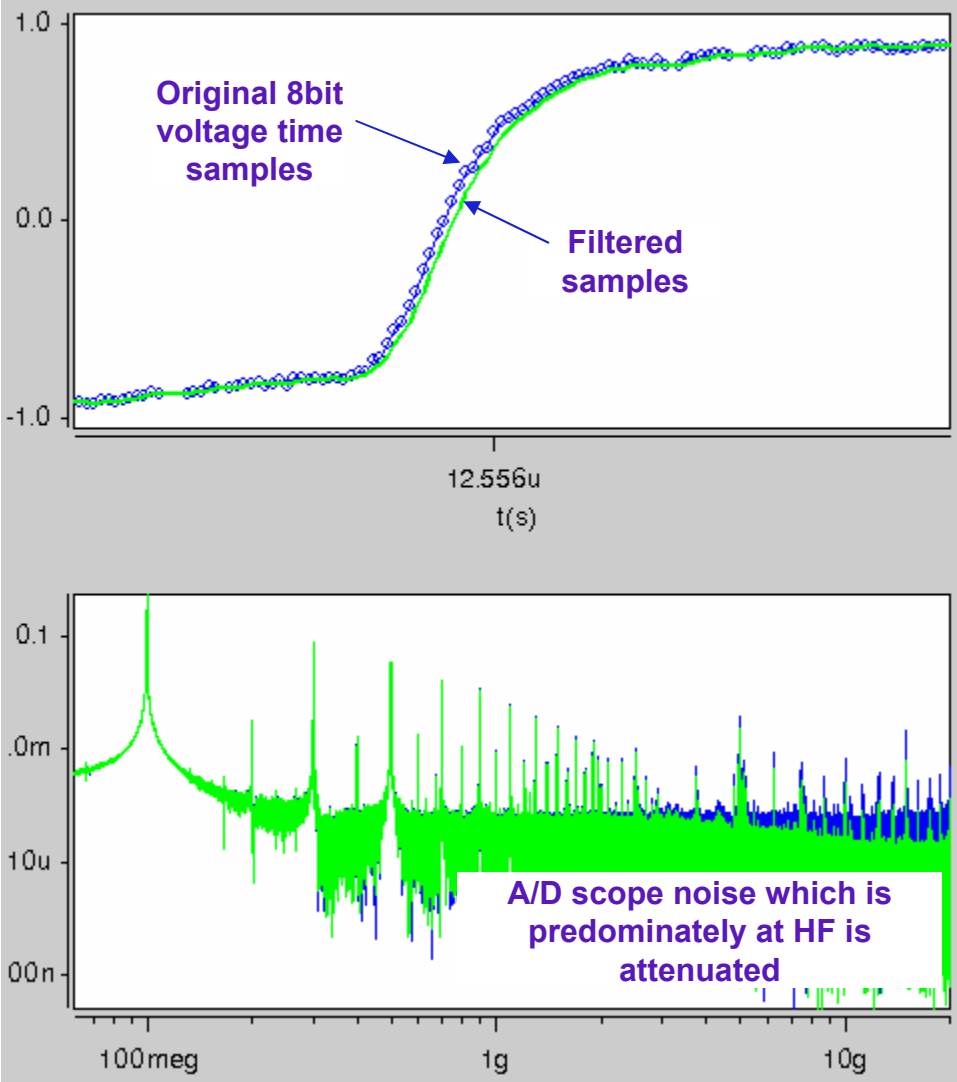
Scope noise floor reduction



- Availability of 40Gs/s scopes with >10GHz bandwidth enables simple noise floor reduction techniques
- Make a reasonable assumption of maximum PCIe refclk input bandwidth
  - ✓ 5GHz bandwidth
- Computed voltage time points provide increased voltage resolution (>8bits) and are formed by the average of local samples
- Provides a reduction of RMS noise after crossing time calculation
  - ✓ Typically 0.4ps RMS

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Measurement Alternatives

- An alternative way of measuring refclk phase jitter and processing the results is to use a clock recovery based instrument
  - ✓ Uses 14 bit A/D resolution
  - ✓ Confines the measurement to the data edge
  - ✓ With a smaller noise bandwidth
- All refclk jitter separations can be done on waveform and frequency bins as per specifications to obtain:
  - ✓ SSC only
  - ✓ LF jitter between 10kHz and 1.5MHz with SSC removed
  - ✓ HF jitter above 1.5MHz Measure edge rate of clock to be measured

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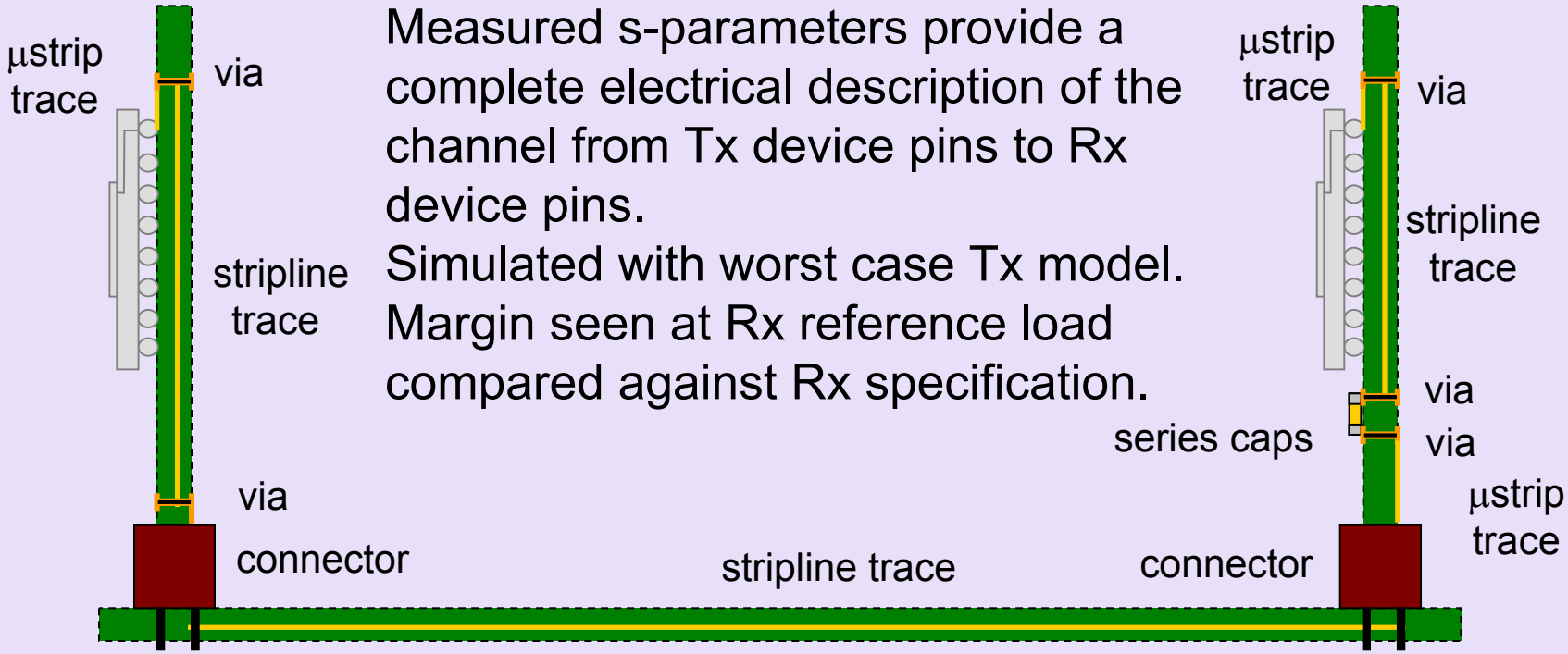
PCIe 2.0 Channel Specification:

Characterizing the channel
Extracted channel approach
Selecting worst case Tx parameters
Accounting for non-simulated jitter

Extended Channel Approach



Measured s-parameters provide a complete electrical description of the channel from Tx device pins to Rx device pins.
Simulated with worst case Tx model.
Margin seen at Rx reference load compared against Rx specification.

- Key channel effects:
  - Dielectric and conductor loss
  - Impedance discontinuities
  - Crosstalk, forward & reverse
  - Mode conversion effects

S-parameters capture all loss effects
Channel step response is equivalent

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Reducing Number of Terms

- A generalized 3-in, 3-out differential measurement would require 12^2, or 144 separate single-ended measurements
- But, there are methods of reducing the number of measurements considerably
  - ✓ Symmetry:
    - Directionality: Sij = Sji
    - Aggressors symmetric with respect to victim
    - D+ and D- of victim line may be symmetric with respect to aggressors
  - ✓ Unused data:
    - Aggressor → aggressor or victim → aggressor parameters
    - Return loss on aggressor ports
- Making use of the above can reduce the number of measurements to ≈12
  - ✓ Aggressor → victim crosstalk: 4, victim near end & far end return loss: 4, Vict insertion loss: 4

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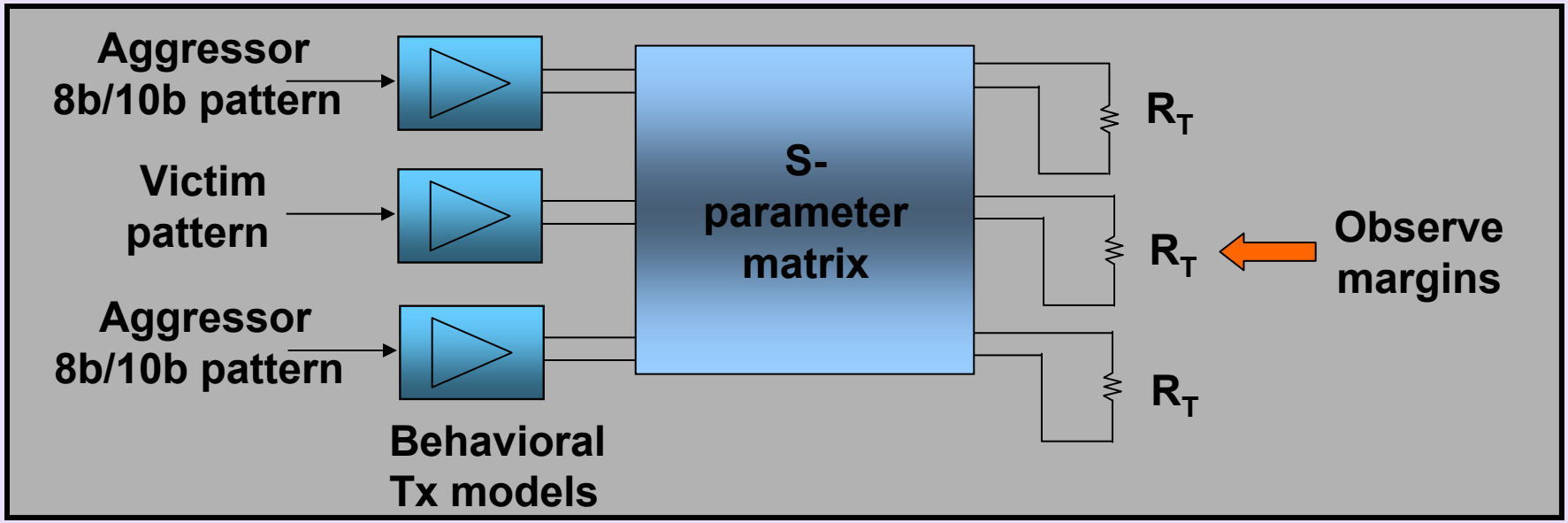
End to End Simulation Model

- Tx characteristics included in simulation:
  - ✓ $V_{TX\text{-}DIFF\text{-}PP\ (min)}$, $V_{TX\text{-}DE\text{-}RATIO\ (min\ and\ max)}$, $T_{MIN\text{-}PULSE\ (min)}$, $T_{TX\text{-}RISE\text{-}FALL\ (min\ and\ max)}$,
  - ✓ $T_{RF\text{-}MISMATCH\ (max)}$, $RL_{TX\text{-}DIFF}$, Aggressor-to-Victim skew
- Most Tx parameters can be fixed at worst case values found via inspection while others need to be swept.
- Measurement into reference load (R_T) provides uniform load characteristics



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Worst Case Tx Parameters for 5 GT/s Channel Simulation

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	800		mV	Only min value needed in simulations.
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	400		mV	Only min value needed in simulations. Refer to Section 4.3.6.2.6.
$V_{TX-DE-RATIO-6DB}$	Tx de-emphasis level	5.5	6.5	dB	Both min/max range needs to be simulated.
$V_{TX-DE-RATIO-3.5DB}$	Tx de-emphasis level	3.0	4.0	dB	Both min/max range needs to be simulated.
$T_{MIN-PULSE}$	Instantaneous pulse width	0.9		UI	Single pulses of both polarity need to be compressed to min value
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	0.15		UI	Some channels sensitive to min value. Max value defined by T_{TX-EYE}
$T_{RF-MISMATCH}$	Tx rise/fall mismatch		0.1	UI	Only max value needed in simulations
$RL_{TX-DIFF}$	Tx package plus Si differential return loss	- 8 - 10		dB	Over 1.25 – 2.5 GHz range Oer 0.05 – 1.25 GHz range
RL_{TX-CM}	Tx package plus Si common mode return loss		6	dB	Same as defined in Tx spec

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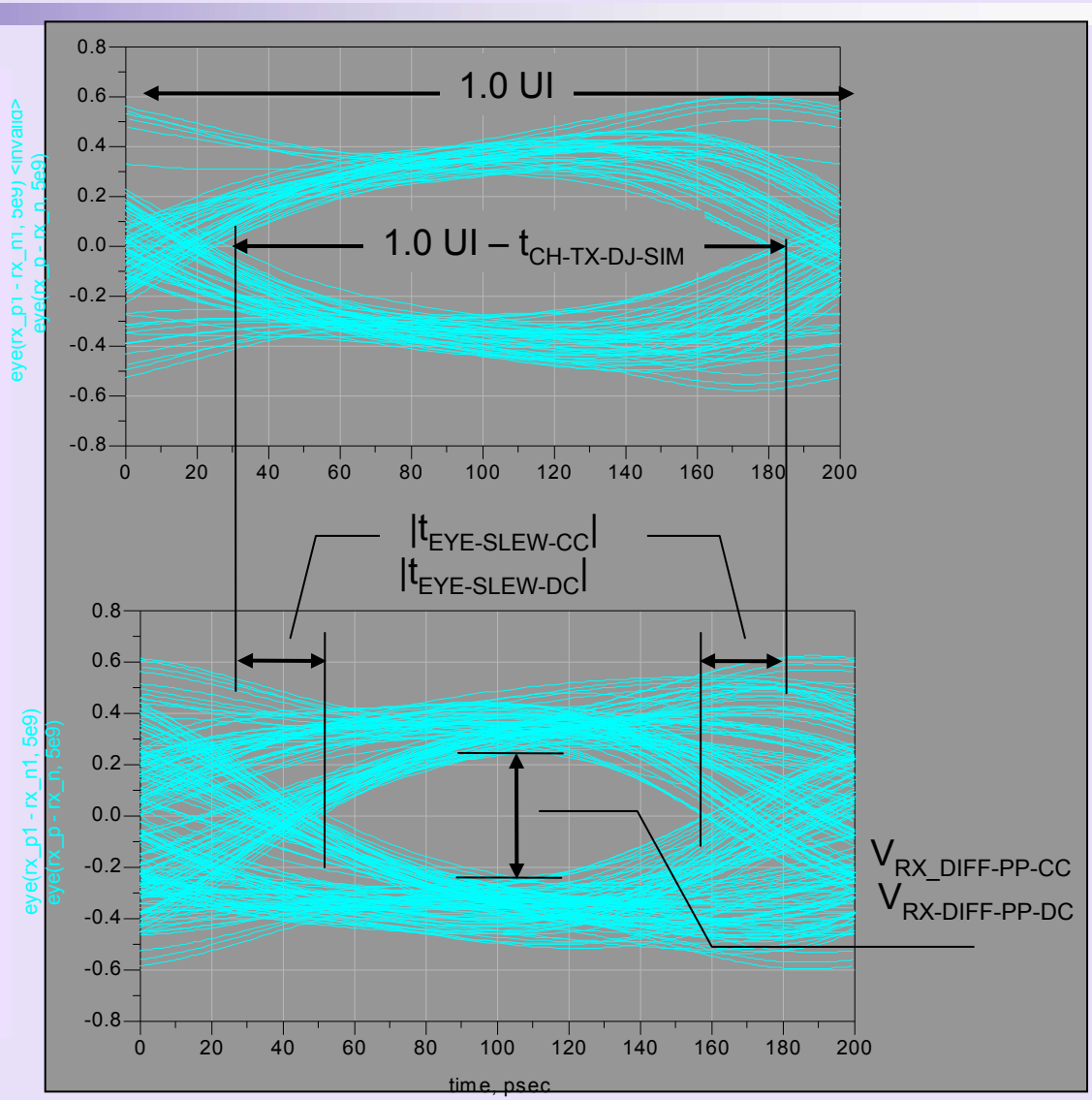
Accounting for Non-Simulated Jitter

- Low frequency jitter not comprehended in channel simulation
- May be accounted for by applying rectangular exclusion zone as shown below.
- Both eye width and eye height are affected
  - ± 28.9 ps for common clk
  - ± 34.7 ps for data clocked
  - 120 mVPP for common clk
  - 100 mVPP for data clocked



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PCI
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PCIe 2.0 Receiver Specification:
Advantages of tolerancing methodology
Calibration channel
Calibrating test setup
Key AC parameters for each Refclk architecture: Common, Data & Separate
PCI
EXPRESS

Characterizing the Receiver

- Procedure for Rx Tolerancing
  - ✓ Build test setup capable of injecting into receiver worst case jitter and voltage margins as defined in Rx spec table
  - ✓ Calibrate setup into precision reference load
  - ✓ Replace reference load with Rx under test and observe BER
- Advantages of a Tolerancing-based Rx spec
  - ✓ Minimizes guardbanding while stressing DUT
  - ✓ Makes use of BER, the only output an Rx can provide
  - ✓ Proven in other high speed Comm interfaces

Rx margining leverages LF/HF jitter separation methodology employed for Refclk and transmitter

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Calibration Channel

- The purpose of the calibration channel is to generate the maximum ISI that sets max limit for $V_{RX\text{-}MIN\text{-}MAX\text{-}RATIO}$
  - ✓ Calibration channel is defined to yield 5:1 voltage ratio.
  - ✓ Ratio value empirically determined
  - ✓ Channel length: ≅28” for FR4 material and 5 mil wide traces or 40” and 10 mil for higher quality materials such as Nelco 4000-13
  - ✓ Pattern generator may drive a binary output, no de-emphasis rqd.
  - ✓ From receiver’s point of view, Tx de-emphasis is irrelevant as long as Rx is driven with simultaneous w/c margins
- Calibration channel characterized in terms of its transient response, and return loss
  - ✓ Calibration channel return loss must be 20 dB or better over 0.5 GHz to 5.0 GHz range

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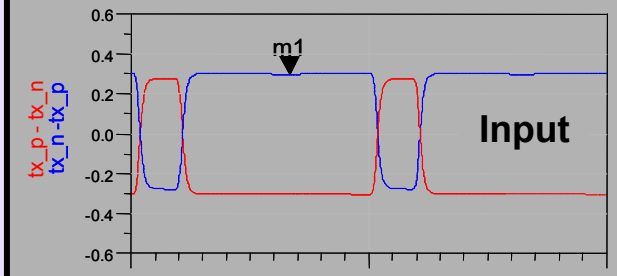
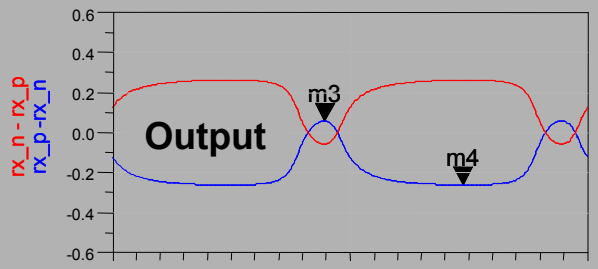
Characterizing the Calibration Channel

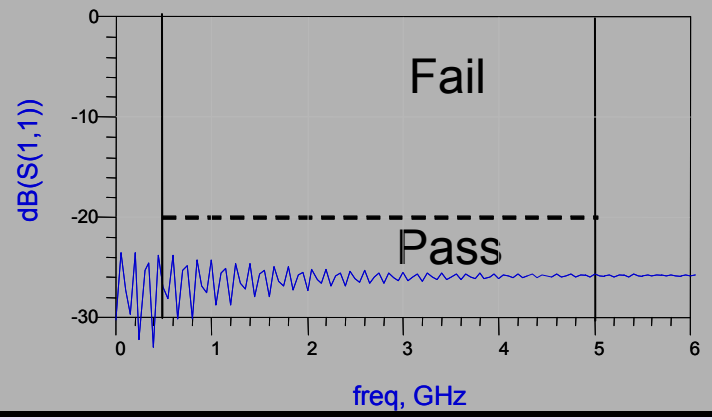


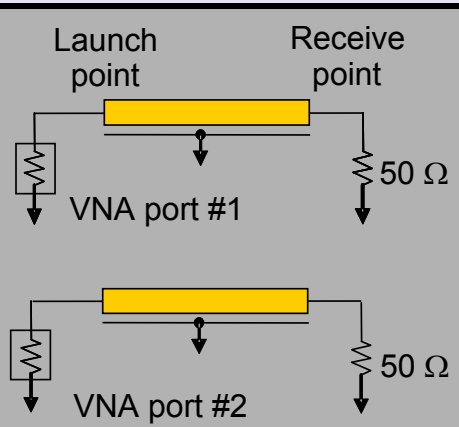
Pattern consists of 0.9 UI low followed by 5.1 UI high and represents w/c pulse DCD distortion



V_{SWING} min/max ratio is ~ 5.0/1

Transient behavior





Calibration channel return loss must be 20 dB or better over 0.5 – 5.0 GHz range

Return Loss

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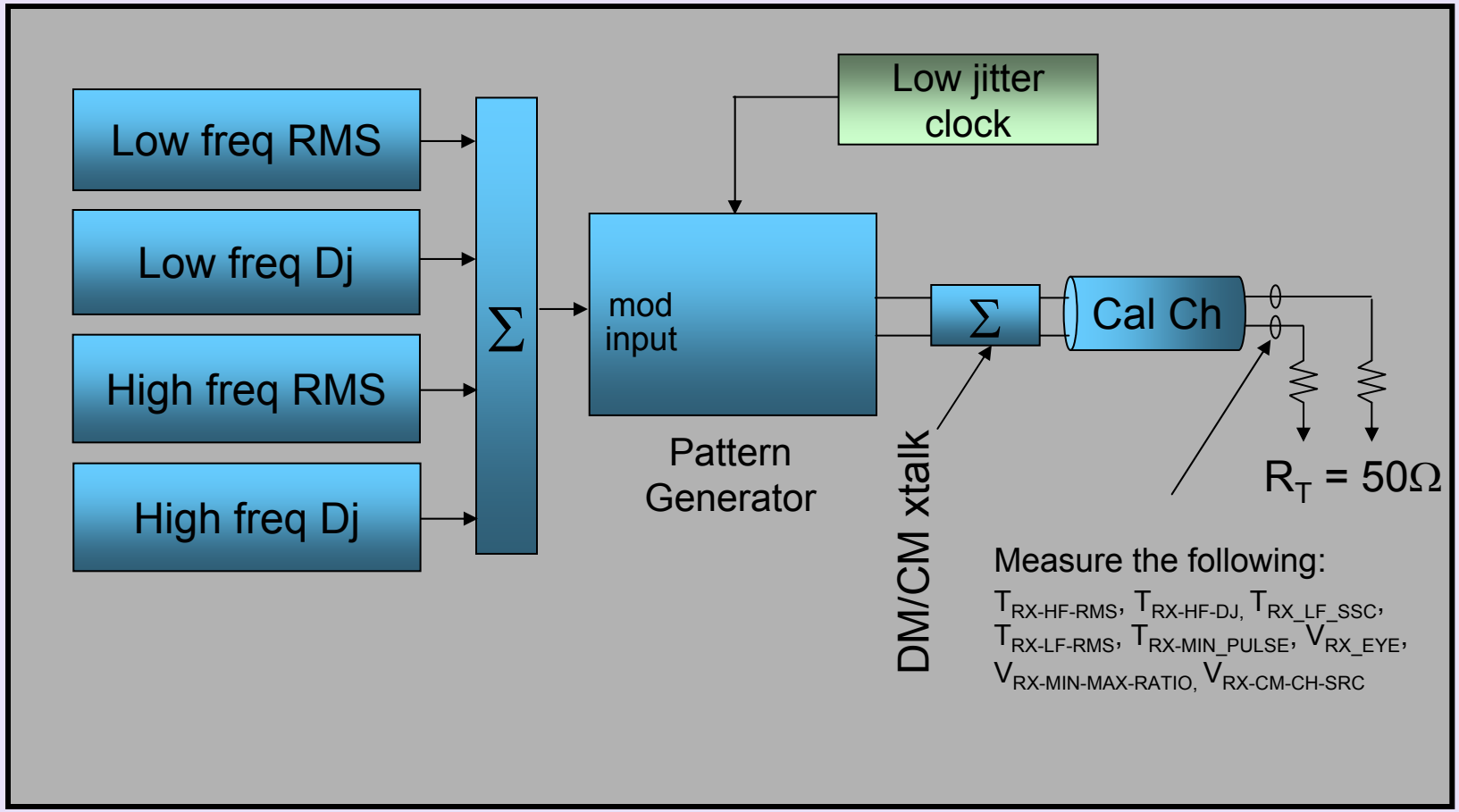
Calibrating Rx Margining Setup (step 1)



Test setup shown represents functionality only, not actual instruments

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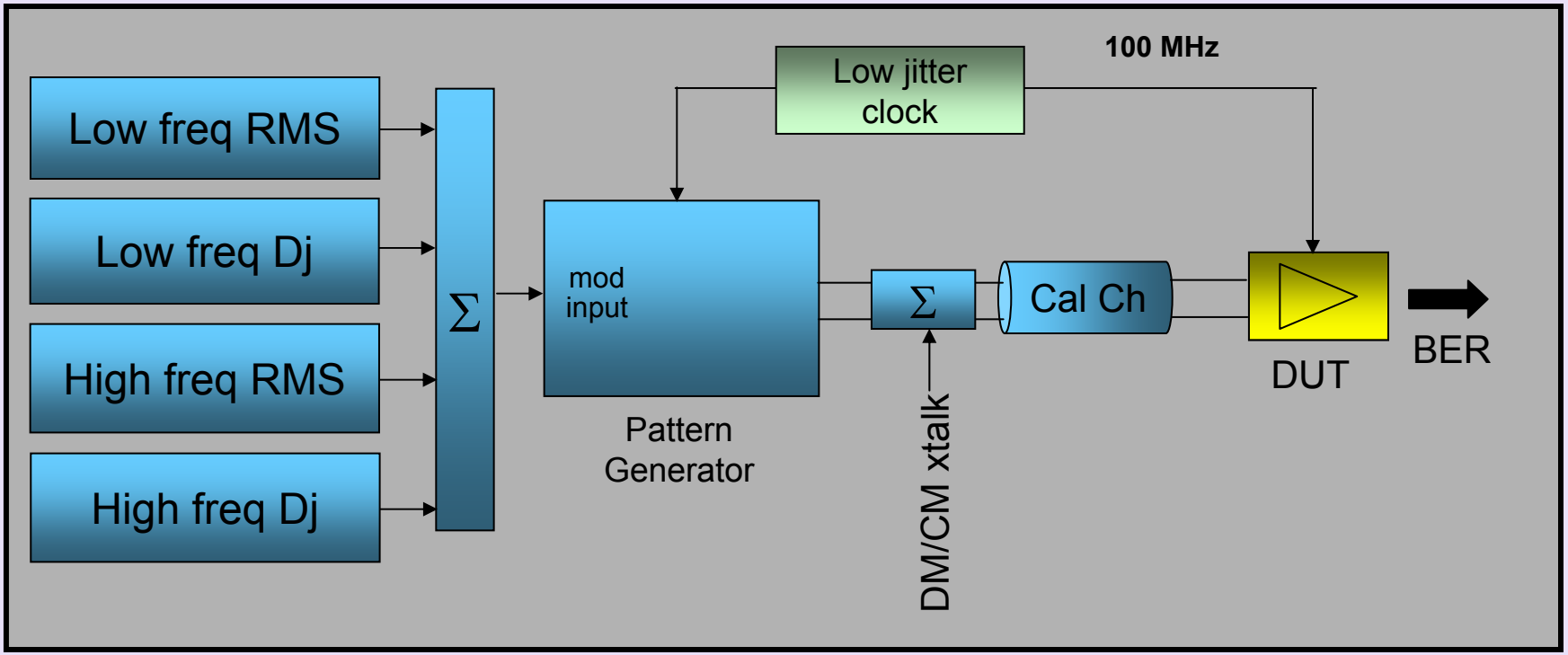
Characterizing Rx to Spec (Step 2)



- Pattern generator's internal clock must be sync'ed to external Refclk
- Low jitter Refclk obviates need for 2-port measurement
- Direct measurement of 10^{-12} BER is possible in <20 minutes

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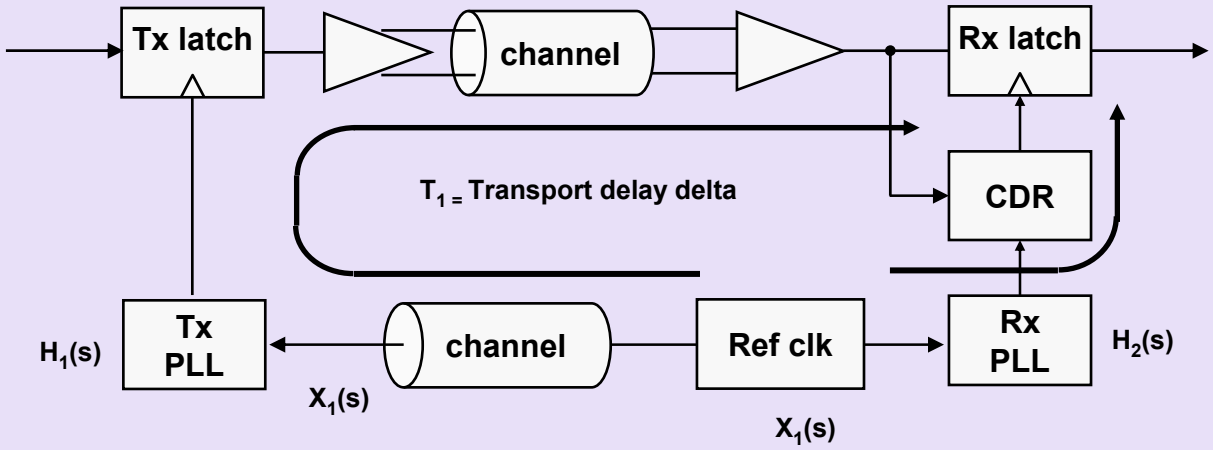
Common Clock Topology



$$H(s)=\left[\underbrace{\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}}_{\text{5 MHz, 1 dB or 8 MHz, 3 dB}}e^{-sT_1}-\underbrace{\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}}_{\text{16 MHz, 3 dB}}\right]$$

$$Y(s)=X_1(s)*H(s)$$

PLL difference function

- **Tx and Rx paths track LF jitter in accordance with PLL difference function.**
- **PLL difference function removes jitter in below 5 MHz and above 16 MHz**
- **SSC residual jitter reduced to 33 KHz, 75 ps triangular waveform**

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Receiver Tolerancing Setup (Common clock architecture)

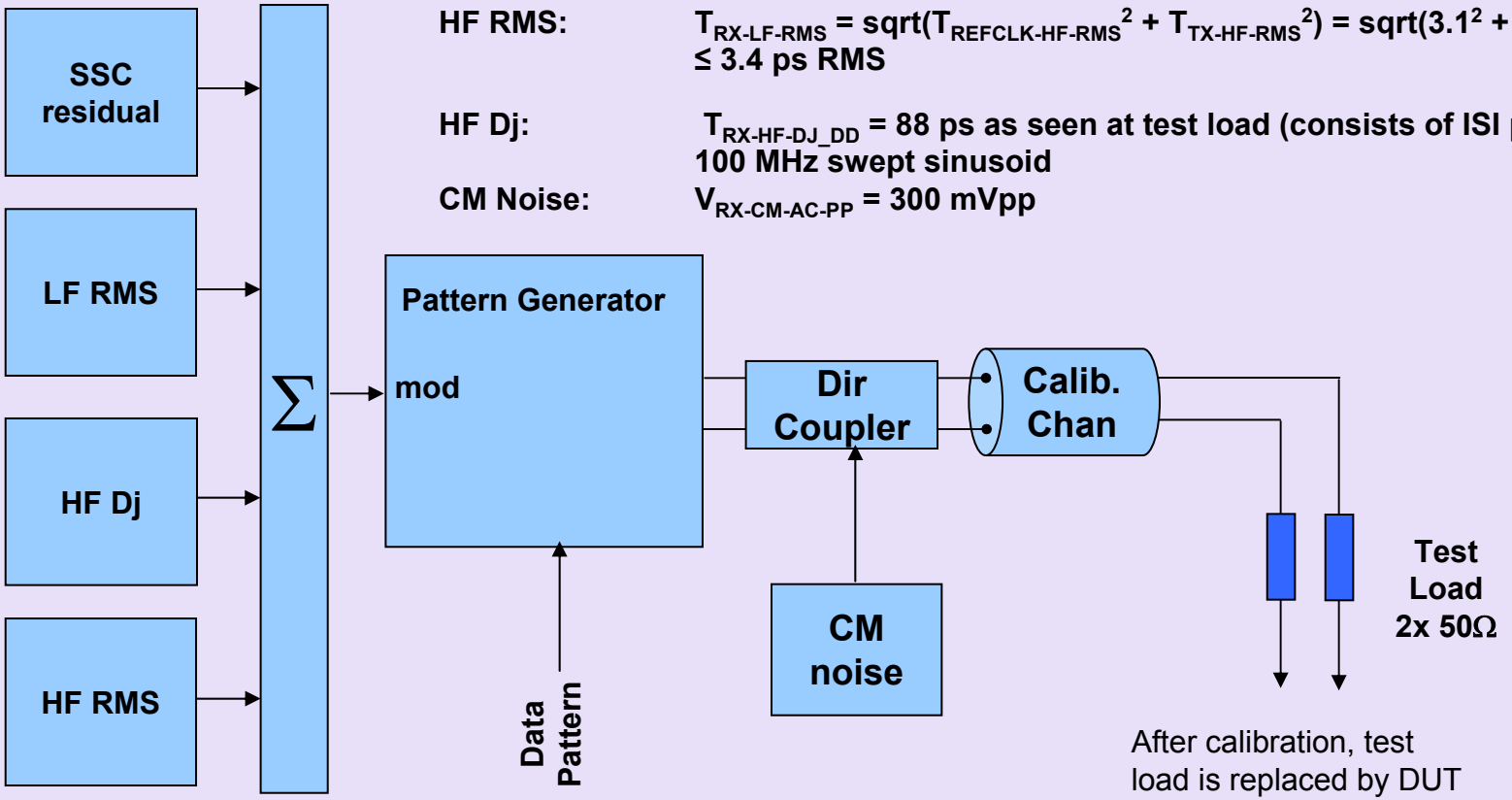
SSC residual: $T_{RX\text{-}SSC}$ = 75 ps (residual due primarily to transport delay)

LF RMS: $T_{RX\text{-}LF\text{-}RMS} = \text{sqrt}\,(T_{TX\text{-}LF\text{-}RMS}^2 + T_{REFCLK\text{-}LF\text{-}RMS}^2) = \text{sqrt}(3.0^2 + 3.0^2)$
≤ 4.2 ps RMS

HF RMS: $T_{RX\text{-}LF\text{-}RMS} = \text{sqrt}(T_{REFCLK\text{-}HF\text{-}RMS}^2 + T_{TX\text{-}HF\text{-}RMS}^2) = \text{sqrt}(3.1^2 + 1.4^2)$
≤ 3.4 ps RMS

HF Dj: $T_{RX\text{-}HF\text{-}DJ\_DD}$ = 88 ps as seen at test load (consists of ISI plus 1.5 – 100 MHz swept sinusoid

CM Noise: $V_{RX\text{-}CM\text{-}AC\text{-}PP}$ = 300 mVpp



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5.0 GT/s Rx Tolerancing Parameters (common clock architecture)

Parameter	Description	Min	Max	Units
UI	Unit Interval	199.94	200.06	ps
$T_{RX\_HF\_RMS}$	> 1.5 MHz Rj		3.4[1]	ps RMS
$T_{RX\_HF\_DJ\_DD}$	> 1.5 MHz Dj (including channel effects)		88[2]	ps
$T_{RX\_SSC\_RES}$	0-1.5 MHz Dj (SSC residual)		75[3]	ps
$T_{RX\_LF\_RMS}$	0-1.5 MHz Rj		4.2[4]	ps RMS
$T_{RX\_MIN\_PULSE}$	Minimum width pulse at Rx	120		ps
$V_{RX\_MAX\_MIN\_RATIO}$	min/max pulse voltage ratio on consecutive UI		5	--
V_{RX_EYE}	Receive eye voltage aperture	120	1200	mV
$V_{RX\text{-}CM\text{-}AC\text{-}PP}$	Common mode noise		300	mVPP

1. Jitter BW: 1.5 – 100 MHz, spectrally flat, consisting of contributions from Refclk and Tx
2. Includes sinusoidal component plus channel effects. Sinusoid swept continuously from 1.5 – 100 MHz or over same range in 10^{th} octave steps
3. SSC residual consists of 33 KHz triangular wave with 75 ps PP magnitude
4. 0 – 1.5 MHz, spectrally flat, consisting of contributions from Refclk and Tx

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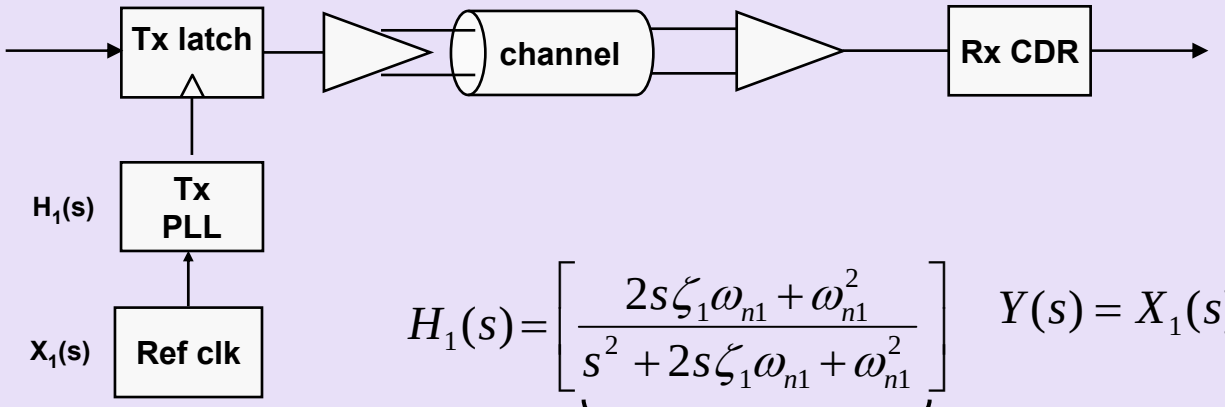
Data Driven (CDR) Topology



$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \right]$$

16 MHz, 3 dB

$$Y(s) = X_1(s) * H_1(s)$$

PLL difference function

- **The full 20 ns of SSC jitter must be tracked by the CDR**
- **Receiver must track additional <1.5 MHz Rj and Rj in the 1.5 MHz to 8 MHz range that would otherwise be removed by the PLL difference function in the CC case.**
- **Rx must also track LF Refclk jitter from 1.5 MHz down to 10 KHz**

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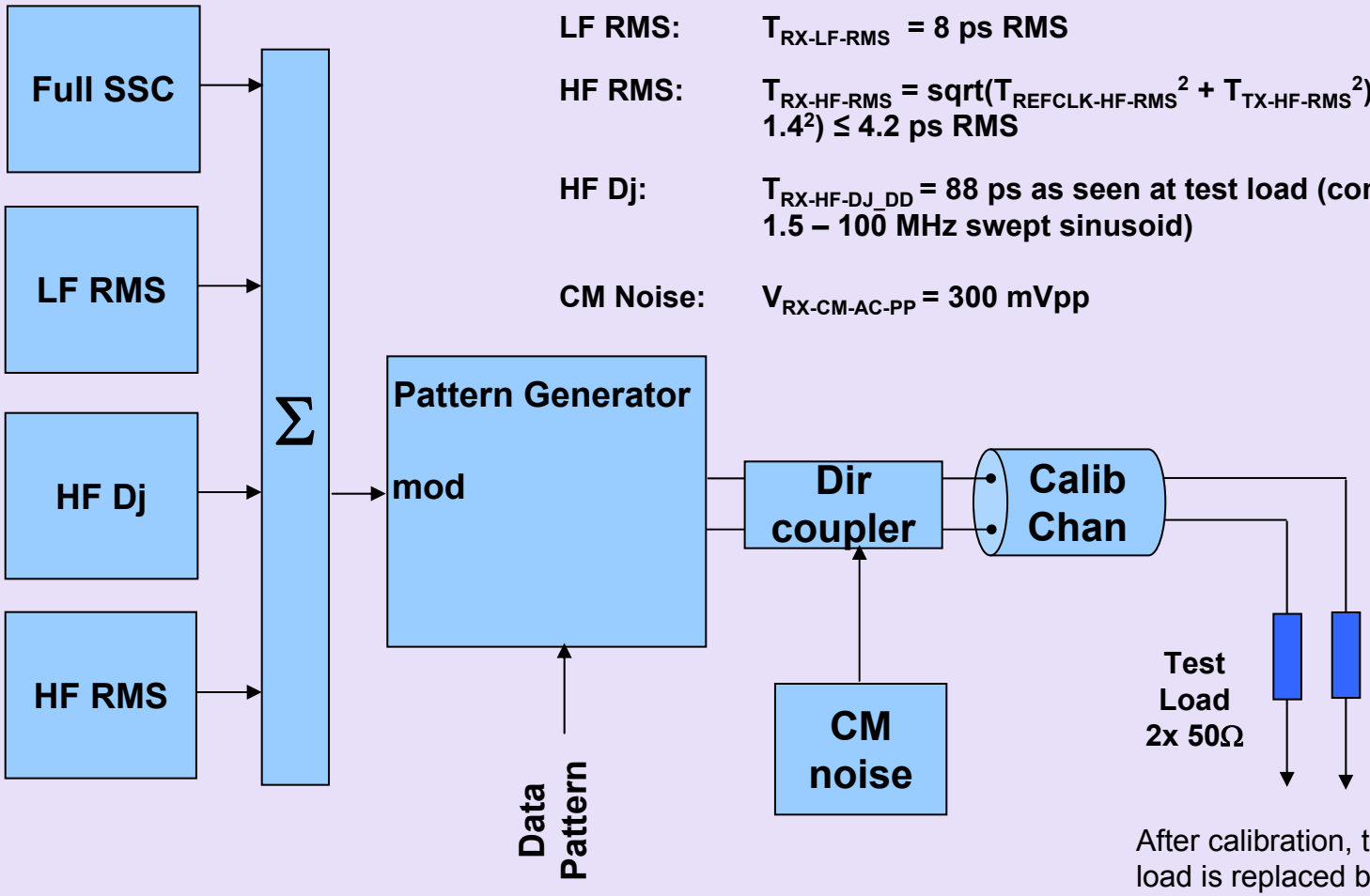
Receiver Tolerancing Setup

(Data Driving clock architecture)



Full SSC: $T_{RX\text{-}SSC}$ = 20 ns. Rx must track entirety of SSC

LF RMS: $T_{RX\text{-}LF\text{-}RMS}$ = 8 ps RMS

HF RMS: $T_{RX\text{-}HF\text{-}RMS} = \text{sqrt}(T_{REFCLK\text{-}HF\text{-}RMS}^2 + T_{TX\text{-}HF\text{-}RMS}^2) = \text{sqrt}(3.9^2 + 1.4^2) \leq 4.2$ ps RMS

HF Dj: $T_{RX\text{-}HF\text{-}DJ\_DD}$ = 88 ps as seen at test load (consists of ISI plus 1.5 – 100 MHz swept sinusoid)

CM Noise: $V_{RX\text{-}CM\text{-}AC\text{-}PP}$ = 300 mVpp

After calibration, test load is replaced by DUT

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5.0 GT/s Rx Tolerancing Parameters (data driving architecture)

Parameter	Description	Min	Max	Units
UI	Unit Interval	199.94	200.06	ps
$T_{RX\_HF\_RMS}$	> 1.5 MHz Rj		4.2[1]	ps RMS
$T_{RX\_HF\_DJ-DD}$	Max Dj impinging on Rx under tolerancing		88	ps
$T_{RX\_LF\_SSC\_FULL}$	0-1.5 MHz Dj (Full SSC)		20[2]	ns
$T_{RX-LF-RMS}$	10 KHz – 1.5 MHz RMS jitter		8[3]	ps RMS
$T_{RX\_MIN\_PULSE}$	Minimum width pulse at Rx	120		ps
$V_{RX\_MAX\_MIN\_RATIO}$	min/max pulse voltage ratio on consecutive UI		5	--
V_{RX_EYE}	Receive eye voltage aperture	100		mV
$V_{RX-CM-AC-PP}$	Common mode noise		300	mVPP

1. Spectrally flat from 0 – 1.5 MHz. Includes 3.9 ps from Refclk and 1.4 ps from Tx
2. Full SSC must be tracked. Includes sinusoidal component plus channel effects.
3. Over 10 KHz – 1.5 MHz BW with -20 dB/decade to account for 1/f noise slope

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PCI
SIG
Transmitter
Reference Clock
Channel
Receiver
Future Developments
PCI
EXPRESS

PCIe 3.0 Requirements

- Data through put rate: 2x PCIe 2.0 bandwidth
  - ✓ Not required to exceed 2x cadence
- Cost: HVM materials and tolerances
  - ✓ FR4, PCIe connectors, low-cost clocks, etc
  - ✓ Pay-as-you-go (e.g. surface mount connectors, back drilled vias, etc)
- Compatibility: same as existing usage models
  - ✓ New devices must operate with old devices at highest common performance level
  - ✓ Similar power budget as before
  - ✓ Same clocking architectures (Common Refclk, Data Driven) with SSC
  - ✓ Same channel reach as before
    - Client: 14”, one connector, FR4 PCB
    - Server: 20”, two connectors, FR4 PCB
- Options considered
  - ✓ Two options considered, both yielding 2x PCIe 2.0 bandwidth
    - ❶ 10GT/s with 8b/10b coding
    - ❷ 8GT/s without 8b/10b (using scrambling only)

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Assumptions/Enablers

- Statistical jitter analysis
  - ✓ More closely approximates reality
  - ✓ Doing without leaves too much margin on the table
- Optimized Refclk/CDR bandwidths
  - ✓ Permits use of existing refclk infrastructure

	PCIe 2.0	PCIe 3.0***
Min CDR BW	1.5 MHz	10 MHz
PLL BW	8-16 MHz	2-4 MHz

- Trainable Tx/Rx equalization to mitigate channel effects
  - ✓ For removing ripple in pulse response more than HF loss
  - ✓ Rx equalization: multi-tap DFE*** (study in progress)
  - ✓ Tx equalization: multi-tap LE*** (study in progress)
  - ✓ Tap weights will need to be periodically retrained
- Process target: 65nm or better
  - ✓ Mainly to meet power requirements

*** Currently in discussion; not the final spec

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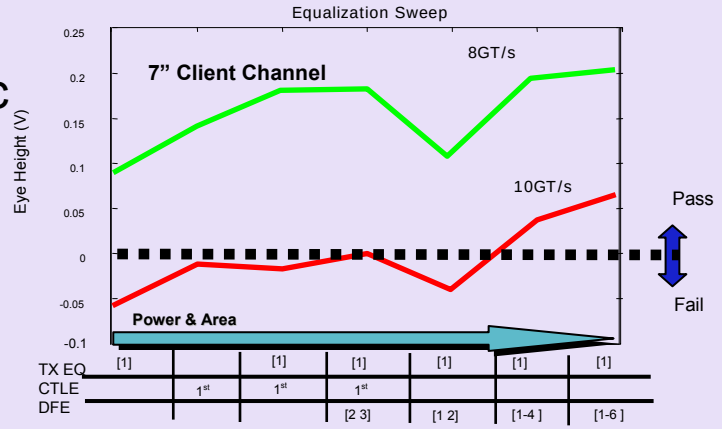
PCIe 3.0 Analysis Results

- 8GT/s is feasible over channels of interest with reasonable equalization and channel improvements
- 10GT/s imposes a power penalty
  - ✓ 8G-10G power increase nearly quadratic
- 10GT/s imposes a cost penalty
  - ✓ Lower loss PCB materials
  - ✓ Backdrilled vias
  - ✓ Layout restrictions



- PCI-SIG® unanimously approved 8GT/s as the target bit rate for PCIe 3.0
  - ✓ Base specification anticipated in late 1H09
  - ✓ CEM specification anticipated in late 2H09

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