
PCI
SIG®

Board Design Guidelines for PCI Express® Architecture

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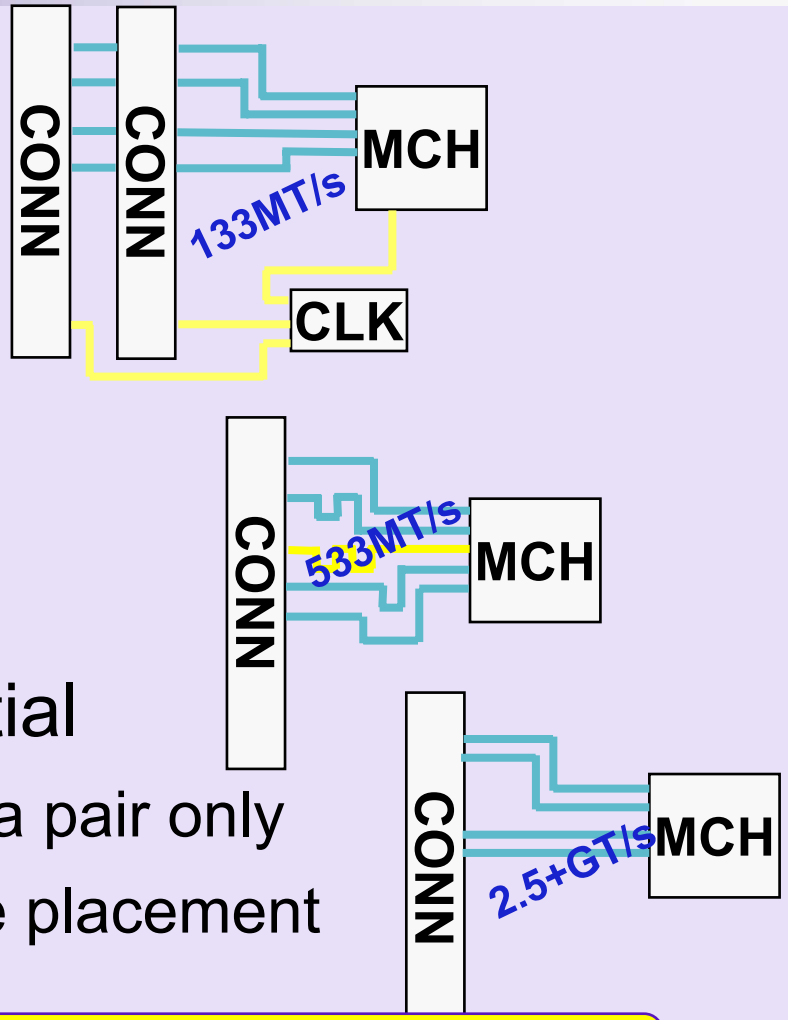
Agenda

- Background
- Layout considerations
- Simulations
- Compliance
- Summary

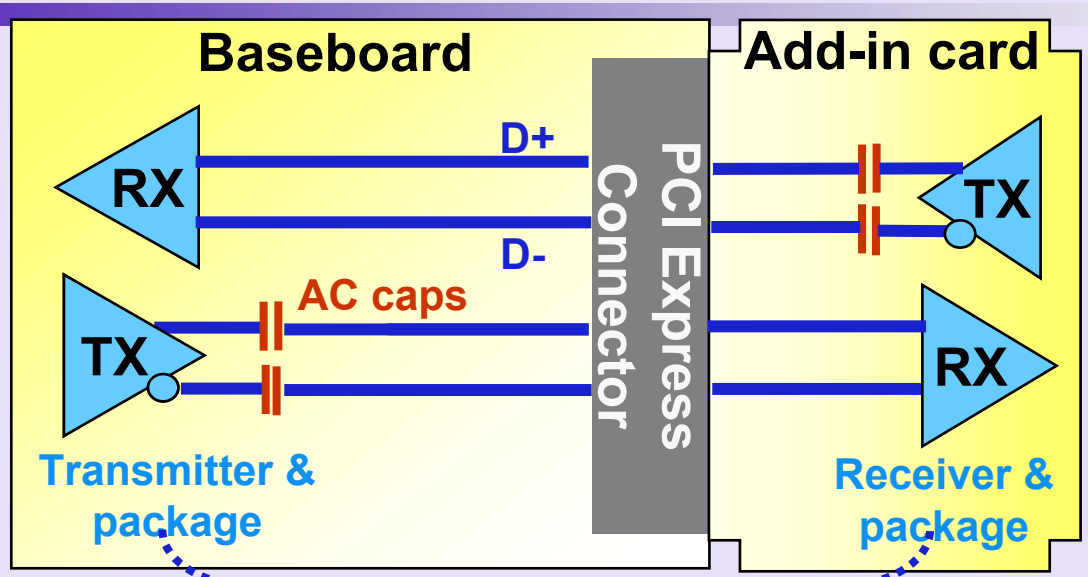
Bus Topologies

- PCI common clock
  - ✓ Meet setup/hold timing
  - ✓ Multi-drop parallel I/O
- AGP source synchronous
  - ✓ Match all data to strobe
  - ✓ Single strobe, multiple data
- PCI Express serial differential
  - ✓ Point-to-point, match per data pair only
  - ✓ Longer route, creative device placement

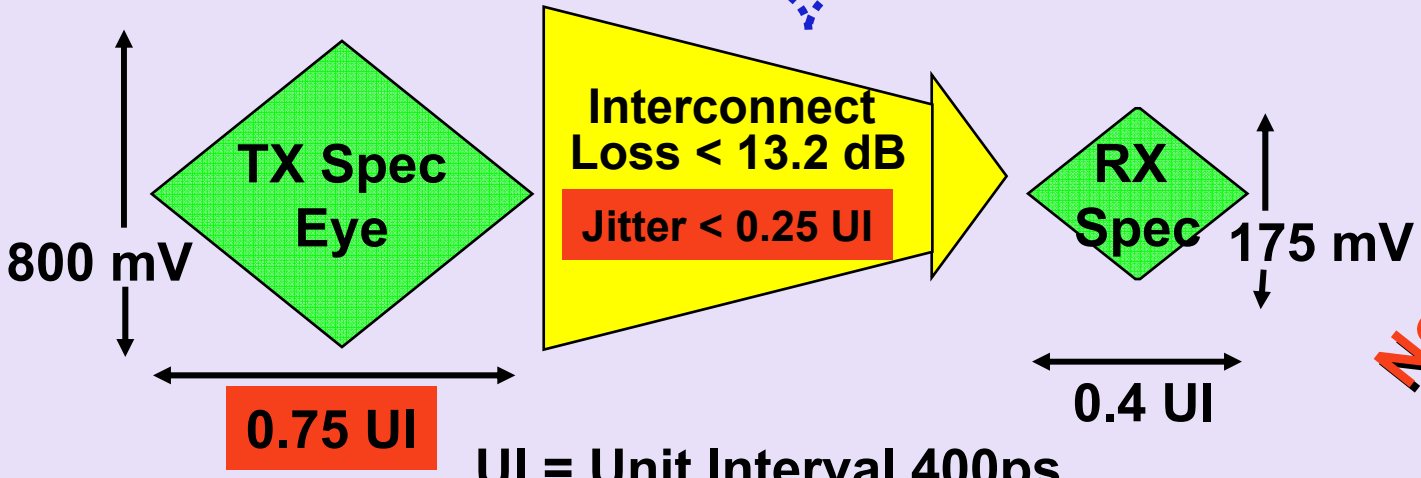


Point-to-point routing is straightforward

Serial differential



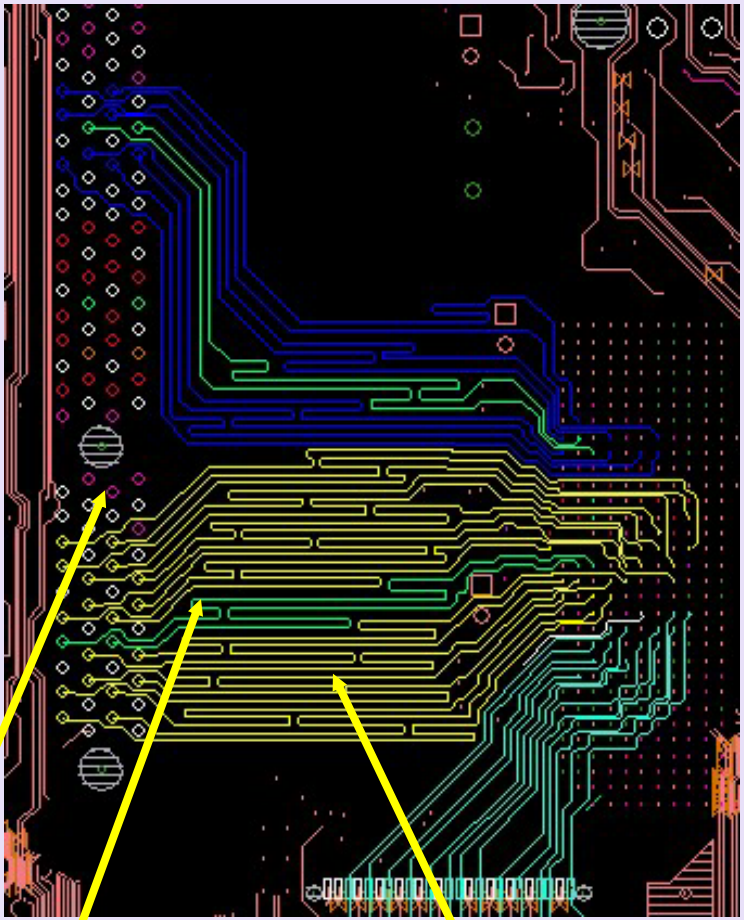
- ✓AC coupled
- ✓Lane-to-lane de-skew
- ✓Polarity inversion



Note: Min Tx Eye Width and Tj of Interconnect Changed in rev 1.1

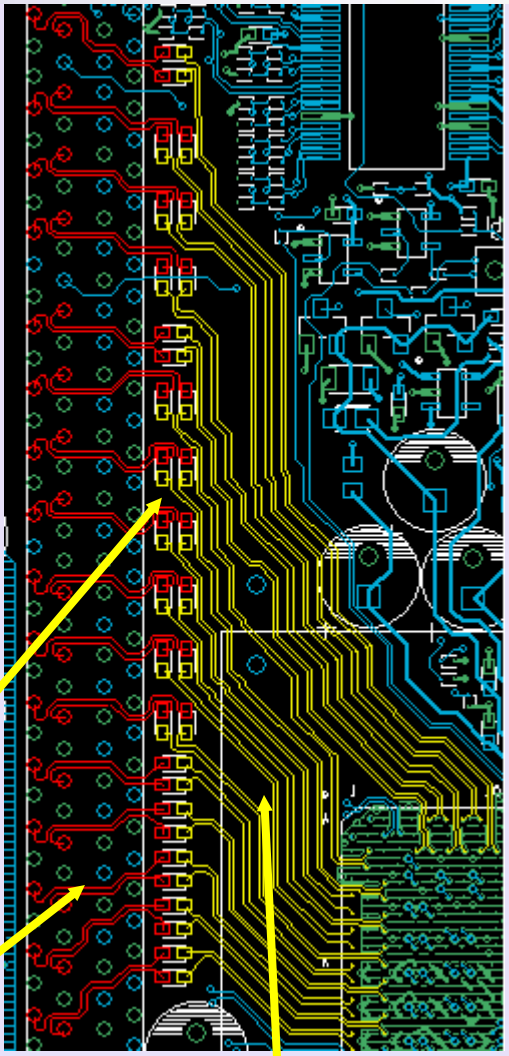
AGP8X Layout Challenges

- Data and Strobe must be length matched
  - ✓ Serpentine routing is needed for length matching
- Short Motherboard Trace Lengths
  - ✓ 2″–6″ max MCH to connector
- Tight Timing Budget
  - ✓ Data-to-strobe timing skew



PCI Express makes layout easy

- Trace length matching between pairs is not required
  - ✓ Embedded clock simplifies routing rules
- GND reference preferred
  - ✓ Avoid splits and voids
- Use GND stitching vias when changing layers
- Longer motherboard trace
  - ✓ 12”+ possible



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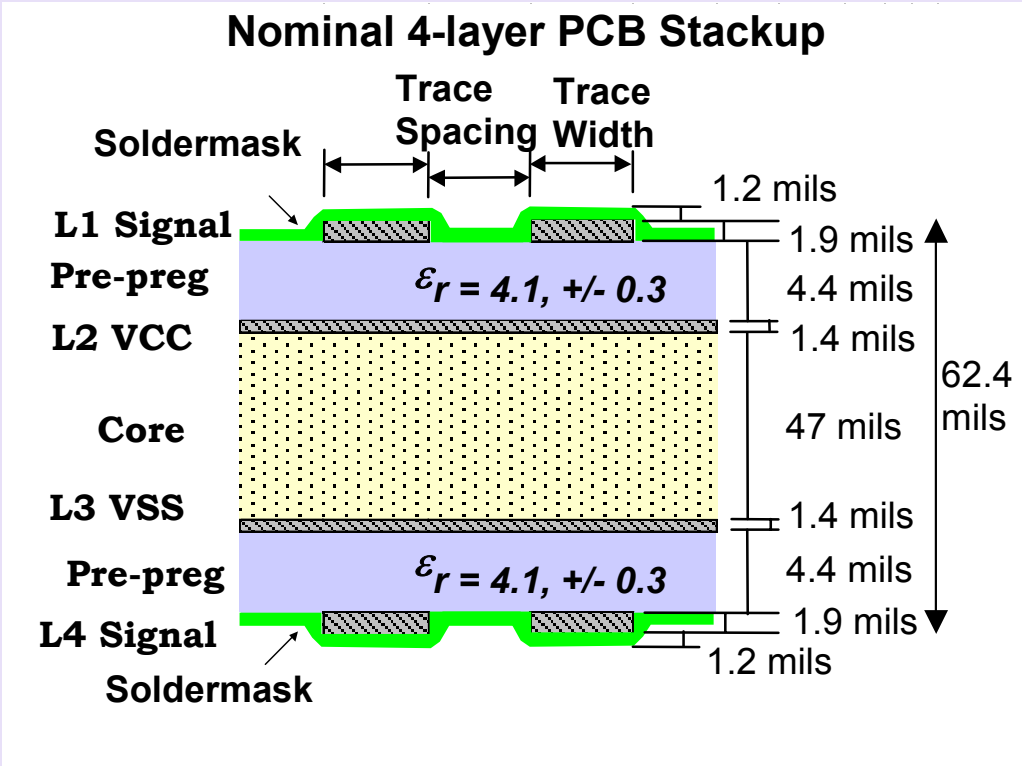
Stackup design

- No new PCB technology required
- Standard 4-layer stackup 0.062” thick PCB
- Microstrip ½ oz Cu plated Ok
- Stripline 1 oz Cu (6+ layers) Better



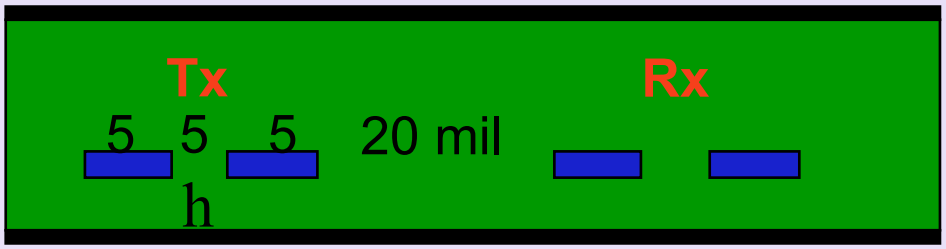
Follow simple layout rules & design tradeoffs

Trace Geometry & Impedance

- Use wider trace width ⇒ Minimize loss
- Use wider traces for long routes
- More pair-to-pair spacing ⇒ Minimize crosstalk
- Target differential Z_o of 100 Ω ±20%

Microstrip

Non-interleaved Topology example

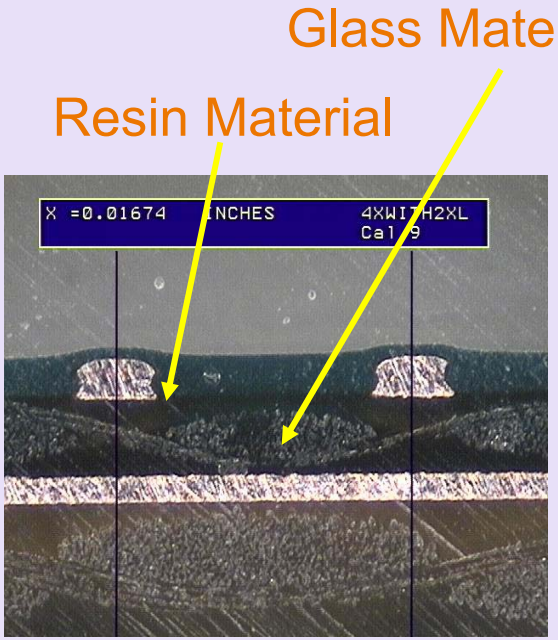


Stripline

Interleaved Topology example

PCB material dominates loss

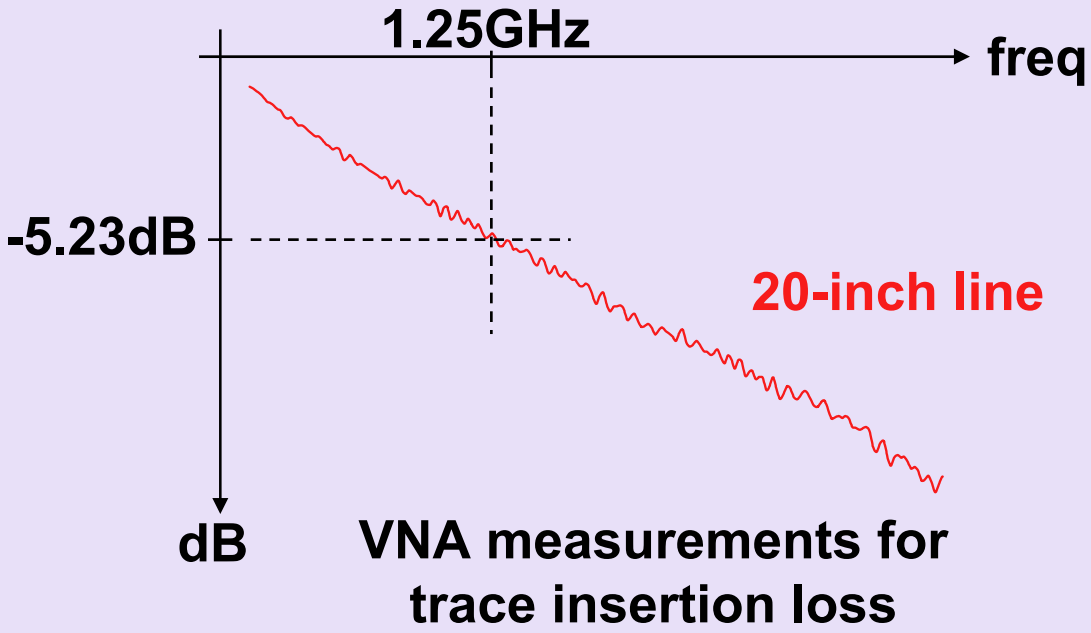
- Stackup FR4 material
  - ✓Copper roughness ⇒ loss ↑
  - ✓Thinner dielectrics ⇒ loss ↑
- Non-homogeneous dielectric
  - ✓Localized Zo variation due to material weave ⇒ loss ↑
- Wide differential Impedance variation on μstrip
  - ✓Etching and Plating process ⇒ loss ↑



FR4 cross-section

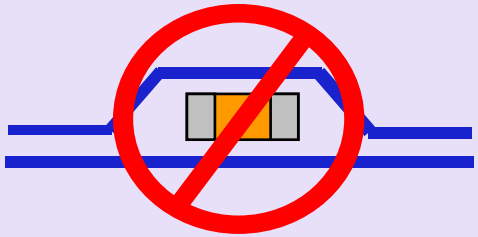
Trace length

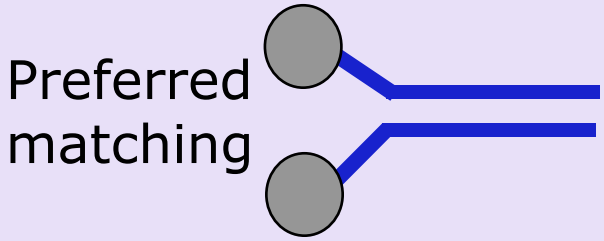
- Longer trace length ⇒ loss ↑
- 0.25 to 0.35 dB inherent loss per inch for FR4 microstrip traces
- Limit motherboard trace to < 12 inches and add-in card trace to < 3 inches

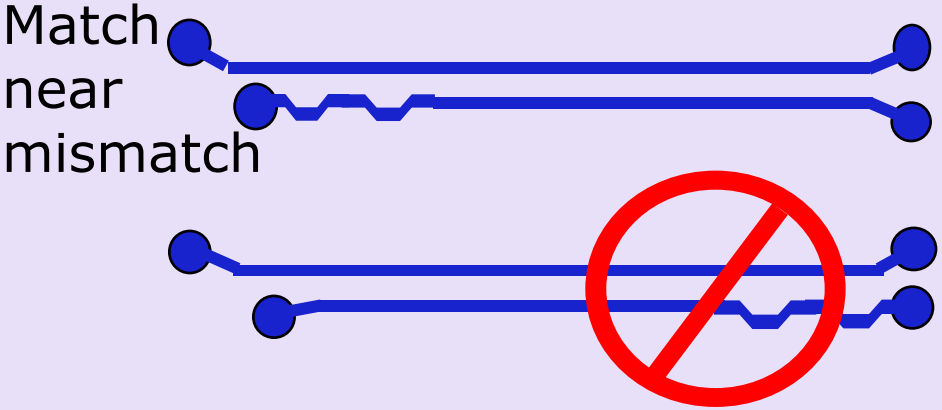


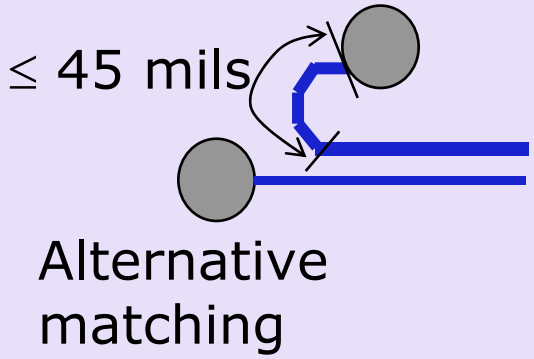
Trace Symmetry & Matching

- Match each differential pair per segment
  - ✓ Match overall length ≤ 5 mils
  - ✓ Symmetric routing for each pair



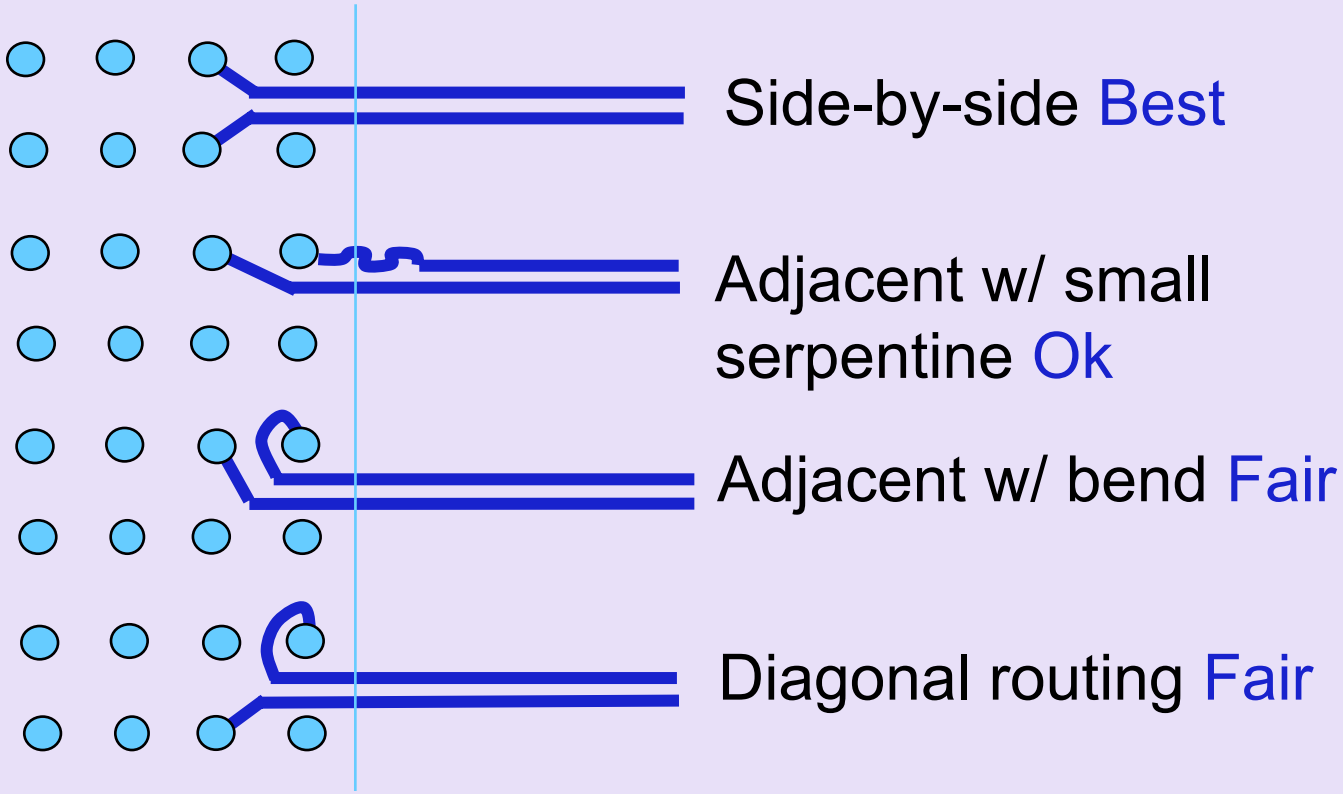






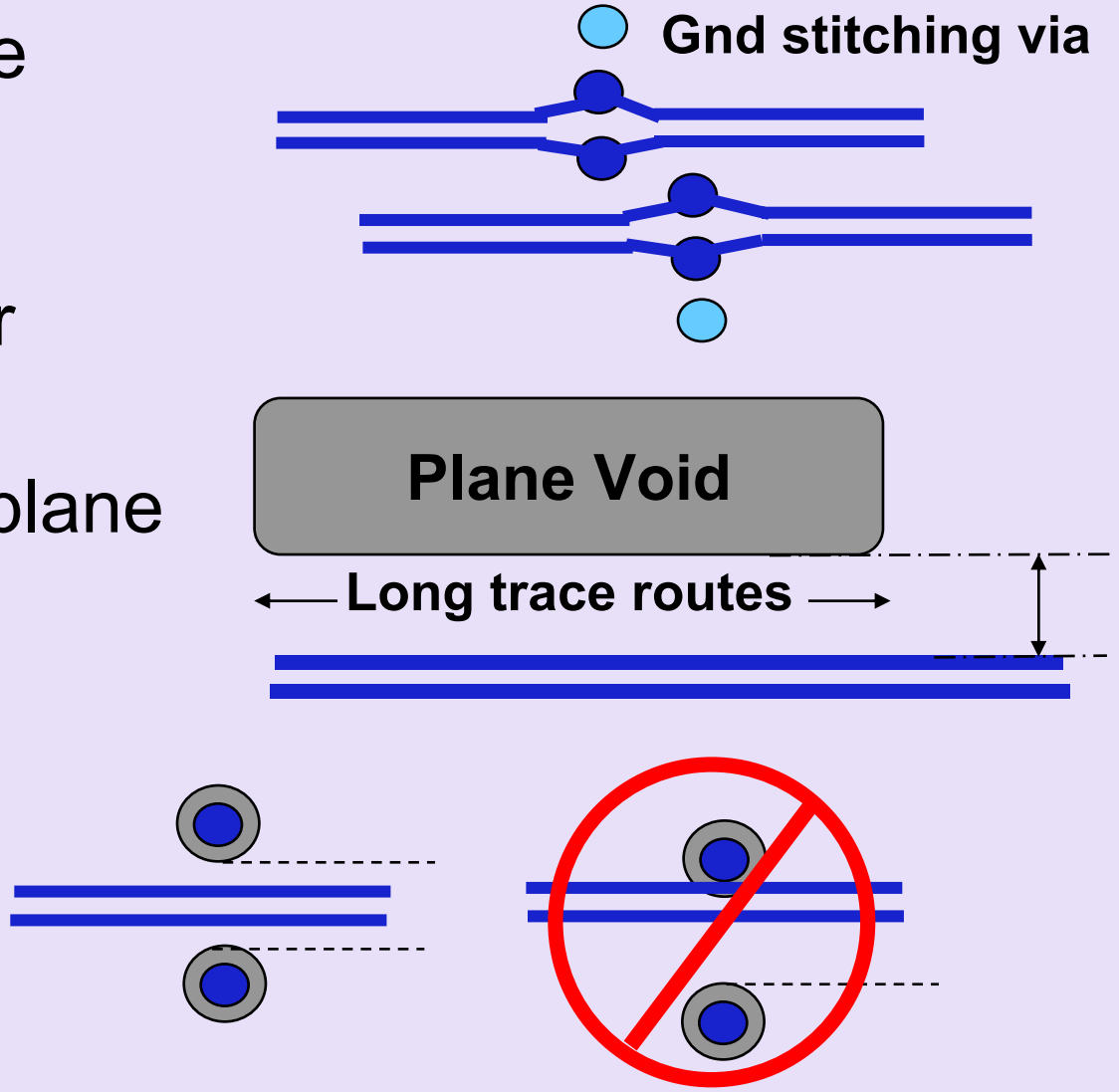
Pin field breakout

- Use side-by-side breakout for package to maintain symmetry
- Avoid tight bends



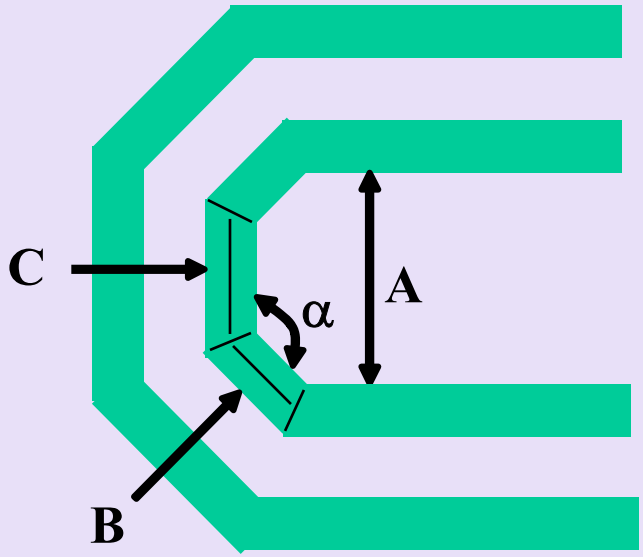
Reference plane

- Full ground plane reference
- Stitching vias required for layer transition
- Clearance near plane void
- Avoid trace over anti-pad



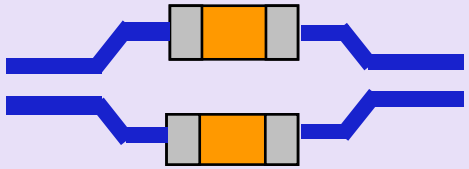
Bend Guidelines

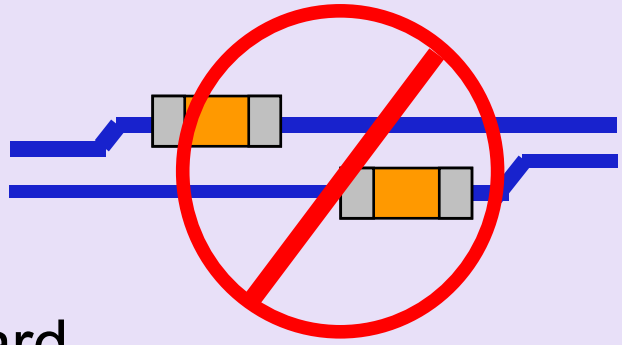
- Avoid tight bends
  - ✓ No 90° bends; impact to loss and jitter budgets
- Keep angles >= 135° (α)
- Keep minimum air gap
  - ✓ A >= 3x the trace width
- Length of B and C >= 1.5x the width of the trace



AC coupling caps

- Size: 0402 best, 0603 ok
- No 0805 size or C-packs
- Symmetric placement

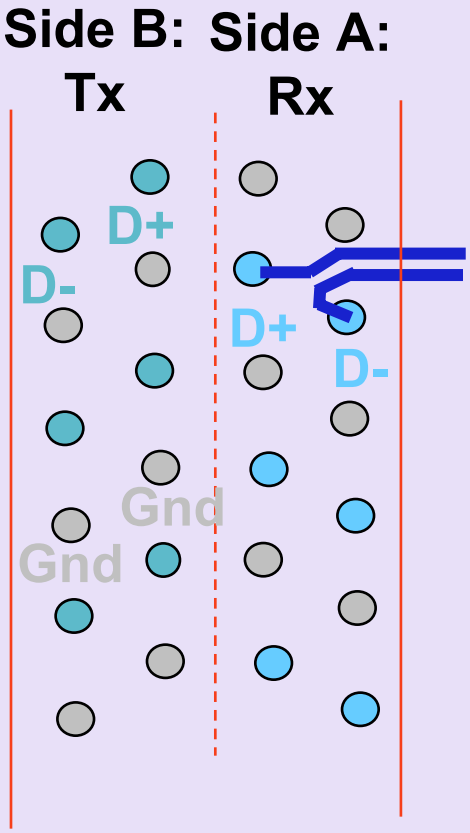




- Cap Size: 0.1uF best
- Cap location:
  - ✓ Along Tx pairs on Motherboard
  - ✓ Along Tx pairs on Add-in card

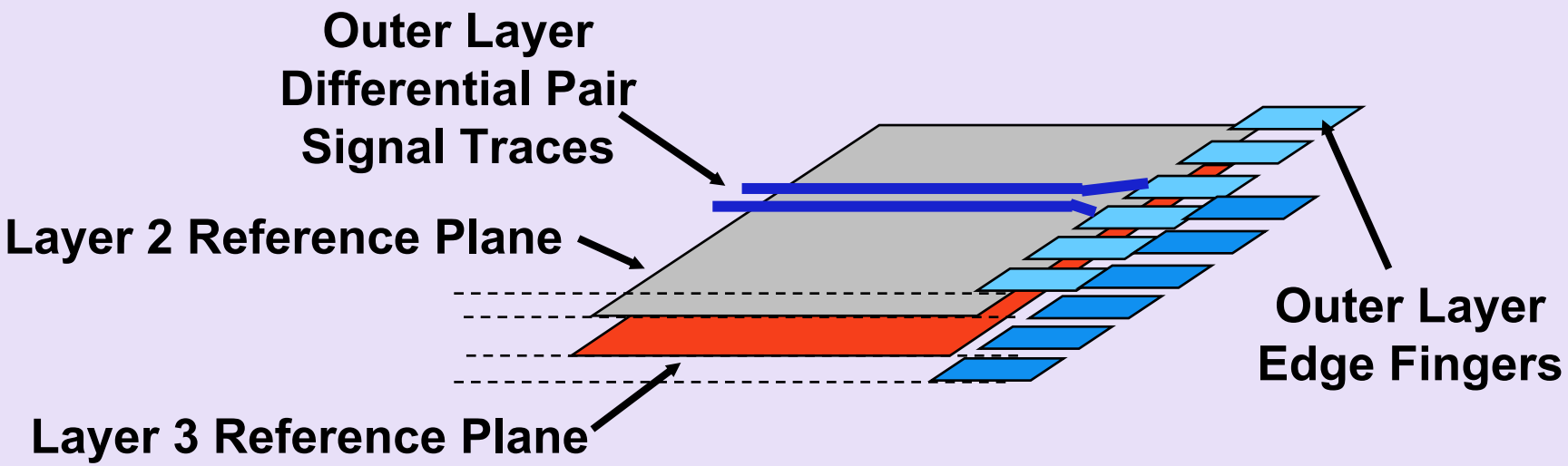
Connectors

- New connector with standard PTH
- Pinout optimized for differential routing
- Loss & crosstalk part of baseboard budget
- Connector sizes: x1, x4, x8, x16



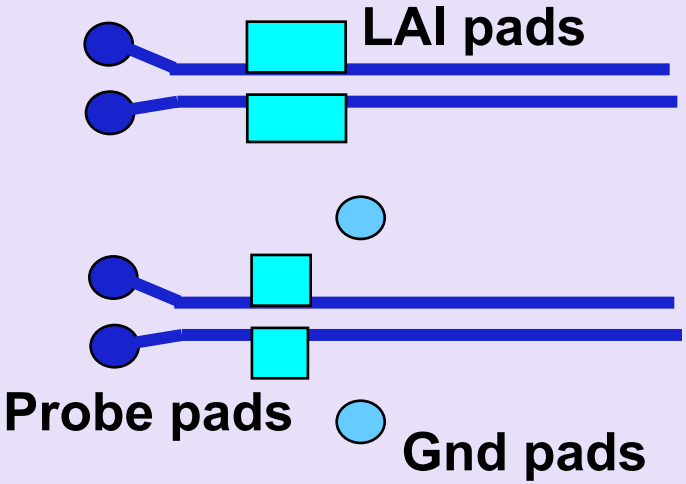
Card edge fingers

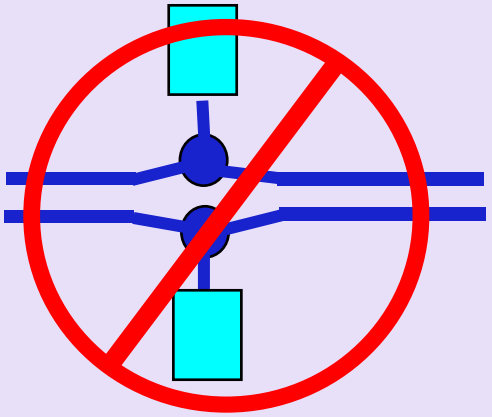
- Remove ref plane under edge fingers pads
  - ✓ For better impedance/loss performance



Test points & Vias

- Minimize Vias usage
  - ✓ Up to 0.25 dB loss per via
  - ✓ Via pad size ≤ 25 mil, hole size ≤ 14 mil
- Put test points or LAI pads in series
  - ✓ No stubs
  - ✓ Provide Gnd pads for single-ended probing





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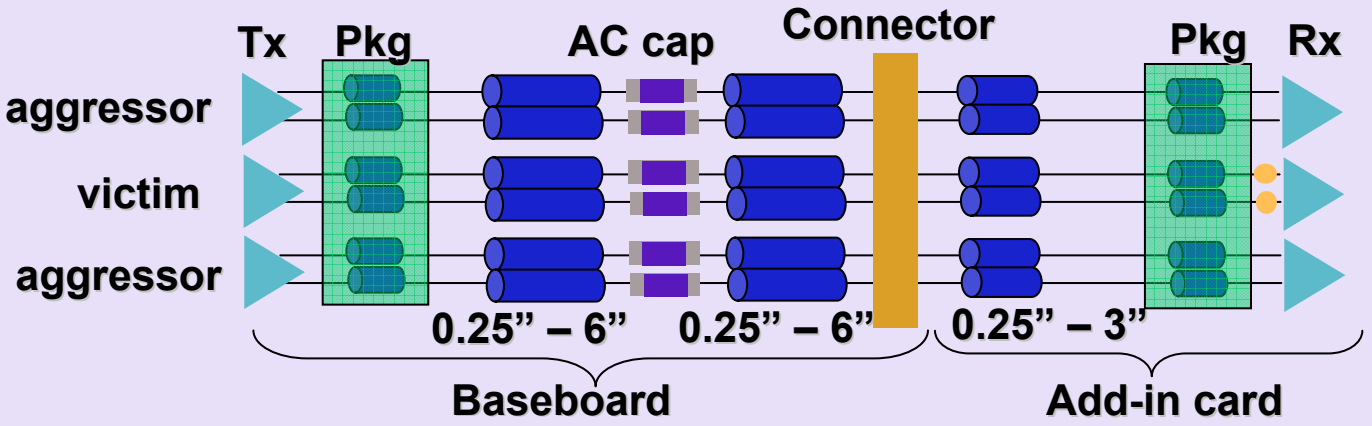
Simulations

- Simulations to maximize board solution space
  - ✓ Simulation analysis using HSPICE, etc
  - ✓ Dielectric and conductor loss must be modeled
- Simulate spec parameters
  - ✓ Compliance Eye (Loss/Jitter)
  - ✓ AC & DC common mode
  - ✓ Return Loss (for buffer/package)
- Models
  - ✓ Buffer, package, PCB (trace, via), connector
  - ✓ Worst case ref channel

Perform simulations to maximize solution space

Topology & modeling

- Multi-pair (2 aggressors, 1 victim) coupled models

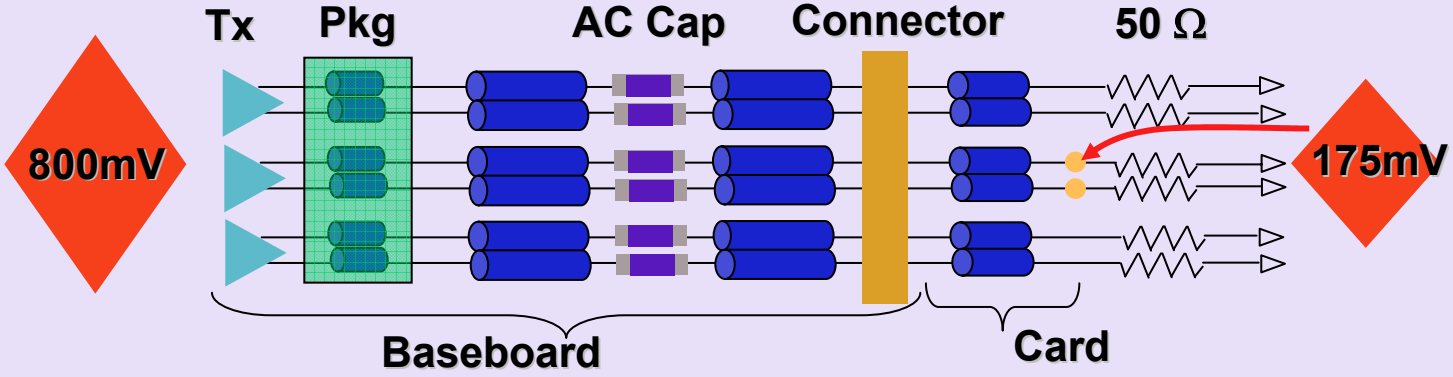


- Corner case PCB: impedance variations and non-homogenous effects
- 8b/10b compliance data pattern in Spec

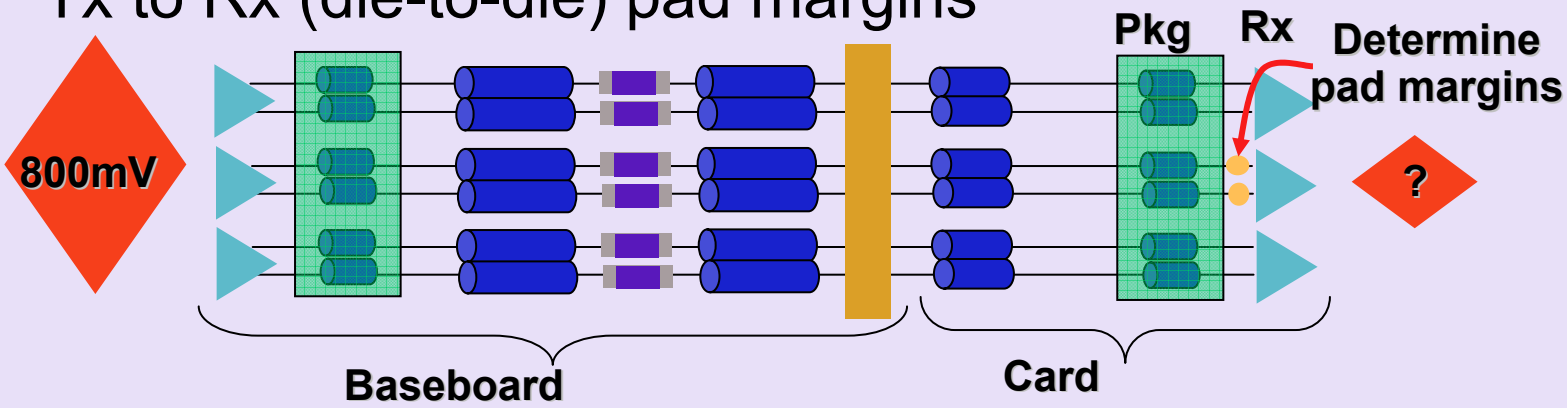
Aggressor	1100000101	0011111010	1100000101	0011111010	1100000101	0011111010
Victim	1100000101	0011111010	1100000101	1100000101	0011111010	1100000101
Aggressor	1100000101	0011111010	1100000101	0011111010	1100000101	0011111010

Spec vs. Product Simulations

- Spec simulations for generic board solution
  - ✓ Tx to 50Ω load ~175mV

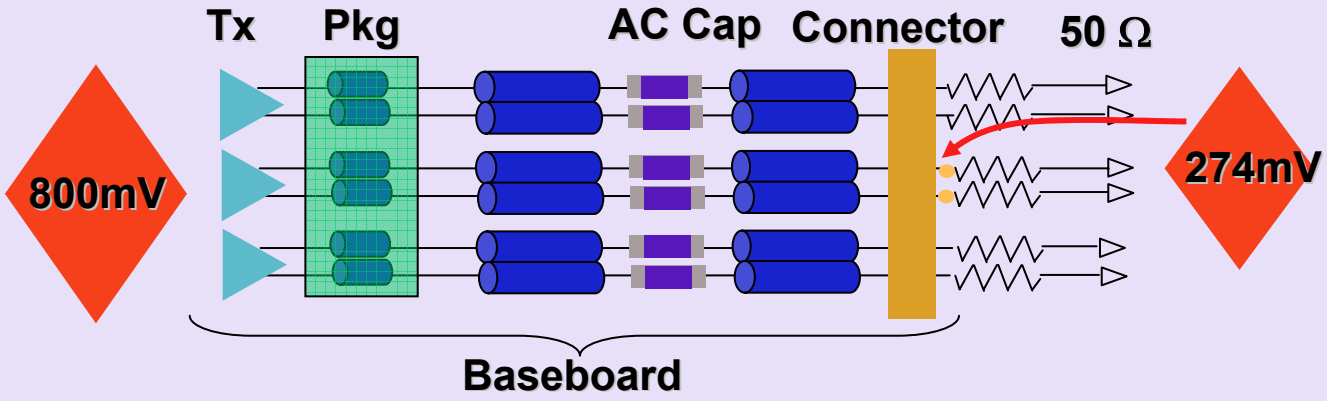


- Product simulations for specific package
  - ✓ Tx to Rx (die-to-die) pad margins

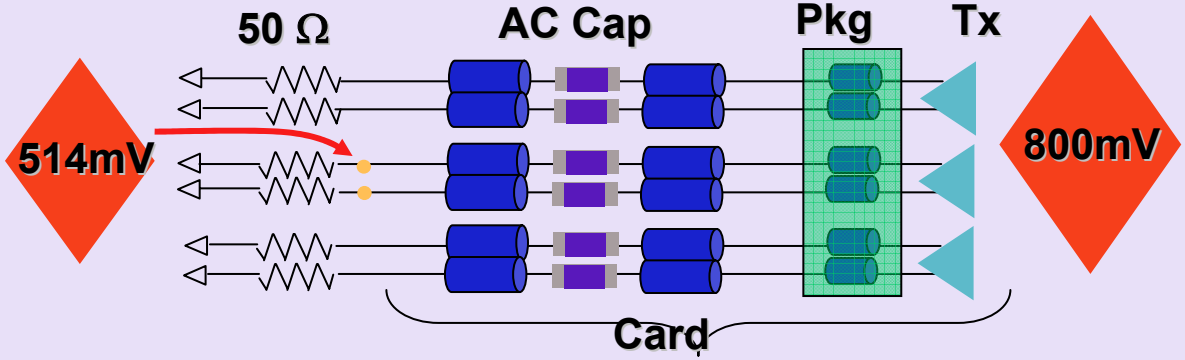


Baseboard vs Card TX Eyes

- CEM Spec for separate Baseboard vs Card budget
  - ✓ Baseboard Tx to 50Ω load

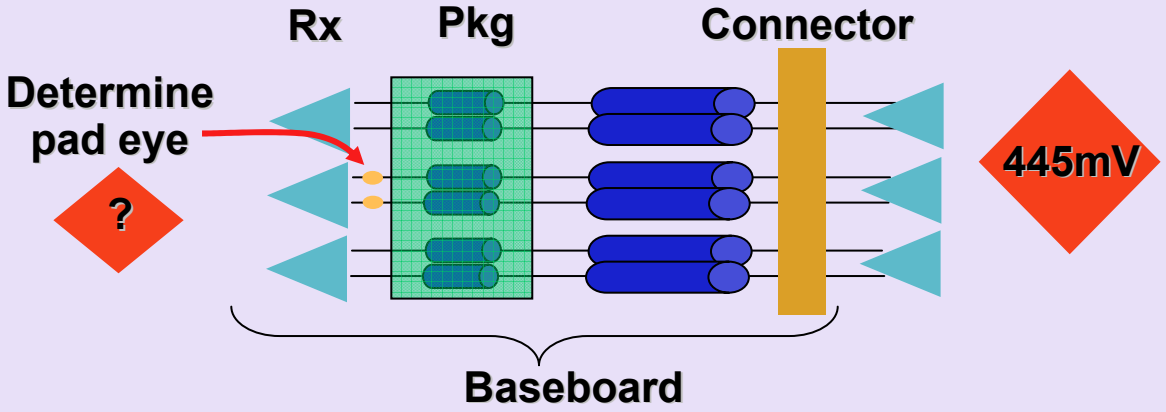


  - ✓ Card Tx to 50Ω load

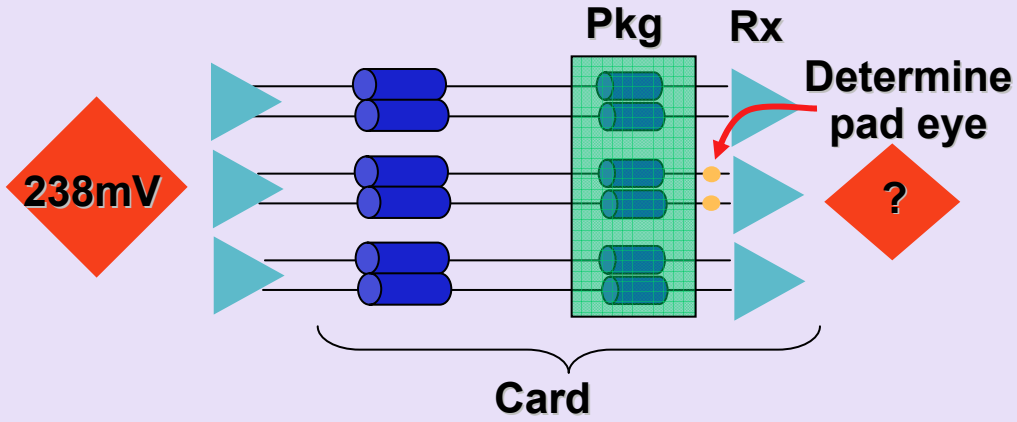


Baseboard vs Card RX Eyes

- CEM Spec defines Baseboard vs Card input requirements
  - ✓ Eye for Baseboard Rx

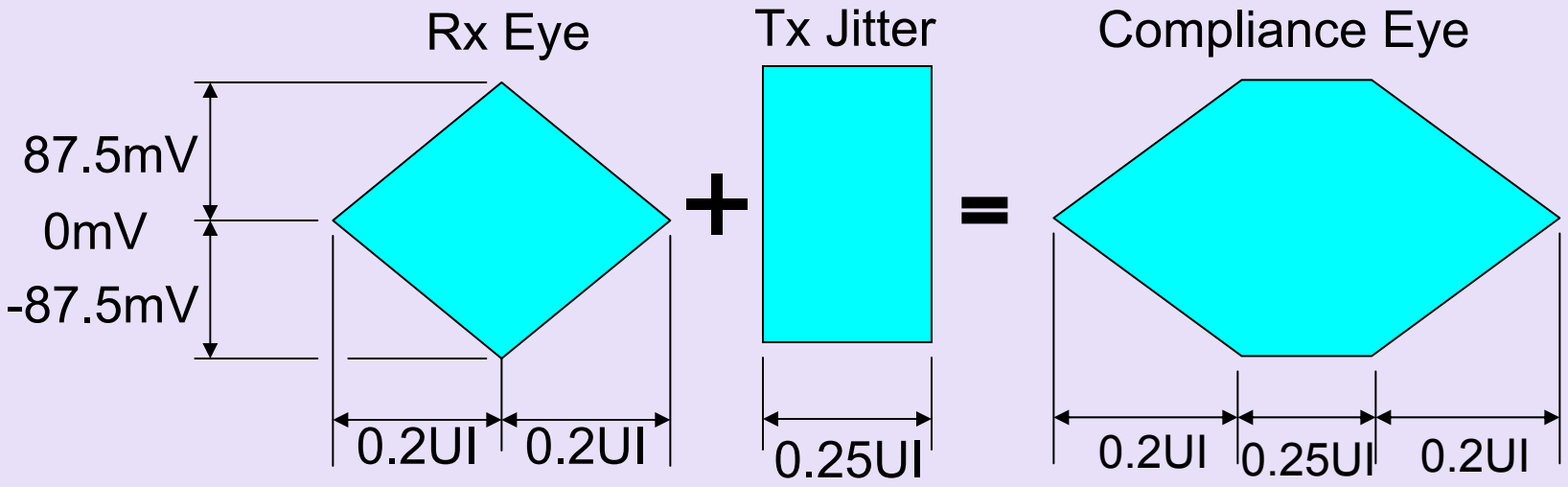


  - ✓ Eye for Card Rx



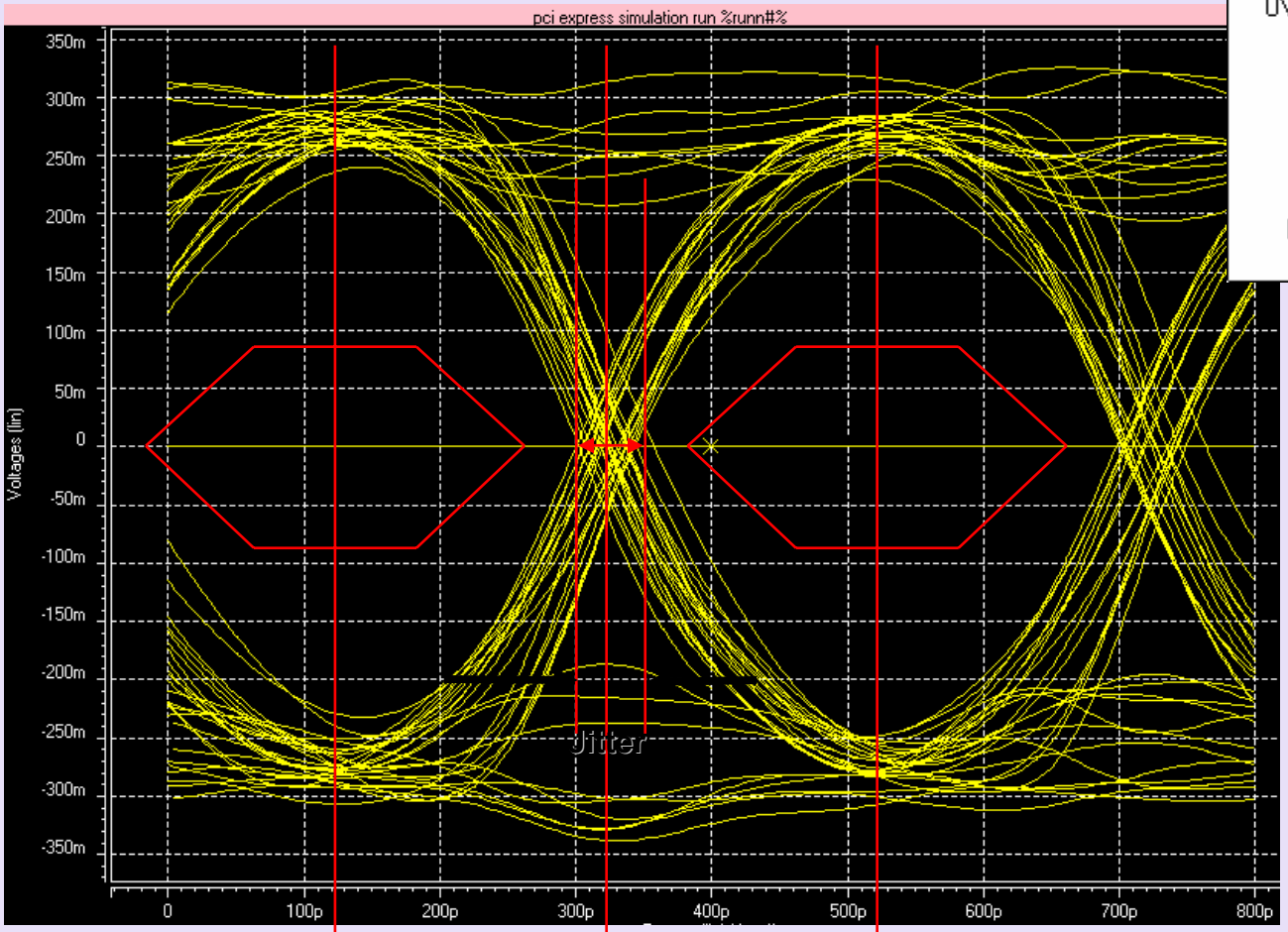
Compliance eye mask

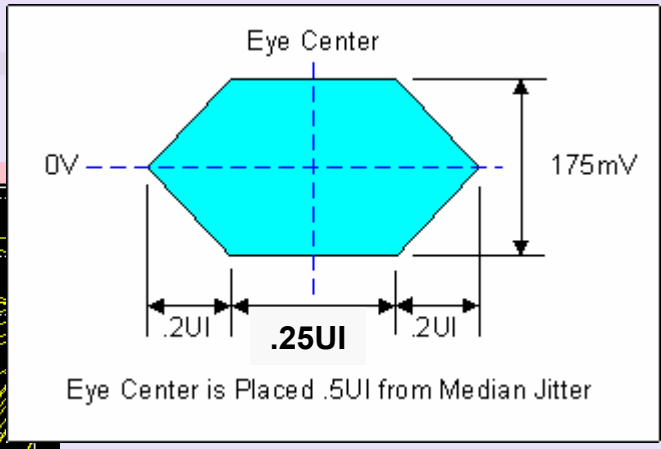
- Must meet compliance eye @ Rx pins
  - ✓ Min Rx eye ⇒ 0.4 UI at 0 mV differential
  - ✓ Min Vdiff-p-p at Rx ⇒ 175 mV
  - ✓ Add any Tx jitter not included in modeling



Data Analysis

- Example eye diagrams at RX pin





Example parameters for worst-case eye:

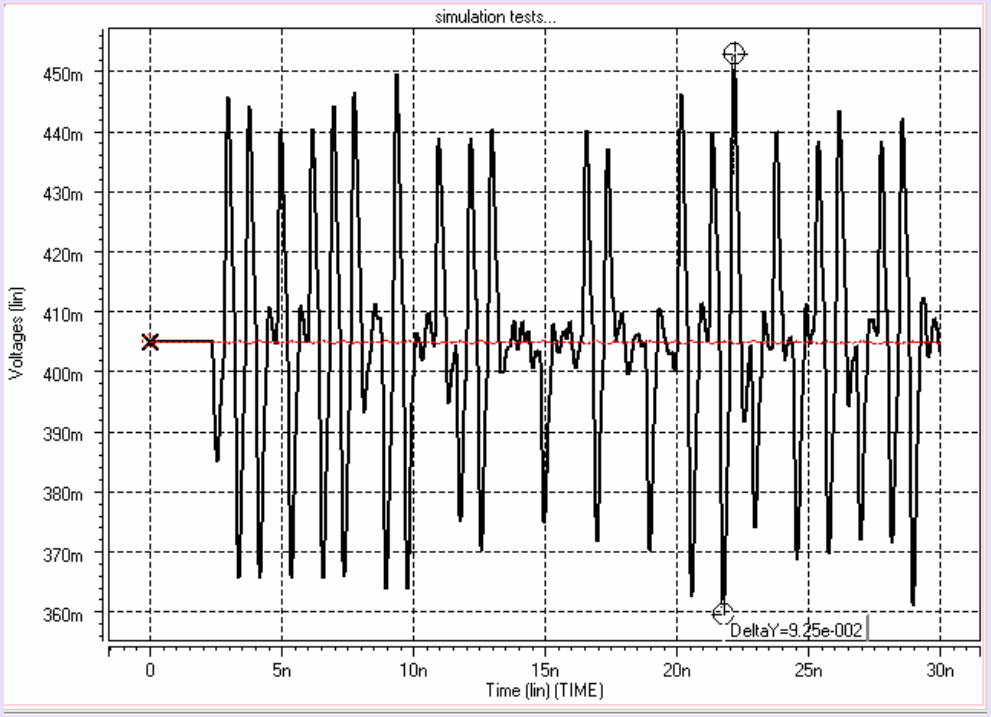
RX cap	= 1.3 pF
TX cap	= 1.3 pF
RX res	= 53
TX res	= 53
MB length	= 12" (with 250mil BO)
Card length	= 4" (with 250mil BO)
AC cap	= 200 nF
MB Zo	= High ~113 diff Z
Card Zo	= High ~113 diff Z
De-emph	= 3 dB
Swing	= 800 mV
Edge rate	= slow
Vias	= 6

Driving direction = card Tx, MB Rx

30% guard band for AC common mode (for fiber weave effects)
20% guard band otherwise

AC common mode

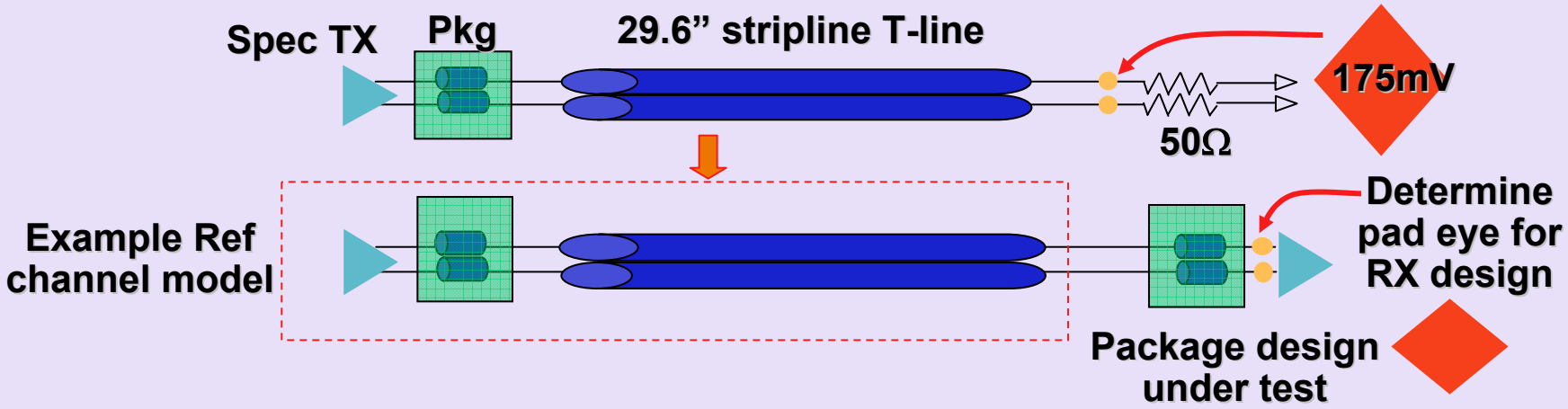
- Max AC common mode @ Rx < 150 mV peak
  - ✓ $V_{AC\text{-}cm} = |V_{D+} + V_{D-}| \div 2 - V_{DC\text{-}cm}$
  - ✓ $V_{DC\text{-}cm}$ = DC(avg) of $| V_{D+} + V_{D-}| \div 2$



Example: 50 mV peak

Ref channel for RX simulations

- Return Loss spec is **not** sufficient to guarantee RX operability
- Use Ref channel model for RX simulations
  - ✓ Calibrate T-line with ~13.2dB loss to 175mV at 50Ω load
  - ✓ Use Spec TX (800mV swing, -3.5dB de-emphasis, 0.3UI TX jitter)



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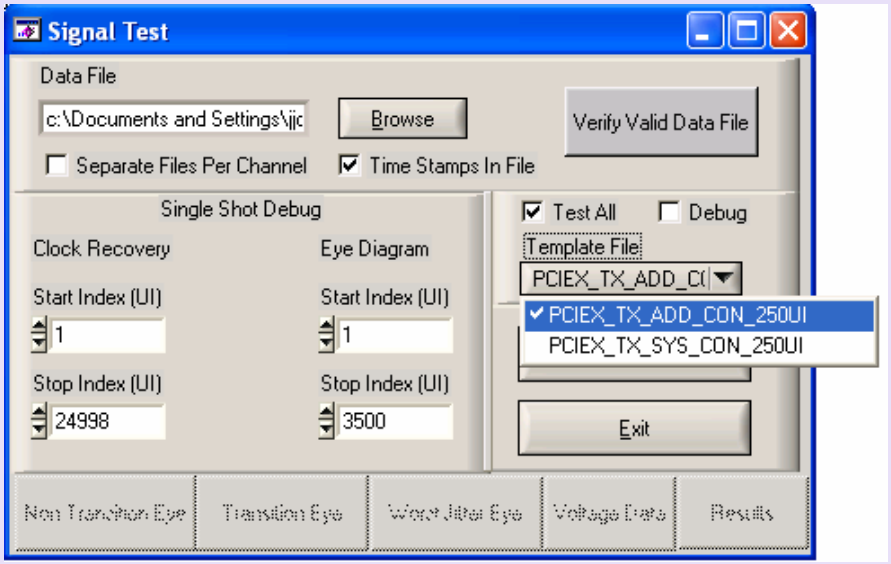
Signal measurement

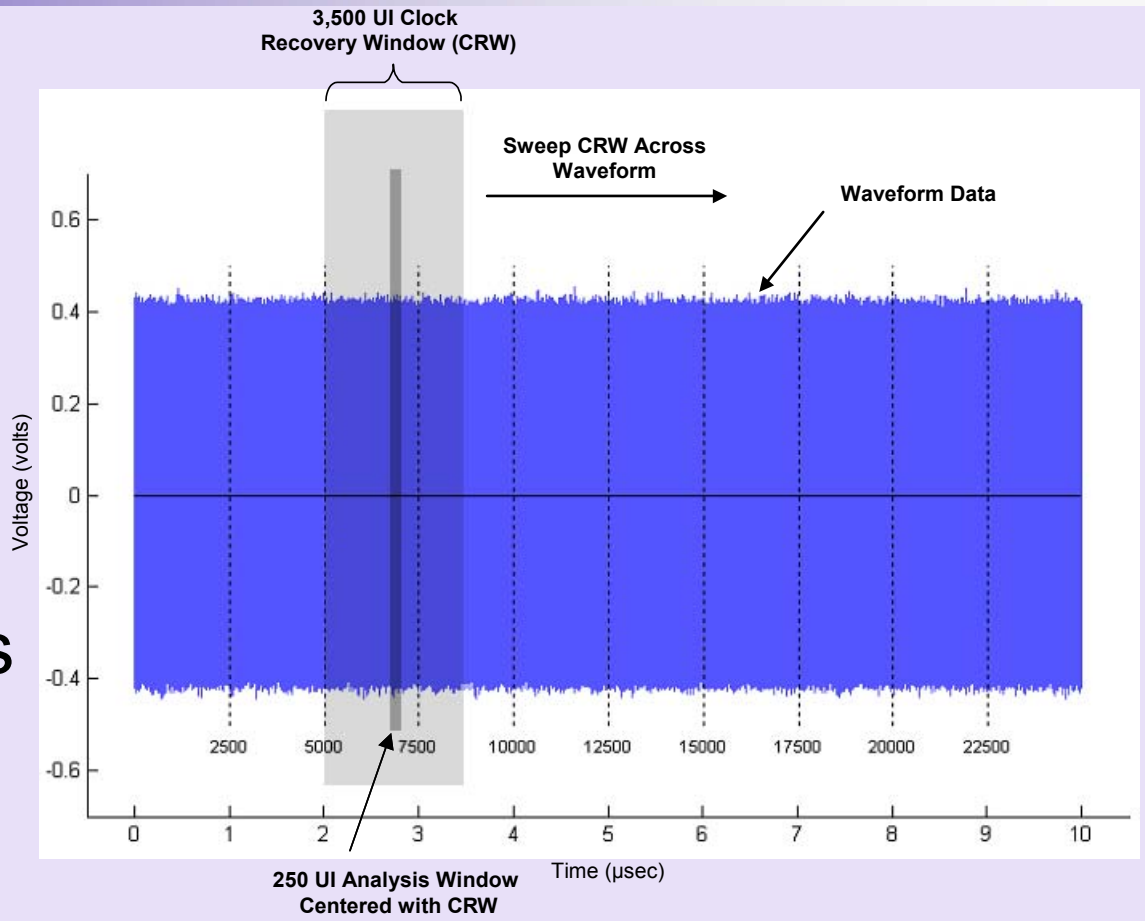
- Generate compliance pattern per Spec
- Probe with real time scope (> 6 GHz analog bandwidth, > 20 G sampling)
- Scope post-processing software for Compliance Eye diagram analysis



Validate compliance eye diagram using scope

1.0a Analysis Methodology

- Average UI recovered from 3500 UI
- Voltage margin & Jitter analysis across 250 UI
- Repeat analysis by sweeping in 100 UI increments across entire acquisition
- AC Common Mode is reported for the entire acquisition



New Clock Recovery For Eye Measurement (rev 1.1)

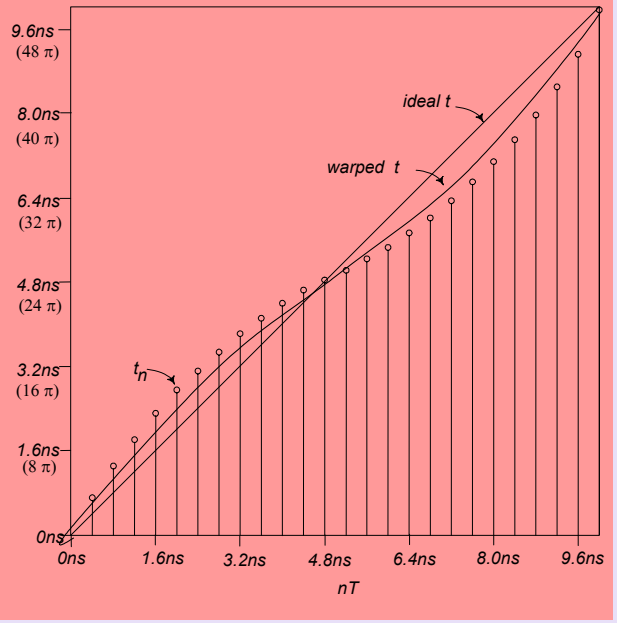
- The estimate of the ideal clock, T, in the phase jitter is the clock recovery

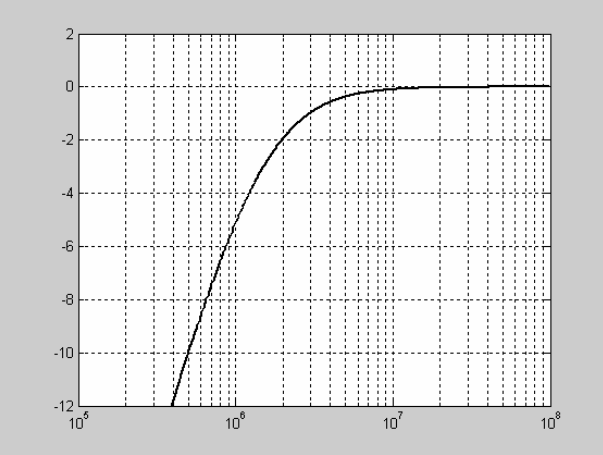
$$\Phi_n = t_n - nT, \quad n = 1, 2, \ldots, \infty$$

- Recovery can be done in T or in Φ
  - ✓ Matlab code in jitter whitepaper that applies it in $\Phi(s)$
  - ✓ It can also be done as a sliding window using average T and looking across 416 UI

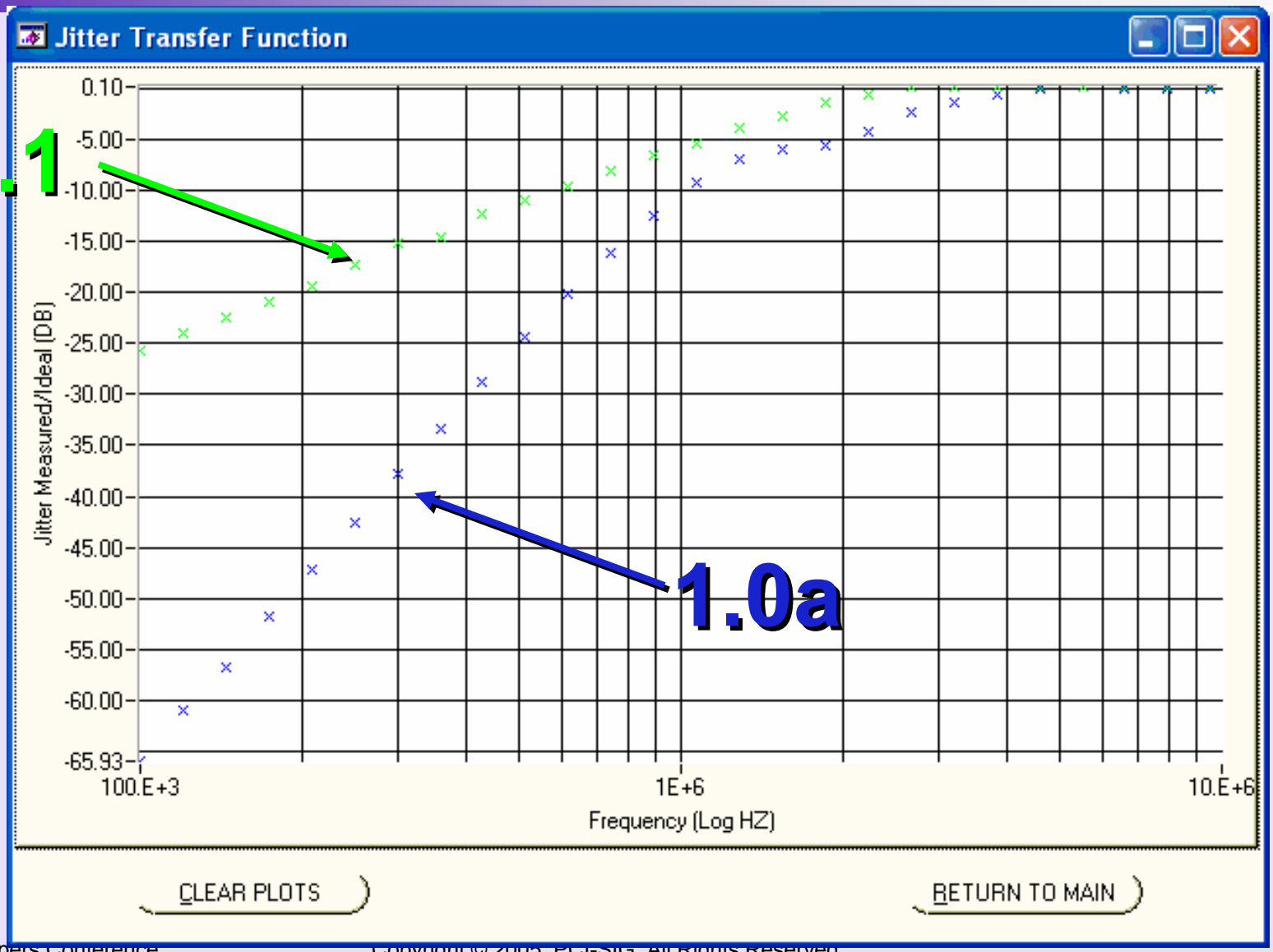
$$H_3(s) = \frac{s}{s + 2 * \pi * 1.5e6}$$

- This implies the minimum required performance of the data recovery circuit (DRC)



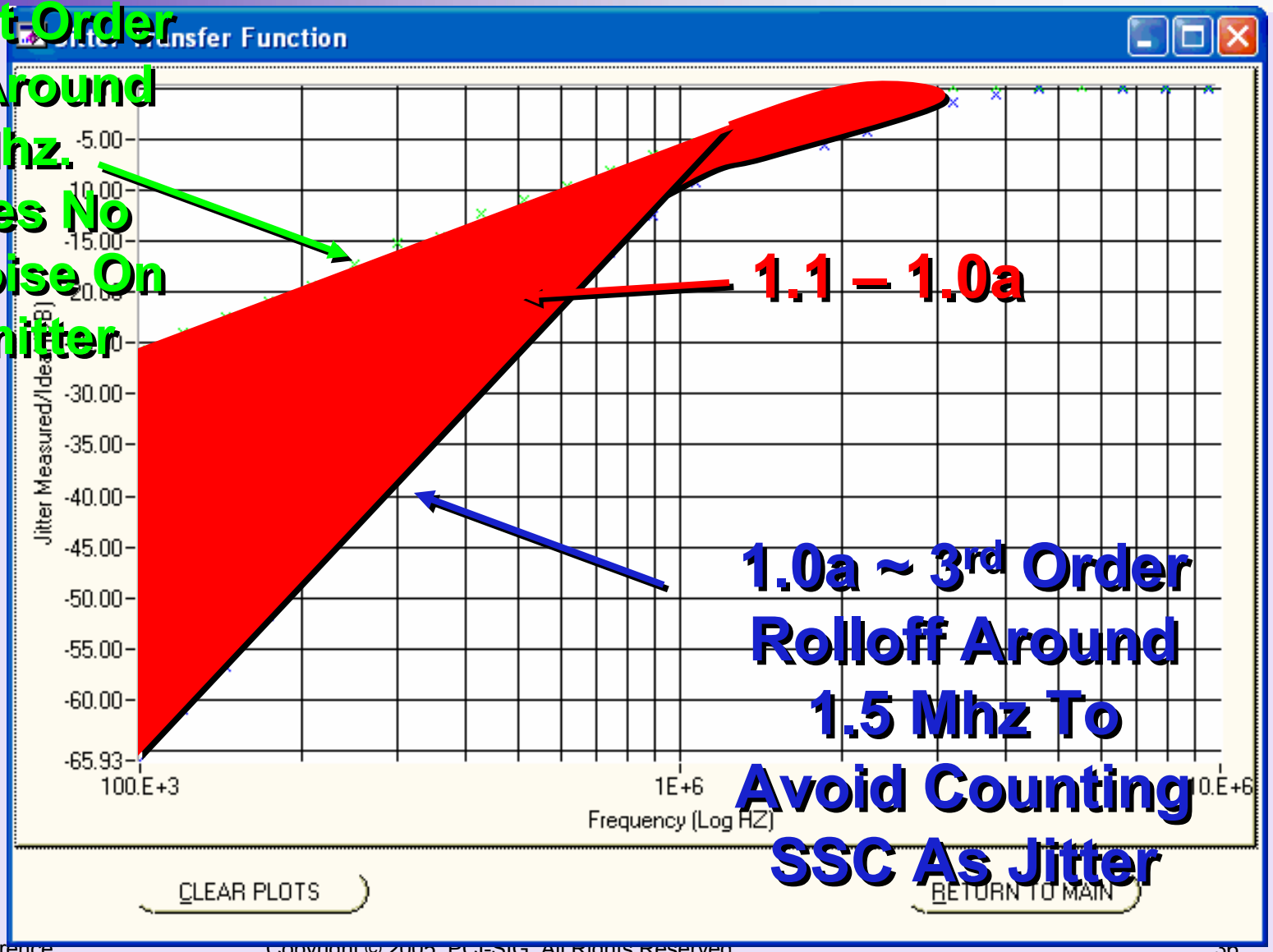


Frequency Response – 1.0a/1.1



Response Delta – 1.0a/1.1

1.1 ~ First Order Rolloff Around 1.5 Mhz. Assumes No Clock Noise On Transmitter



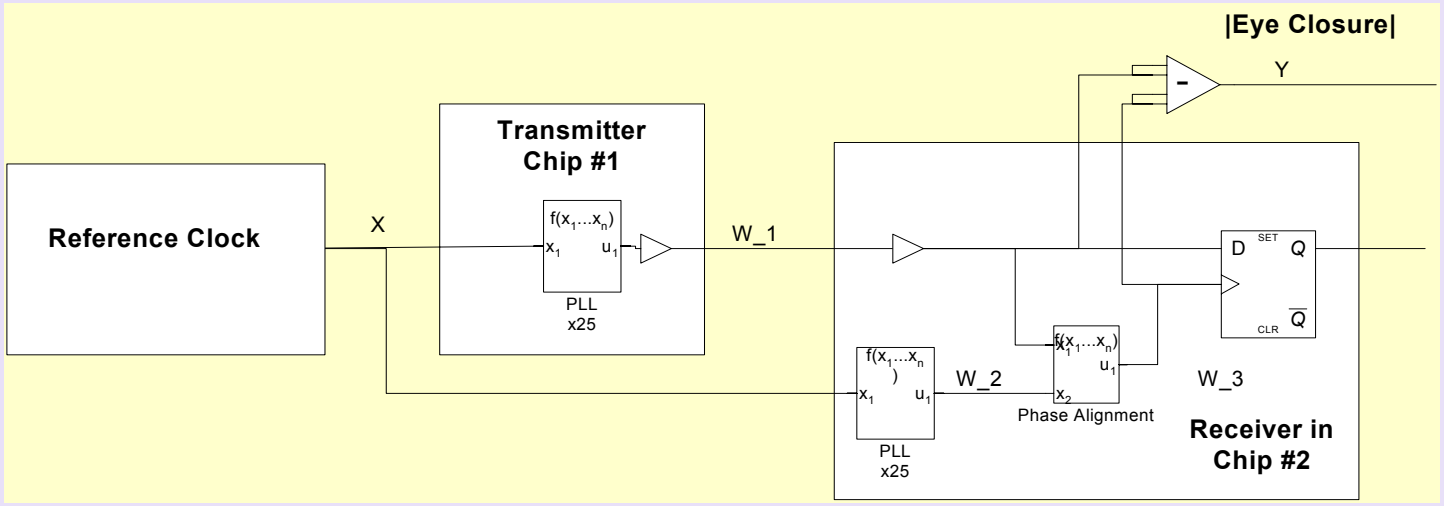
1.1 – 1.0a

1.0a ~ 3rd Order Rolloff Around 1.5 Mhz To Avoid Counting SSC As Jitter

Tx PLL Bandwidth Restrictions

- Tx PLL bandwidth is between 1.5 and 22 MHz, peaking < 3dB
  - ✓ Based on second order transfer function

- Rx is implementation specific



Tx Eye Reduction

- Tx reduction from 120 ps to 100 ps
  - ✓ At 10^-12 BER
- Eye measurements are to be done with a “clean” clock
- The median to max measurement is over 1e6 samples using the compliance pattern

CEM System Budget

- Minimum Rj assumptions have been taken for the Tx, reference clock and the “Internals” of the Rx
- These Rj terms are convolved to achieve the total system budget
- This is then extrapolated to 10^-6 for the CEM and compliance numbers

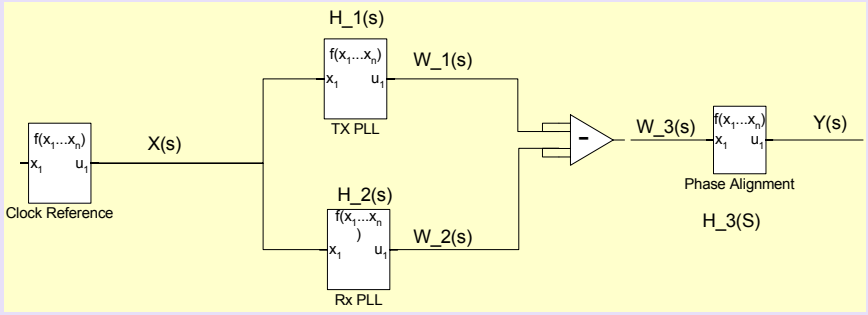
Jitter Contribution	Min Rj (ps) one sigma	Max Dj (ps) P-P	Tj at BER 10^{-12} (ps)	Tj at BER 10^{-6} (ps)
Tx	**2.8**	**60.6**	**100**	**87**
Ref Clock	**4.7**	**41.9**	**108**	**86**
Media	**0**	**90**	**90**	**90**
Rx	**2.8**	**120.6**	**160**	**147**
Linear Total Tj:			**458**	**410**
Root Sum Square (RSS) Total Tj:			**399.13**	**371.52**

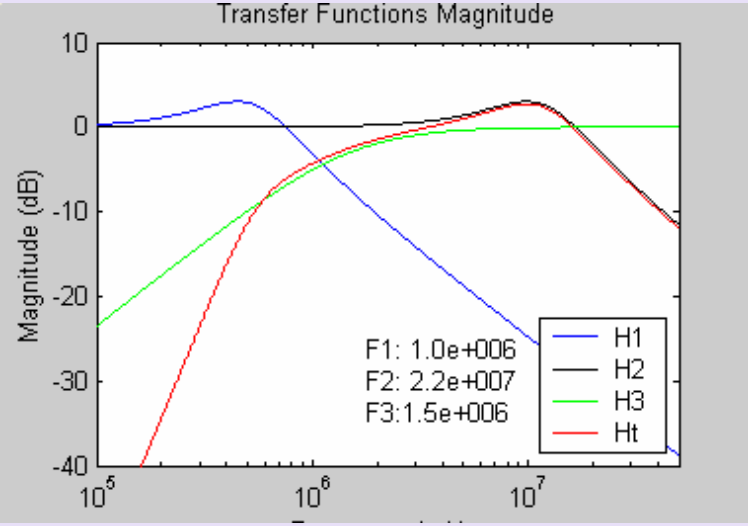
New CEM Jitter Budgets At Connectors (TJ at 10^12 bits)

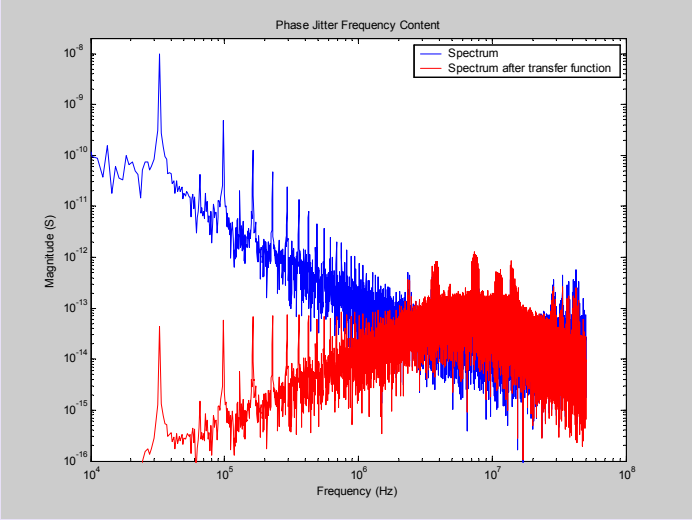
	System Connector Jitter Limit (PP)	Add In Card Edge Fingers Jitter Limit (PP)
1.0a	**217**	**163**
1.1	**167**	**126**

Reference Clock Specification

- The reference clock phase jitter is less than 86 ps
  - ✓ After the (H1 – H2) * H3 transfer function has been applied
  - ✓ H1 = 1.5, H2 = 22, second order
    - 3 dB peaking
  - ✓ H3 = 1.5 MHz, first order
  - ✓ Delay of 10 ns added to H1 for transport delay







Reference Clock Jitter Algorithm

- Produce Interval Array
- Perform FFT Of Intervals
  - ✓ FFT Removes DC Offset
  - ✓ Effectively Removes Average Interval
- Apply Jitter Transfer Function In Frequency Domain
- Perform Inverse FFT
  - ✓ Data Is Now Interval Deltas From Average Interval After Frequency Transformation (Data)
- Integrate Data
  - ✓ $IntData_n = IntData_{n-1} + Data_n$
- Peak Peak Jitter
  - ✓ Max (IntData) – Min (IntData)

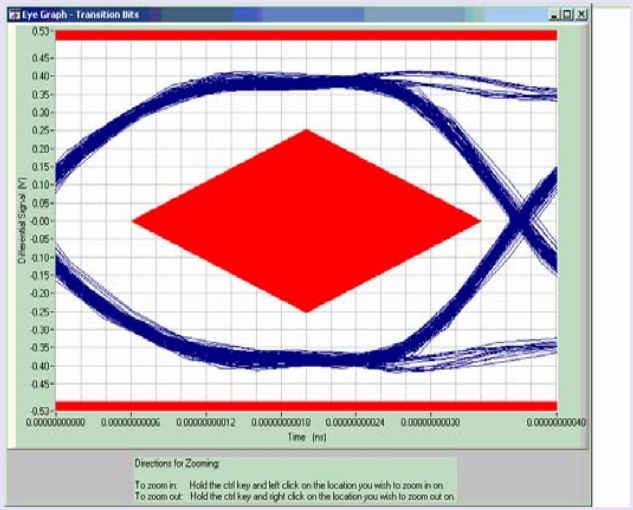
Method Can Also Be Used For Transmitter Data With Small Changes

BER/Jitter Summary

- The Tx specification is to be made with a clean clock
- The Tx bandwidth range and peaking is limited
- The reference clock phase jitter is limited
- The total system budget includes the convolution of Rj

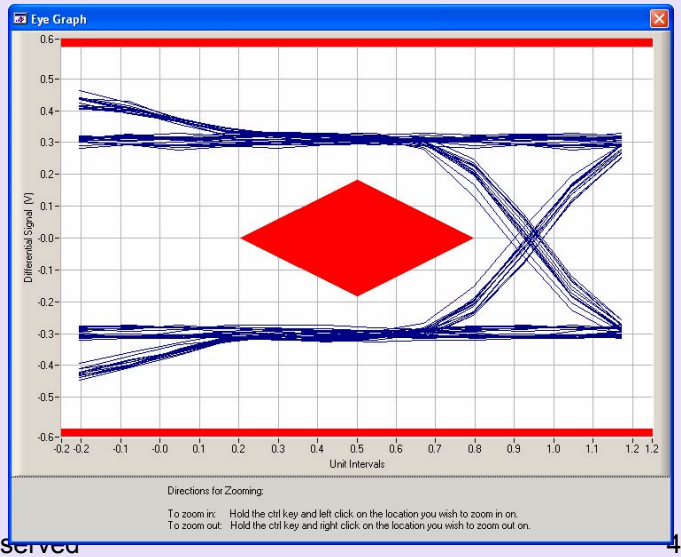
Interpretation of Results

- Scope post-processing software
  - ✓ Transition Eye
  - ✓ De-emphasized Eye
  - ✓ Max jitter
  - ✓ Min Eye voltage margin
  - ✓ AC Common mode
- Probe locations
  - ✓ Tx output at 50Ω load
  - ✓ Rx pin



Example transition bit Eye

Example de-emphasized bit Eye



Summary

- PCI Express point-to-point layout is straightforward
- Manage loss and symmetry in PCB to meet interconnect budget
- Follow basic layout rules and design tradeoffs to implement typical topologies
- Perform simulations to maximize solution space for complex topologies
- Validate compliance eye diagrams using real time scope

Collateral

- Whitepaper and other technical collateral available from the Intel Developer Network for PCI Express* Architecture
  - ✓ http://developer.intel.com/
- Where attendees get additional and updated information
  - ✓ http://www.pcisig.org

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