PCI Express® Cabling Updates

Lee Mohrmann
External Cable Workgroup Chair
National Instruments

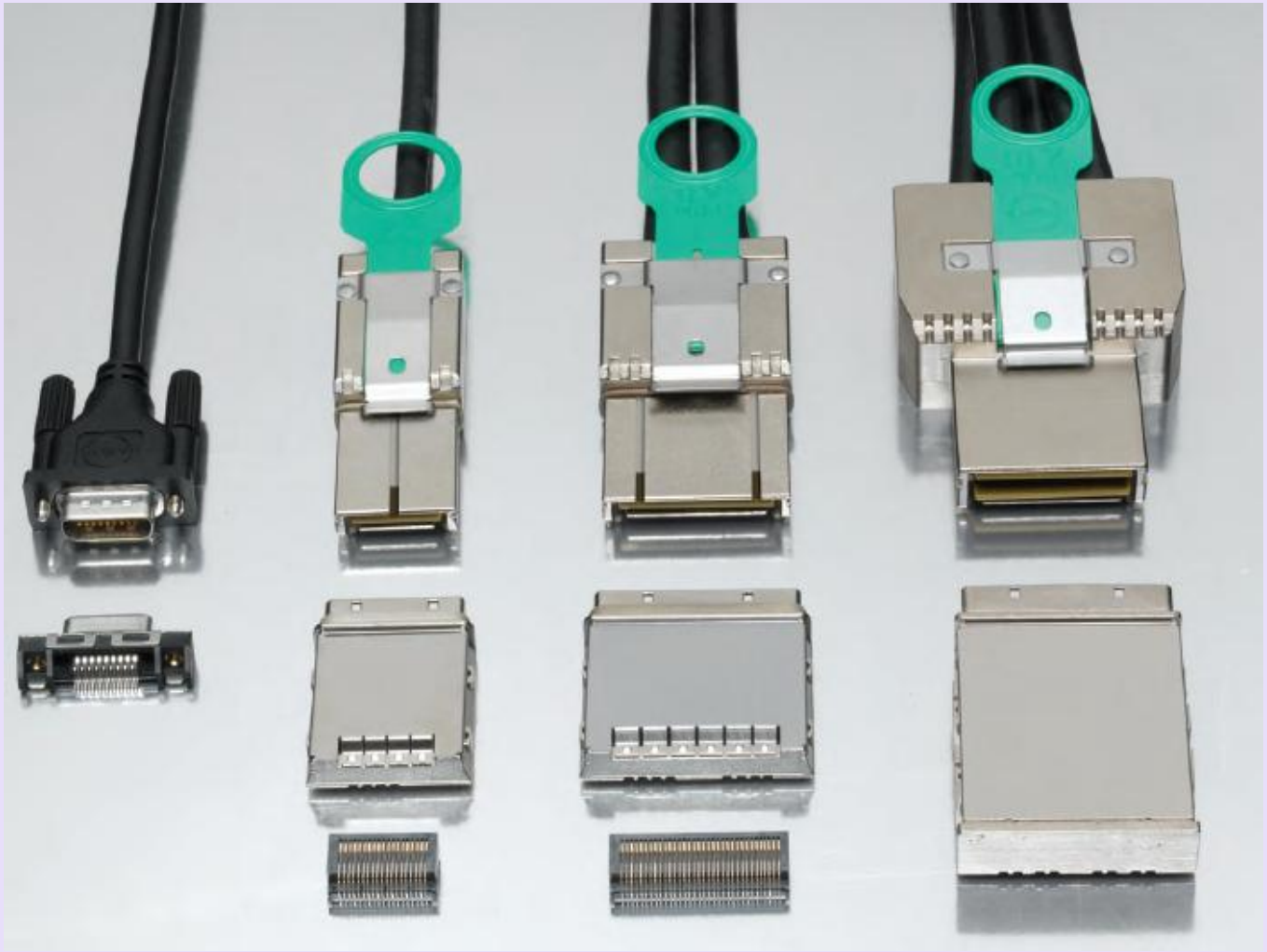
Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

Current Cabling Status

- 1.0 Specification released Jan 2007
- 2.0 Specification releases Q3 2012 (estimated)
- 3.0 Specification working on SOA Q2 2012

PCI Express® External Cable Connectors

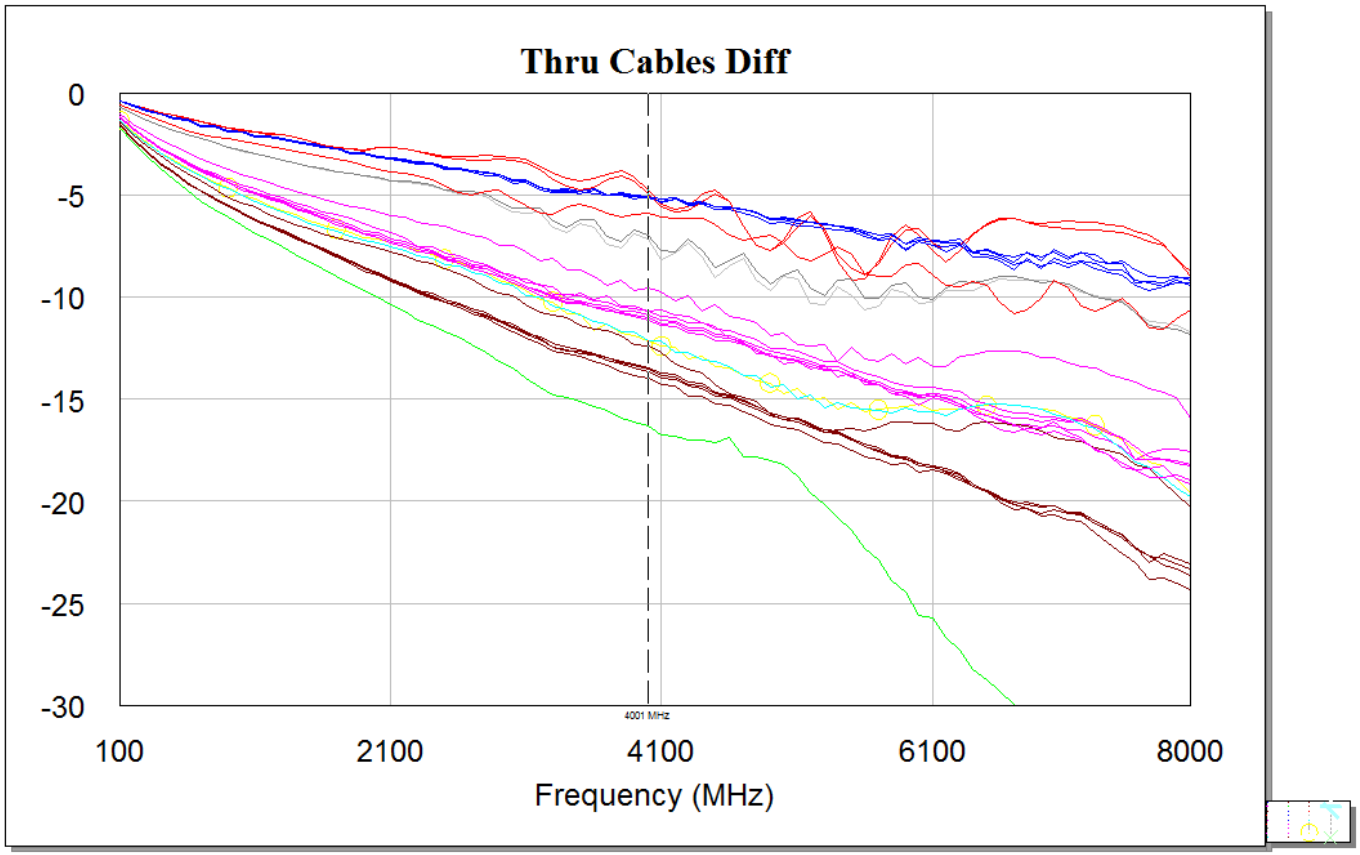


x1 x4 x8 x16

Challenges for PCIe® 3.0

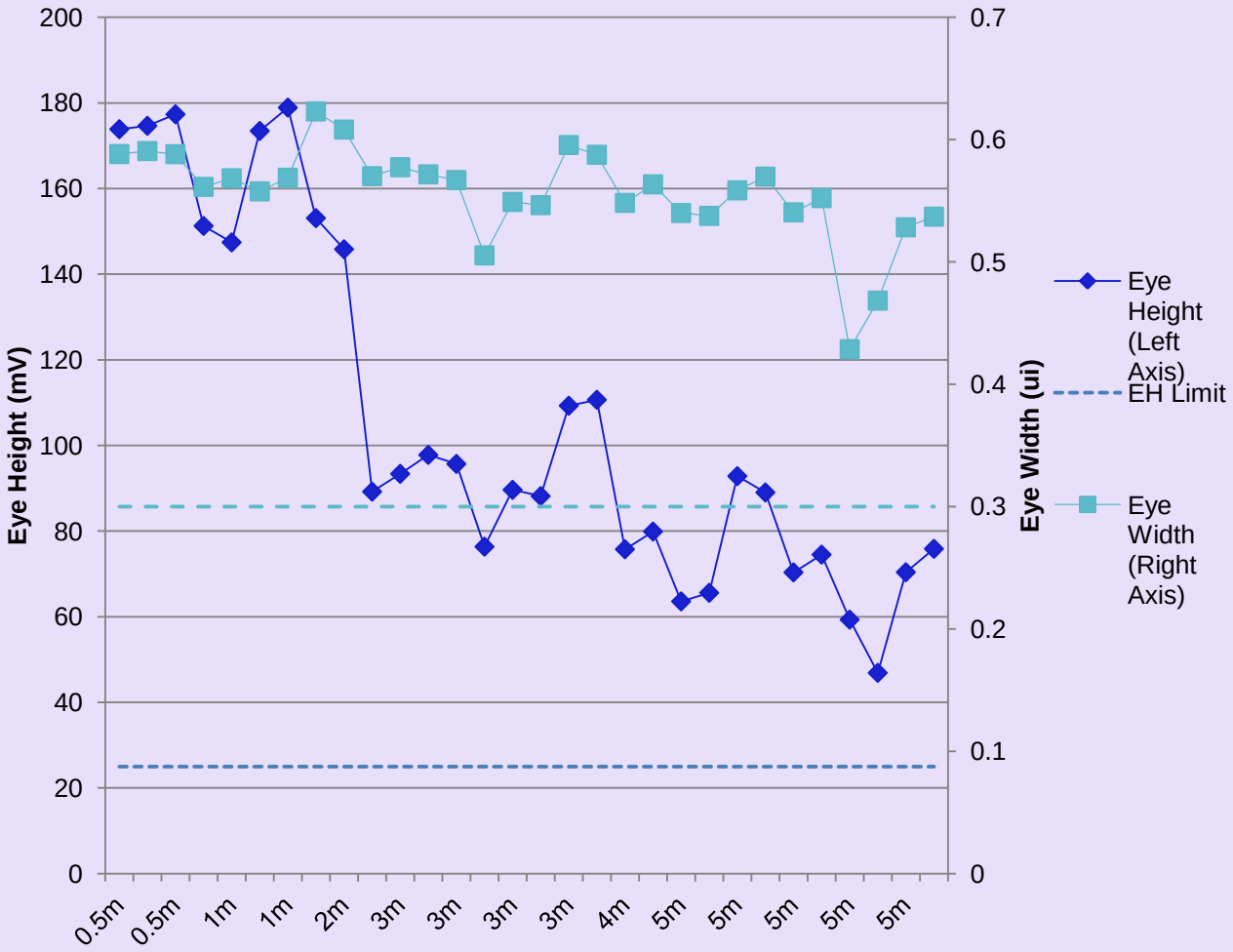
- Other than 8GT/s…
- Clocking
- Equalization
- Optics
- Compatibility

Cable Losses



The spread of cable losses and board losses make a single setting for the equalizaton preset hints unlikely.

Preliminary Simulation Results



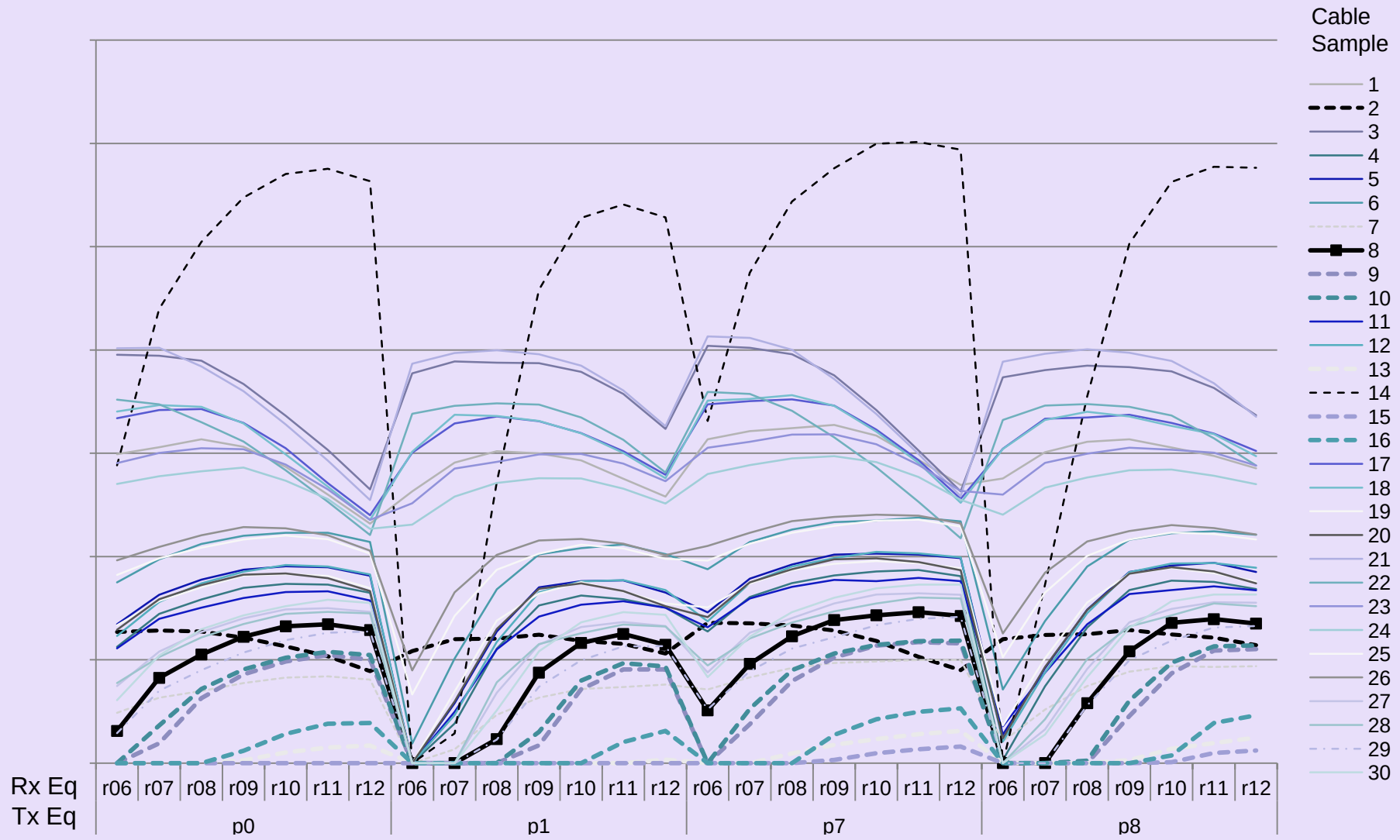
Results indicate that passive cable lengths beyond 3m are possible.

More work needs to be done, these do not include crosstalk.

Link Equalization Settings

- PCIe 3.0 cable needs presets to be able to establish minimal link to begin equalization negotiation
  - ✓ 4 phase process, beginning during PCIe 1.0 operation
    - First phase includes sending presets over the link to begin 8GT/s link operation at low BER. This value determined by system/board level designer during validation and programmed into device.
- Cable links have no pre-knowledge of system losses to set this preset hint
  - ✓ Preset may be too much or too little for any given cable to establish reliable link at 8GT/s

Link Training for PCIe 3.0 Overall Graph Data

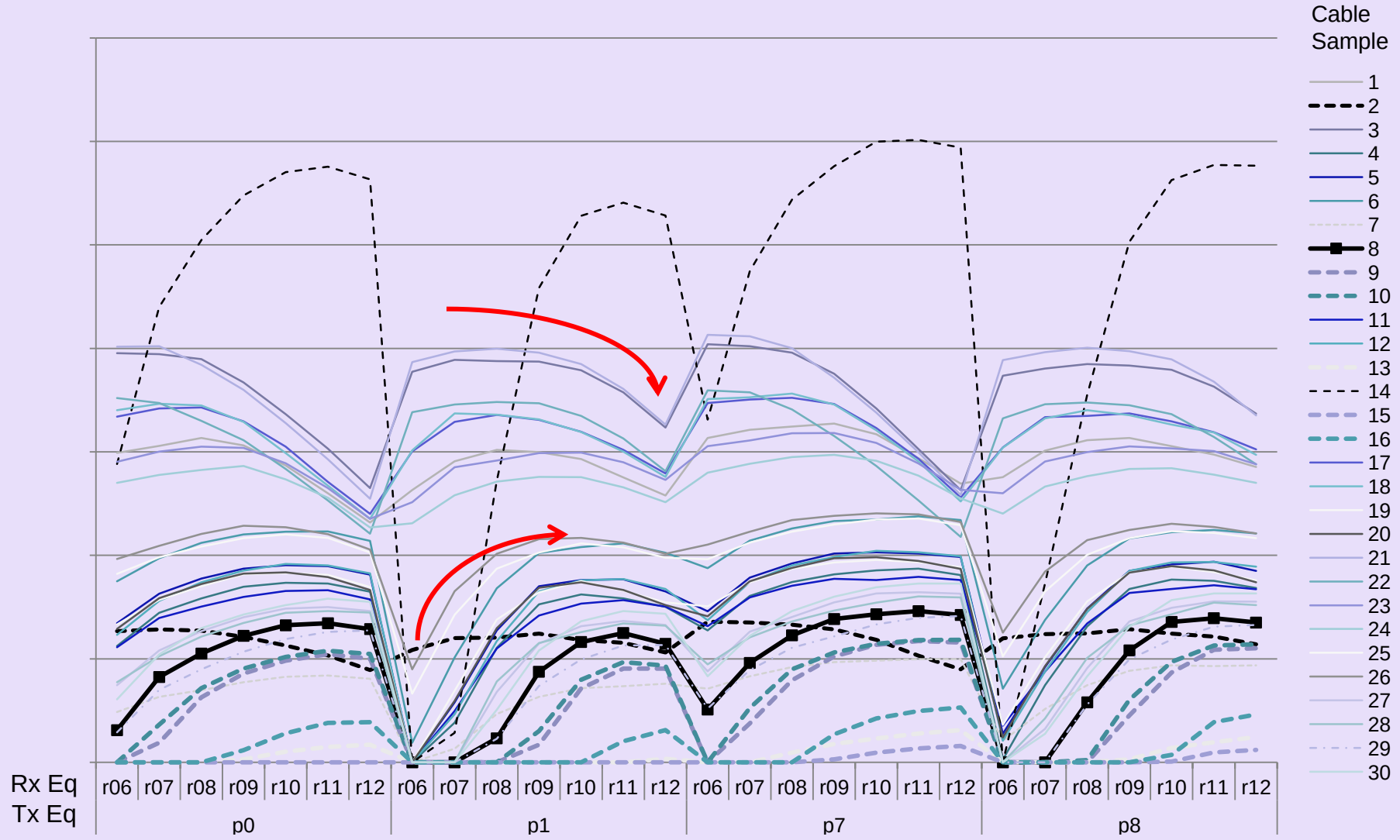


Looking at the Data

- Some cables will train at any preset combination
- Different cable assemblies react differently to the transmitter and receiver settings
  - ✓ This can make finding a common setting difficult
- Data included only a single board configuration at either end. Real systems will have a much larger variety in link profile due to design of mating boards. This will need to be explored.

Note: Four presets shown represent the most common from other form factors

Response Trends to Equalization for the Cable Assemblies



Potential Solutions for Copper Cables

- Use single Tx setting for all cables
  - ✓ Potentially limits solution space
- Cable provide data to equalizers
  - ✓ Cable provides loss information to components for preset hints
- Active Copper
  - ✓ Cable can “remove” its own copper and dielectric loss
- Each solution has its own cost and complexity implications

Providing Data to Equalizers

- Use i2c or other data transfer scheme to send data from cable to each end, or upstream only
  - ✓ Goal would be to provide a cable loss estimate that is translated into preset hints and sent to the devices
- One problem, x4 cable has no extra pins
  - ✓ Multiplex existing sidebands?
  - ✓ Re-pin the cable for PCIe 3.0?
  - ✓ Change connector?

Active Copper Cables

- Participate in, or ignore, Tx change requests?
- Repeaters and External Equalizers are not specifically comprehended in the specification
- And optical links will have this issue as well…

Optical PCI Express Challenges and Considerations

- No sidebands over fiber
  - ✓ Optical sidebands are very expensive
  - ✓ Mixed technology cables are possible, but this increases complexity and removes electrical isolation
- No additional cable pins available in current solution for active cable programming/identification
- Separate Refclk architecture
  - ✓ Currently only a couple of devices can do this
  - ✓ Some optical solutions handle this with varying degrees of success
  - ✓ New ECR is being evaluated, but implementation is unknown
  - ✓ Some solutions use a non-spread clock for optical solution

Optical PCI Express Challenges and Considerations

- Electrical Idle support
  - ✓ What happens to optics during electrical idle?
- Presence Detect
- Link EQ negotiations
  - ✓ Equalization behaviors
- Cascading Jitter
- Data Flow
  - ✓ Credits, Ack/Nack Timeouts, Completion Timeouts due to time-of-flight
  - ✓ Loss of throughput/data bandwidth due to credits

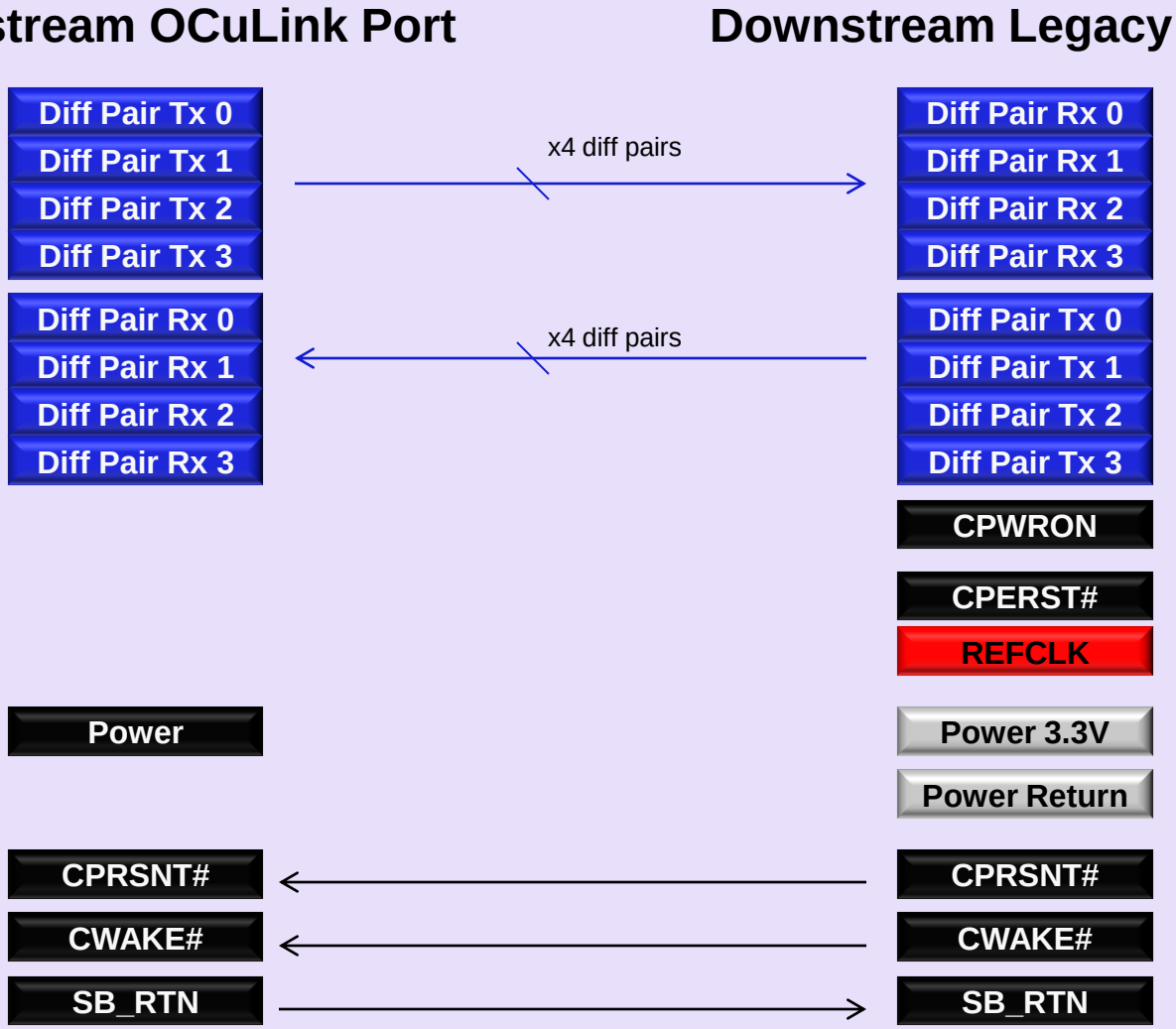
Optical PCI Express Challenges and Considerations

- Which optical form factor?
  - ✓ Active optical cable
  - ✓ optical module (i.e. SFP, CFP, etc.)
  - ✓ Integrated optics with external fiber cable
- Power & Thermal Density for x16 cables appears to be difficult

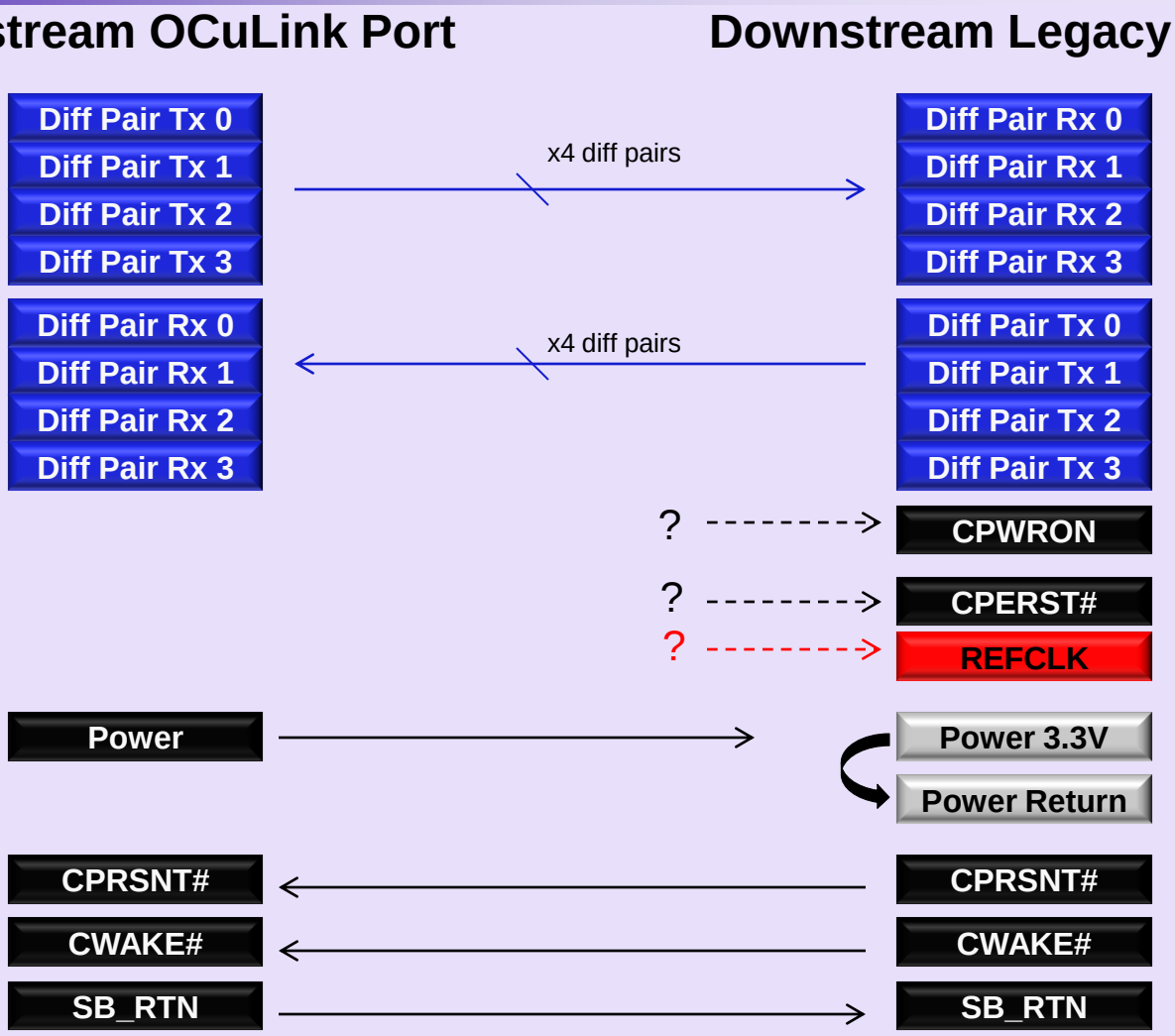
Compatibility

- A new cable group has been tasked with creating a smaller form factor to support mobile applications
  - ✓ Current cable connectors are too large
- The new group is intending to support separate Reference clocks
  - ✓ This will not work with existing cabled products
- Sideband support
  - ✓ There is an attempt to minimize sidebands, but the specifics are in development

Port Signal Mismatch



Port Signal Mismatch



Cabled PCIe 3.0 Options

- Stay with current PCIe cable connectors
  - ✓ Reuse existing sideband pins
  - ✓ Exclude x4 from PCIe 3.0
- New Connector
  - ✓ Allows modularity
    - Ability to down-plug a port without a special cable
  - ✓ Optical support in the same connector
- Architectural Compatibility
  - ✓ OCuLink
  - ✓ Legacy PCIe
- Equalization Scheme

Call to Action

- Review your company's cabling needs and share with the Cabling Working Group. There is time to have your voice heard.

PCI Express® Cabling Updates

Michael Krause
OCuLink Workgroup Chair
Hewlett-Packard

Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

What is OCuLink?

- New specification effort targeting:
  - ✓ Small form factor optimized connectors
  - ✓ Internal enclosure cable usage models
  - ✓ External enclosure cable usage models

External Usage Models

- External enclosures
  - ✓ Ultra-thin mobile
  - ✓ Desktop / workstation
  - ✓ All-in-one computers
  - ✓ I/O expansion enclosure
- Peripherals
  - ✓ Audio / Video equipment (camera, microphones, etc.)
  - ✓ Video distribution
  - ✓ Monitor hub
  - ✓ Medical equipment
  - ✓ External storage
  - ✓ Docking stations

Internal Usage Models

- Internal enclosures
  - ✓ Ultra-thin mobile
  - ✓ Desktop / workstation
  - ✓ Server and storage arrays
- Peripherals
  - ✓ Storage disk drives
  - ✓ NVM / solid state storage drives and adapters
  - ✓ I/O expansion slots

Cable Types and Distances

- Passive copper cable solutions
  - ✓ ~1-2 meters
- Active copper cable solutions
  - ✓ ~2-10 meters
- Active optical cable solutions
  - ✓ ~1-N meters
    - N can be quite large, e.g. 100-300 meters
    - Primarily limited by optics technology and mechanical packaging
      - Also limited by PCIe protocol timeouts (no extreme optical distances)
- Optional peripheral power
  - ✓ ~10W peripheral
  - ✓ ~3W for active module components
  - ✓ Power from either end or both (long distance active)

Connector Attributes (1)

- Single external connector size
  - ✓ Symmetrical cable
- Single internal connector size
  - ✓ Symmetrical cable
- Maximum link width of x4
  - ✓ Implementations can support x1, x2, or x4
  - ✓ Optional aggregated cables to create x8/x16 solutions
- All implementations must support 2.5, 5, 8 GT/s
  - ✓ Will scale to PCI Express® 4.0 (current target 16 GT/s)
- Optional peripheral power support
  - ✓ 5V, Vaux 3.3V

Connector Attributes (2)

- Minimal sideband signals
  - ✓ CPRSNT#, SB-RTN, CWAKE#
- No Refclk
  - ✓ Requires independent clock with SSC ECN
- Durability
  - ✓ External connector – 10K
  - ✓ Internal connector – 50
- Retention mechanism – Yes, method TBD
- No impact to software, i.e. cable is transparent
- No daisy chain mechanical support
  - ✓ Daisy chain accomplished using a 3-port PCIe® Switch and two connectors within the enclosure and two cables

Current Status

- Draft 0.3 Review – Completed
- Draft 0.5 Review – Underway
- Connector Concept Evaluation – Underway
- Draft 0.7 Review – target 3Q2012
- Draft 0.9 Review – target late 4Q2012
- Final specification 1Q2013

Thank you for attending the
PCI-SIG Developers Conference 2012

For more information please go to
www.pcisig.com