
PCI
SIG™

PCI Express Compliance Program

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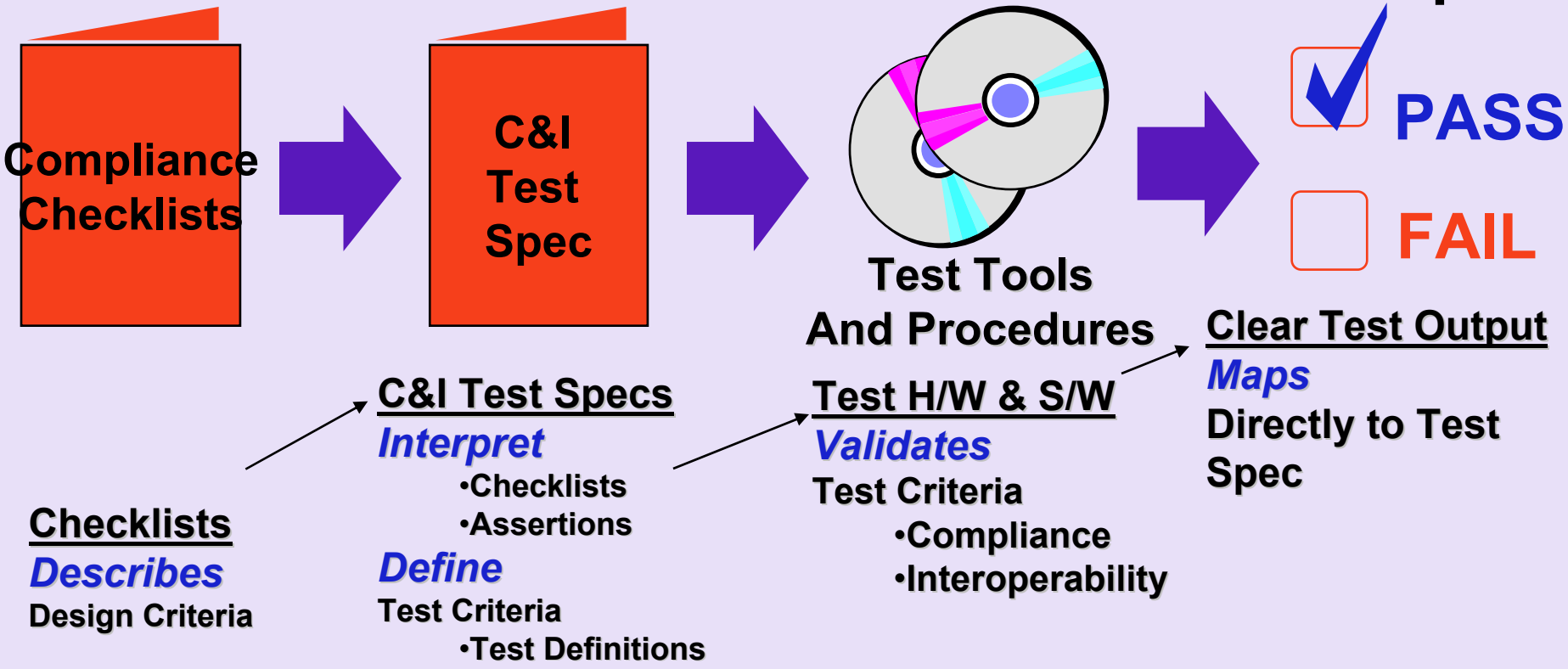
Agenda

- Compliance Process Components
- Compliance Tools Goals
- Compliance Tools
  - ✓ Electrical
  - ✓ Configuration
  - ✓ Protocol
  - ✓ Platform BIOS
- Compliance Workshops

PCI Express Compliance
Process Components



Predictable Path to Design Compliance

PCI Express Compliance Checklists

- Provide design-time ‘rules’ that implementations should follow
  - ✓ Checklists for Root Complex, Endpoint, Switch, addin card, and motherboard
- Simple set of ‘yes/no’ questions
- Checklists available on PCI SIG website
  - ✓ *http://www.pcisig.com/specifications/pciexpress/technical_library*

PHY.2.6#1	Training sequence ordered-sets are never scrambled but always 8b/10b encoded.	yes ___ no___
PHY.3.1#25	The receiver terminations must remain enabled in Electrical Idle.	yes ___ no___
PHY.3.2#5	The Beacon signal must contain minimum width pulses >= 2 ns.	yes ___ no___

PCI Express Compliance
Test Specifications

- Clear description of what is being tested

- Contains:
  - ✓Assertions
    - Prioritized set pulled from checklists
  - ✓Test Descriptions
    - What a test does, and what assertions it checks

PCI Express Compliance
Test Procedures

- Describes how to run tests
  - ✓Required equipment
  - ✓Equipment setup
  - ✓Step-by-step instructions

- Detailed procedures help ensure repeatability
  - ✓At Compliance Workshops
  - ✓In development labs

Compliance Tools Goals

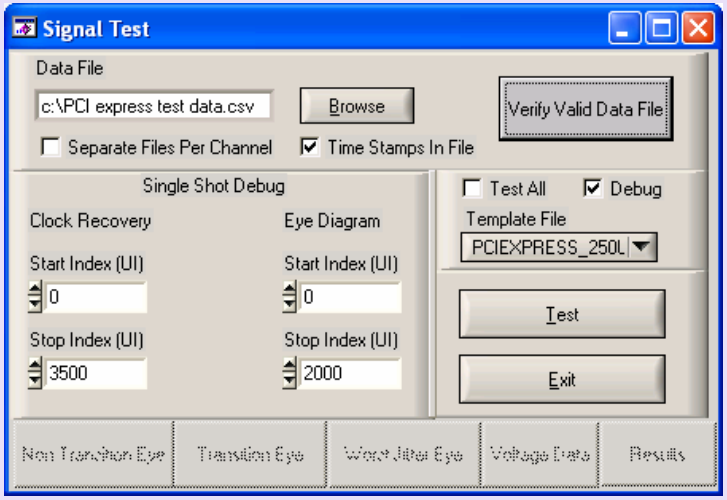
- Wide deployment in development labs
  - ✓ Tools and procedures should be useful and valuable in a development lab setting
- Easy to use
  - ✓ Clear documentation, clear procedures
- Reasonable equipment cost
  - ✓ ~$50K
  - ✓ Ideally, equipment is useful for many other things besides PCI Express compliance testing

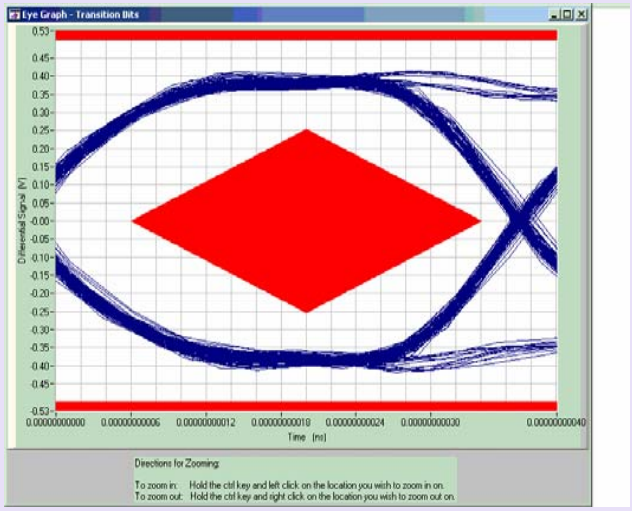
Compliance Test Areas

- Physical layer
  - ✓ Examine electrical signaling
- Configuration Space
  - ✓ Verify required fields and values
- Link & Transaction layer (2 areas)
  - ✓ Exercise protocol boundary conditions
  - ✓ Inject errors and check error handling
- Platform Configuration
  - ✓ Check BIOS handling of PCI Express devices

Electrical Tests and Tools

- Signal Quality Analysis H/W and S/W
  - ✓ Eye pattern, jitter and bit rate analysis
  - ✓ Upstream and downstream signaling
  - ✓ Electrical compliance base board
  - ✓ Electrical compliance load board
  - ✓ Stand-alone Windows-based eye diagram analysis S/W
  - ✓ Electrical test procedures and Oscilloscope setup files
- Jitter Analysis DLL
  - ✓ Clock Recovery
  - ✓ Interpolation
  - ✓ Transition/non-transition eye points
  - ✓ Goal - Promote consistent solutions

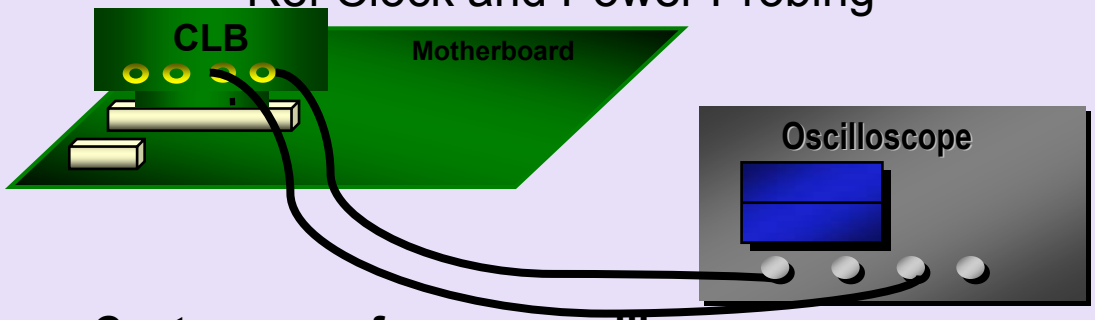




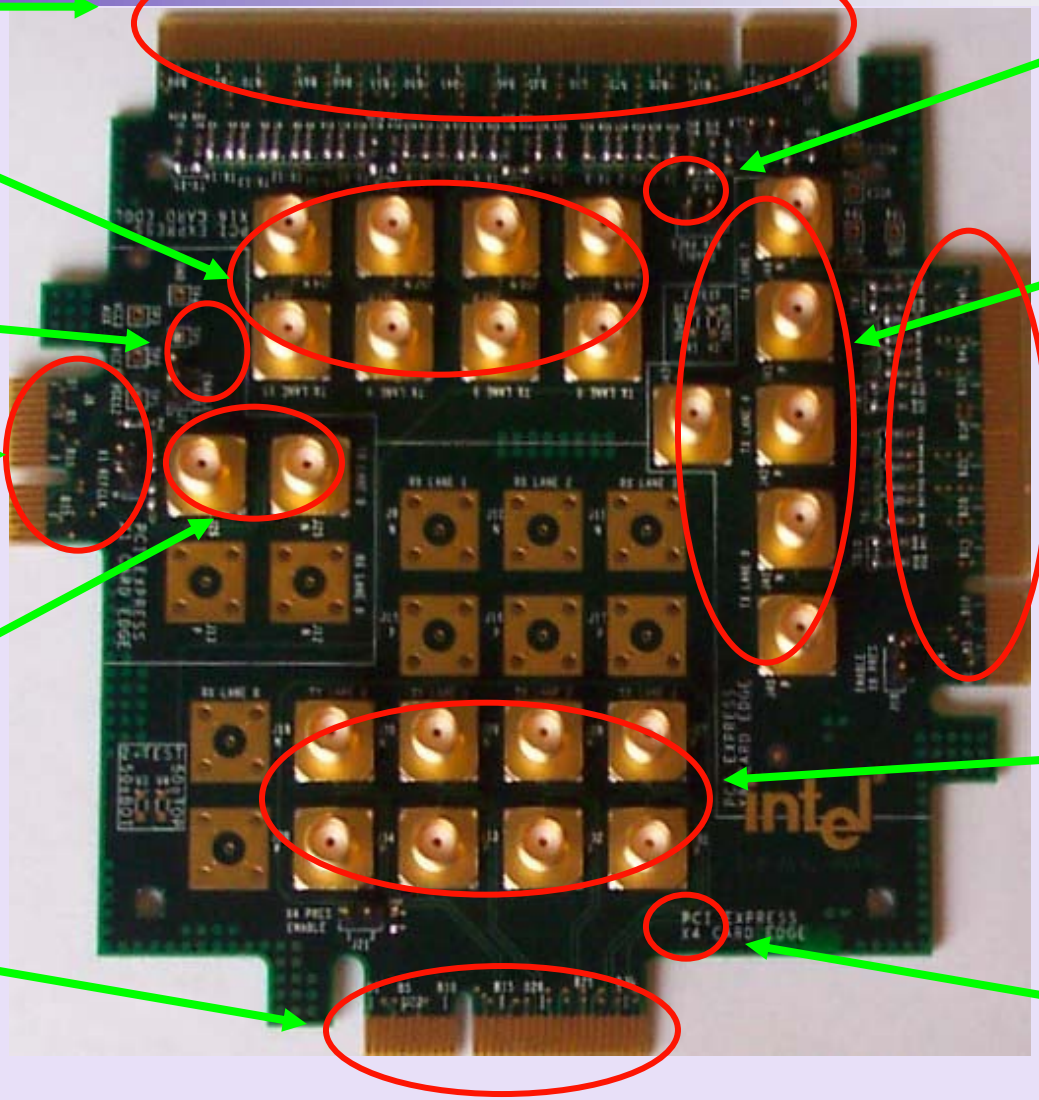
Motherboard Electrical Tools

- Compliance Load Board
  - ✓ Root Complex electrical signal quality
  - ✓ Systems & Motherboards
  - ✓ Terminates Transmitters to utilize spec required compliance mode
  - ✓ X1, X4, X8, X16 test configurations
  - ✓ Improved active probing geometries
  - ✓ SMAs added to x8 & x16, first-middle-last
  - ✓ Analog loopback (Tx to Rx stuff option)
  - ✓ Ref Clock and Power Probing

Available thru PCI SIG website



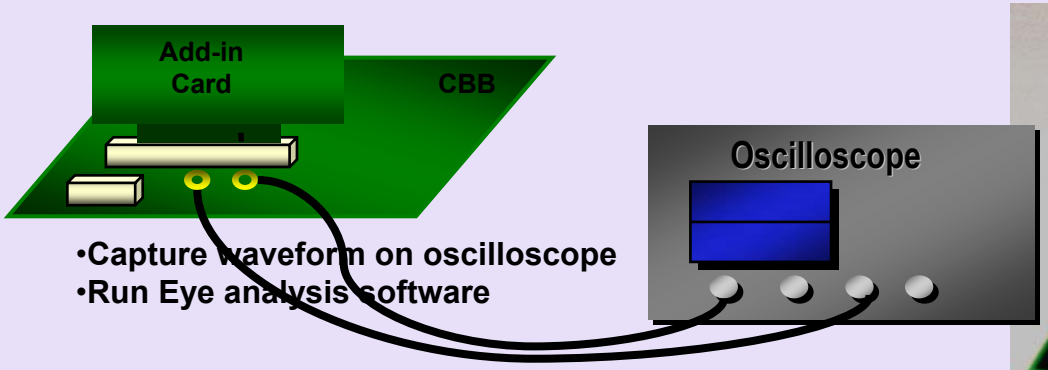
•Capture waveform on oscilloscope
•Run Eye analysis software

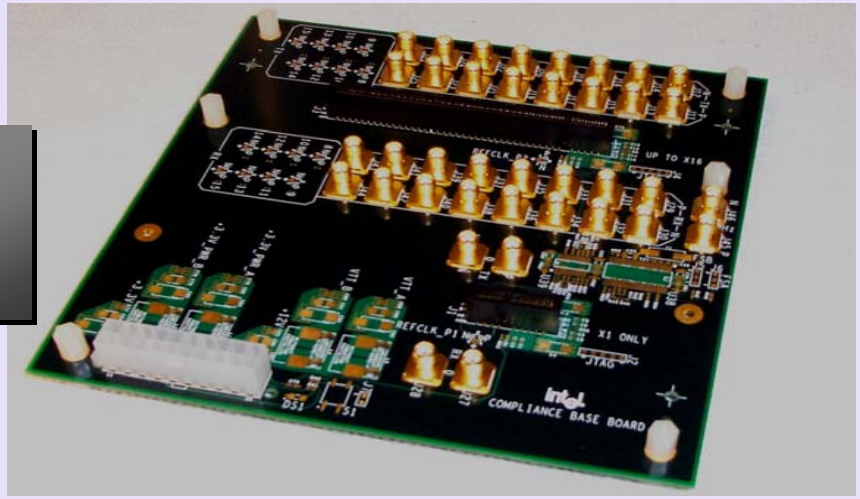


Add-in Card Electrical Tools

- Compliance Base Board
  - ✓ X1, X16 connectors
    - – X16 provides termination X16 through X1
  - ✓ Power adaptor + current measurement
  - ✓ Reference clock or external input

Available thru PCI SIG website





x16 RX Inputs

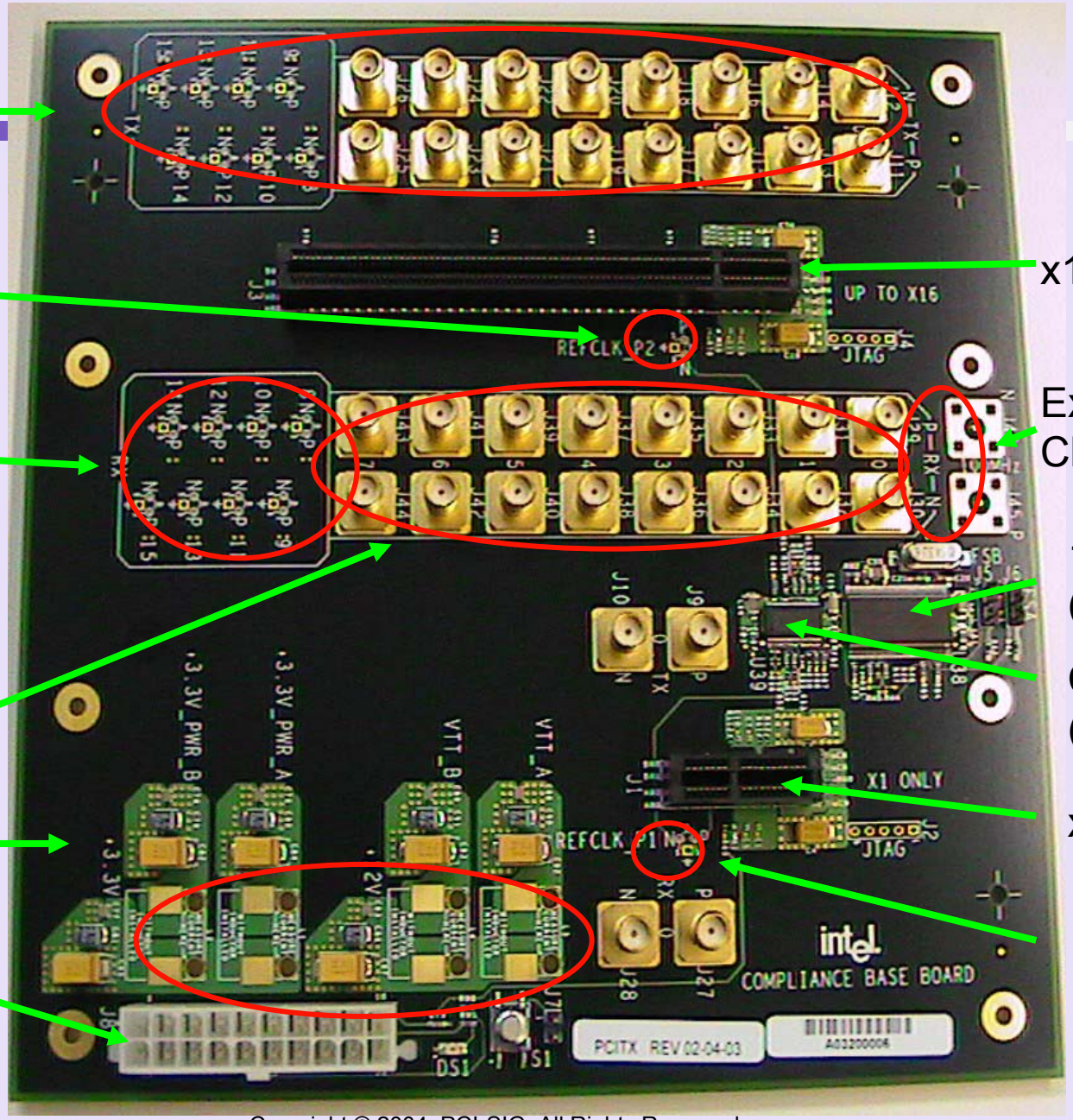
x16 RefClk Probing

x16 TX Active Probing

x16 TX SMA Probing

Current Probing

ATX PS



x16 Test Slot

External Clock Input

100Mhz Clk (CK409)

Clk Buffer (DB400)

x1 test slot

x1 RefClk Probing

Config Space Tests

- Registers and Capabilities
  - ✓Default Values
  - ✓Characteristics
  - ✓Required registers and capabilities
- Functional
  - ✓Configuration Stress
    - Earliest Allowed Requests
    - Different Upstream/Downstream ASPM Combinations
    - Power Indicator/Control Messages

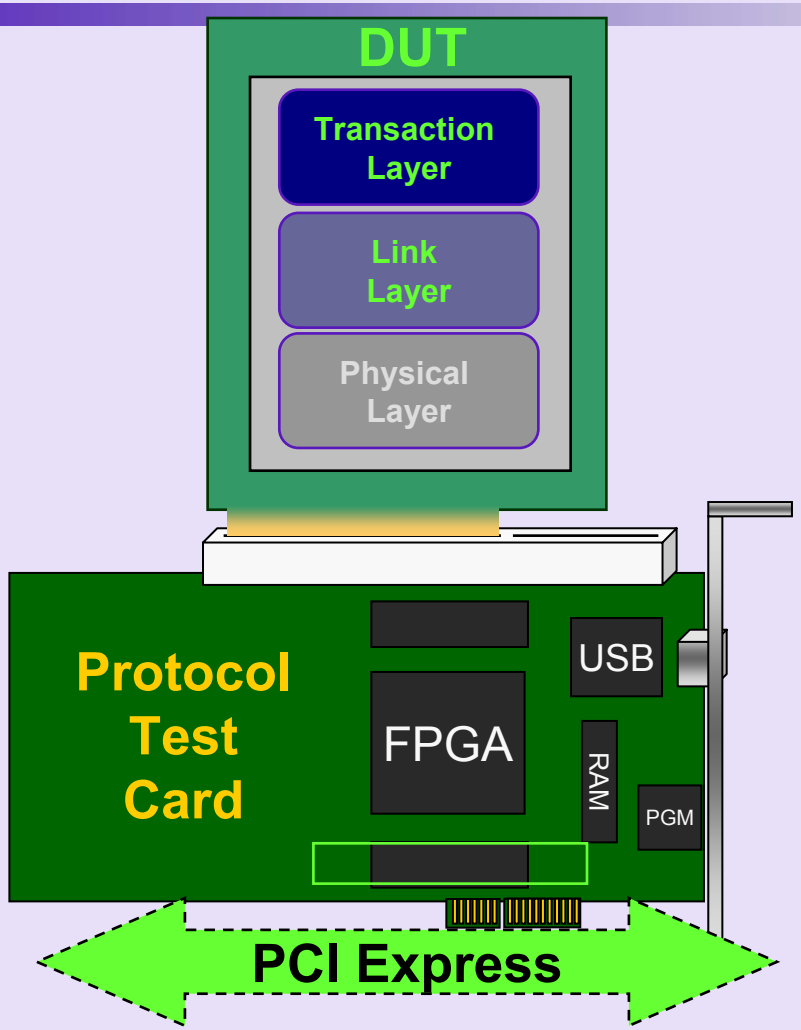
Available thru PCI SIG website

Configuration: Register Only Rule Checks

Check register characteristics and default values..

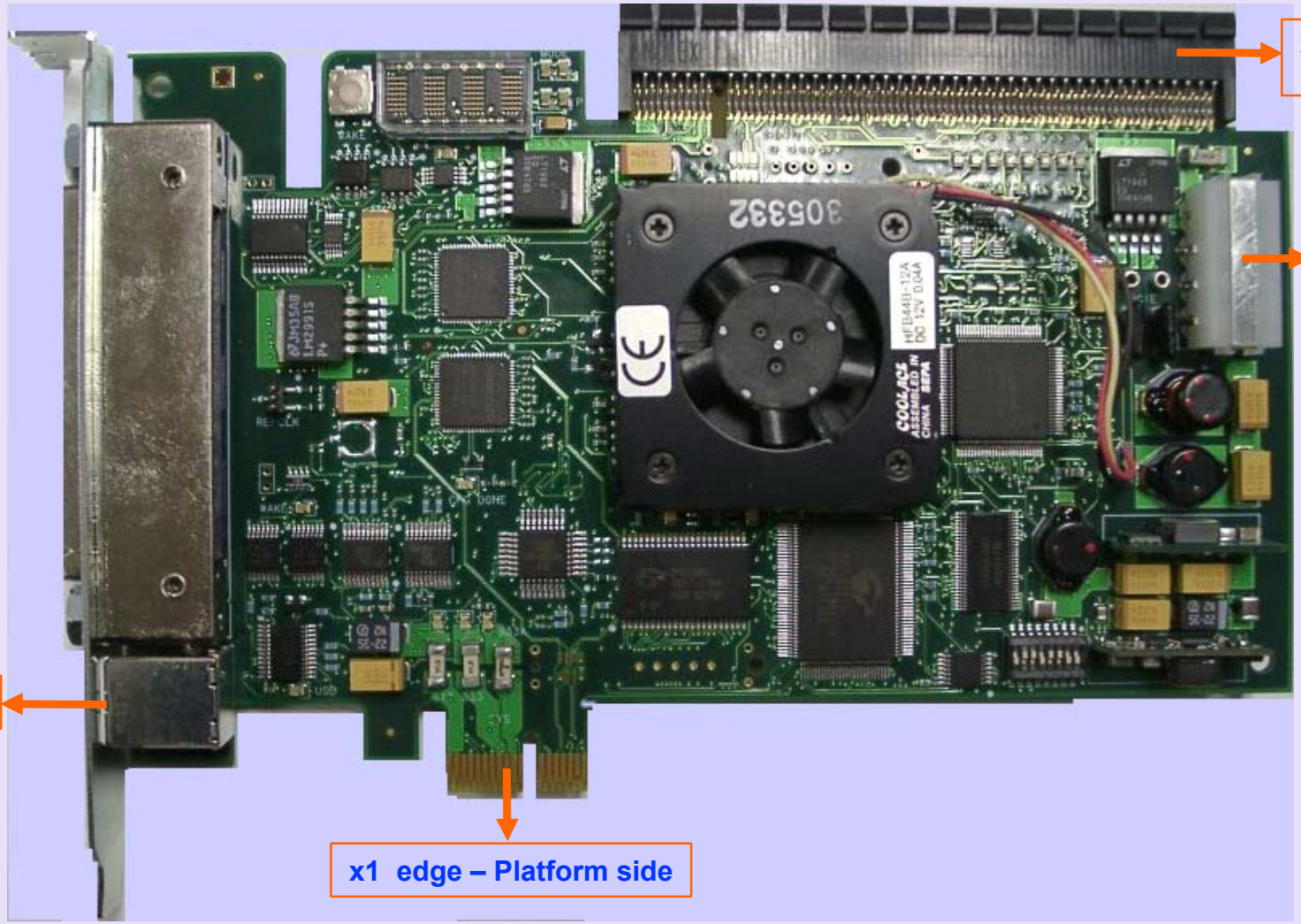
- One test for each new capability
  - ✓ PCI Express Capability
  - ✓ Device Capabilities, Control, and Status
  - ✓ Link Capabilities, Control, and Status
  - ✓ MSI
  - ✓ Advanced Error Reporting
  - ✓ Virtual Channel
  - ✓ Device Serial Number
  - ✓ Power Budgeting

Protocol Testing



- Test Control software running on platform or Device Under Test (DUT) initiates test traffic
- PTC monitors and acts on that traffic
  - ✓ Checking protocol
  - ✓ Injecting errors

Protocol Test Card (PTC)



Link Compliance Tests

- Described in Data Link Test Spec
- Tests
  - ✓ Reserved fields – Device ignores them
  - ✓ NAK response – Device will resend after receiving NAK
  - ✓ Replay Timers – Device will resend packet if no response
  - ✓ Replay Count - Device will resend multiple times when no response
  - ✓ Link Retrain - Device will retrain if continued no response
  - ✓ Replay TLP order – Device replays TLPs in proper order
  - ✓ Bad CRC - Device detects, drops, and logs (DLLPs & TLPs)
  - ✓ Undefined packet – Device ignores
  - ✓ Bad Sequence Number – Device detects, drops, and logs
  - ✓ Duplicate TLP - Device returns data once

Link Replay Timer Test

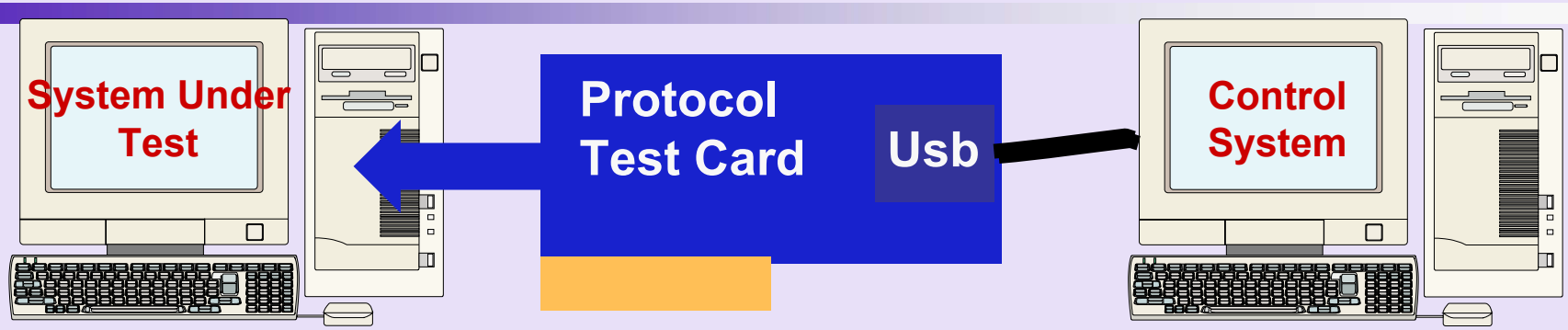
- Get device up and running
- Host does Config_Rd_Req to device
- PTC blocks Config_Rd_Completion from device
- PTC verifies that device ‘replays’ completion

Transaction Compliance Focus

- Basic Functional
  - ✓ Completion request
  - ✓ Completion timeout
  - ✓ Read data
- Baseline Messaging
  - ✓ Legacy interrupts
  - ✓ Native power management
  - ✓ Native Hot Plug
  - ✓ Error Signaling
- Flow Control
  - ✓ Initialization
  - ✓ Transmit and Receive states
  - ✓ Negotiated link width
- Virtual Channel

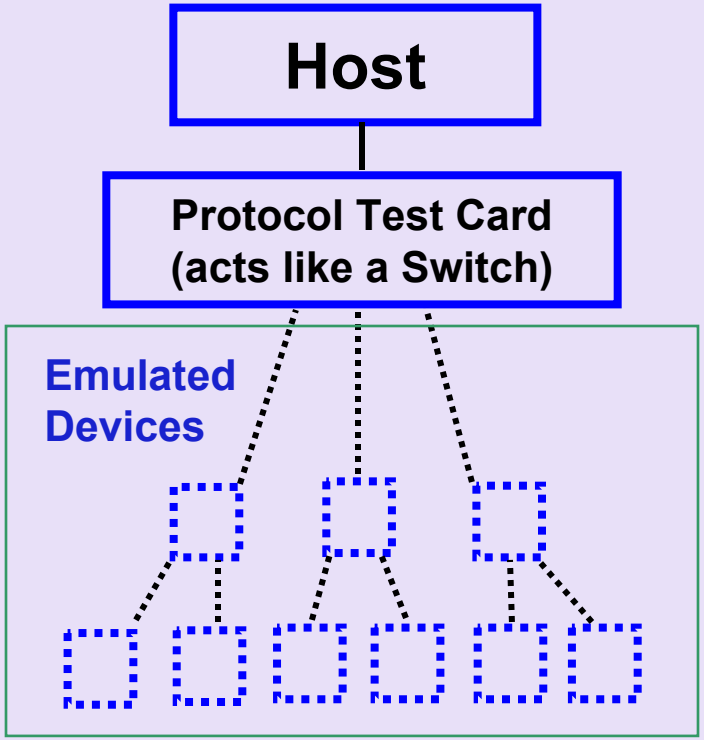
See Test Spec for Details

Platform BIOS Testing



Protocol Test Card Can Represent Any Hierarchical Multi Device/Bridge Topology

Device Decodes All Type 0 and Type 1 Configuration Cycles.



BIOS Test Areas

- Multiple Functions per device
- Different BAR combinations
  - ✓ IO, Mem, 64bit
  - ✓ Various size requests
  - ✓ Prefetchable, non-Prefetchable
- Option ROMs
  - ✓ Varying sizes
  - ✓ Different for each device function
  - ✓ Shrinkable, removable
- Switches and Bridges

Compliance Workshops

- Great opportunity for product interop testing
  - ✓ Different systems, different add-in cards
  - ✓ Engineer networking and troubleshooting
- Typically five workshops per year
  - ✓ Four Domestic, one international
- Second domestic workshop this week
  - ✓ Two more domestic, maybe one more international

Summary

- PCI Express Compliance tools are available
  - ✓ Test specs, procedures, and fixtures are available
  - ✓ Validate in your labs
  - ✓ http://www.pcisig.com/specifications/pciexpress/compliance
- Visit the PCI SIG Website for Compliance Related Announcements
- Attend Compliance Workshops

Thank you for attending the
PCI-SIG Developers Conference 2004.

For more information please go to
www.pcisig.com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