
PCI
SIG®

PCI Express® Cabling

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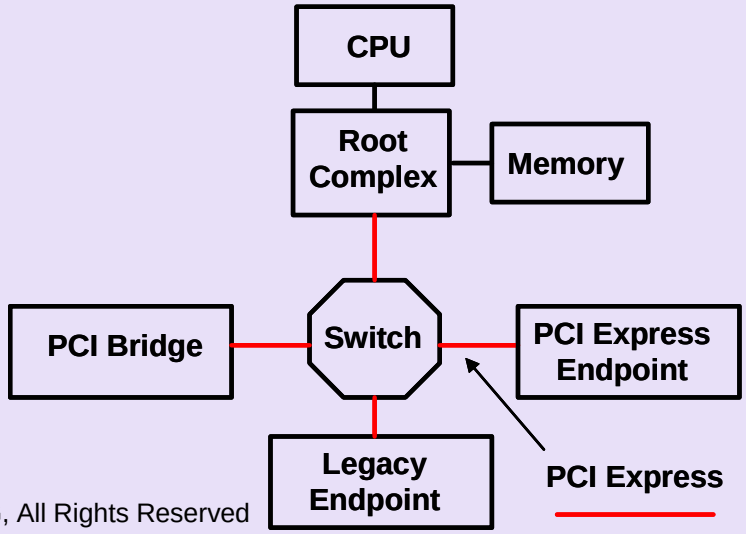
PCI Express® External Cabling

- PCI-SIG® standard defines the input-to-output (I/O) interface functionality to enable the extension of computing processor resources to external subsystems.
- The PCI Express External Cabling specification specifies a copper interconnect to enable longer distances between the computing resources and the external subsystems.
- The copper interconnect will facilitate the interconnection of a wide range of peripherals including PCs, removable Media Drives (e.g. CD/DVD), memory modules, and servers.

PCI Express specifies a hierarchal topology

- Point-to-point links interconnecting ports of physical devices.
- The lanes consist of low-voltage differential signal pairs, a transmit pair and a receive pair.
- Root Complex entity (RC) establishes a reference for the direction of information flow between devices.

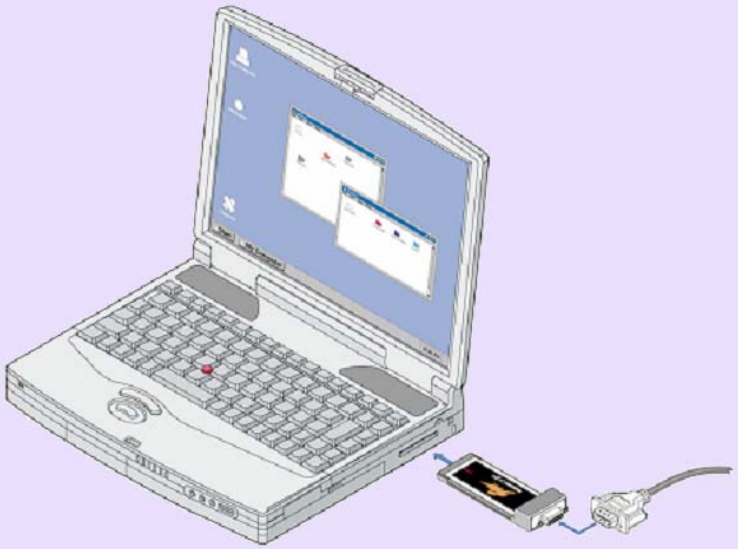


PCI Express External Cabling Applications

- Expansion I/O
  - ✓ Mobile / Desktop / Server platform
  - ✓ ExpressModule
  - ✓ Test & Measurement chassis
  - ✓ ExpressCard
- Split-system (disaggregate) desktop
- Tethered docking for mobile platforms
- External graphics controllers
- Communication equipment
- Embedded applications
  - ✓ High speed data transfer within large office equipment

Example: PCI Express Cabling: ExpressCard™ Implementation

- Single cable connector
  - ✓ x1 for peripheral attachment

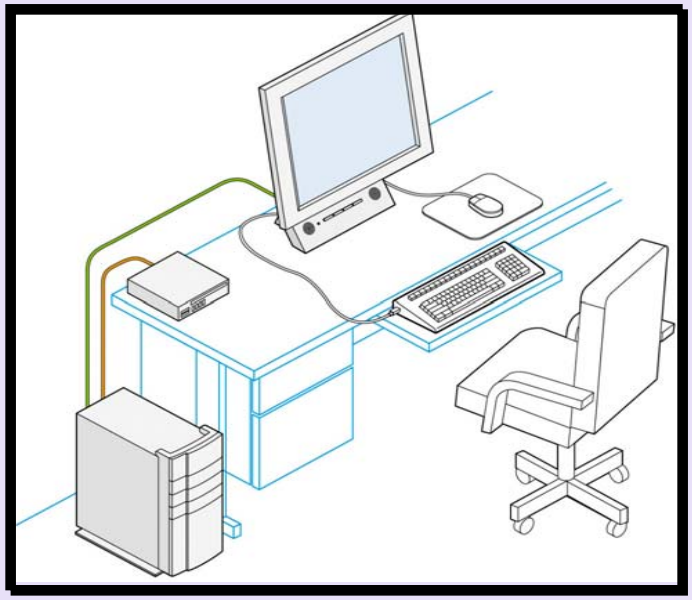


Example: PCI Express Cabling: Server Usage

- Modular I/O Expansion Chassis
  - ✓ Provides additional I/O fan-out for customers who require additional I/O adapters
  - ✓ Leverages existing techniques used with PCI-X
    - – Cable attached to I/O adapter to I/O chassis
    - – I/O Chassis attaches cable to x8 PCIe switch upstream port
      - • x4/x8 fan-out to set of I/O slots

Example: PCI Express Cabling: Split System Application

- Two cable implementation
  - ✓ x16 for graphics
  - ✓ x1 for peripheral attachment



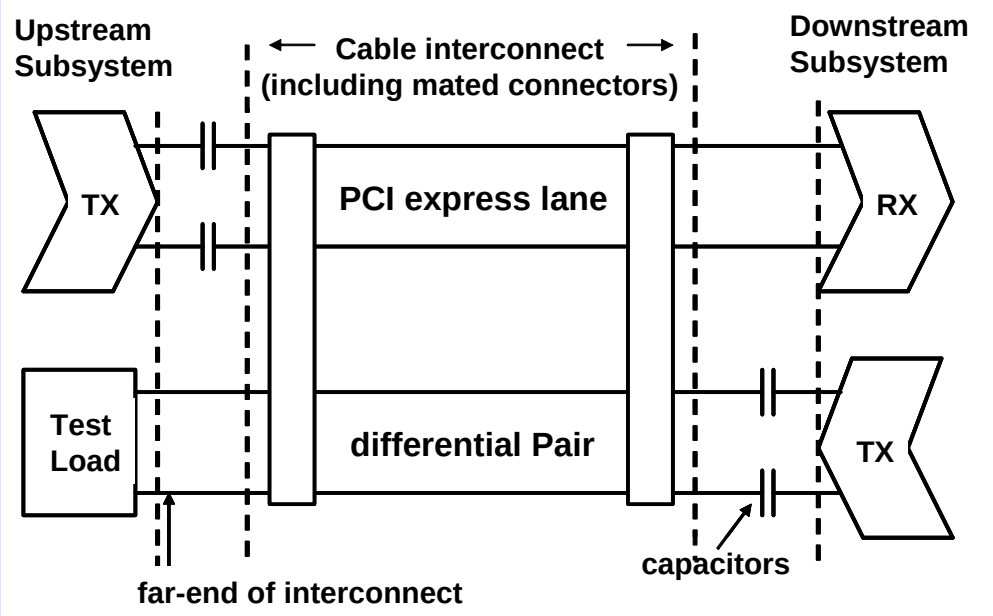
PCI Express External Cabling Specification

- Cable interconnect for supporting data rates of 2.5 GT/s on each PCI Express lane.
- Lane widths specified in multiples of the basic data rate: x1, x4, x8, x16 providing aggregate data rates across lanes from (2.5 x 1) GT/s to (2.5 x 16) GT/s.
- Sideband signaling specified to provide out-of-band control and monitoring.

Cable interconnect

- Upstream and downstream devices are physically interconnected by the cable interconnect. Data flows from upstream to downstream relative to the root complex.

- The cable interconnect is specified as a cable assembly including the mated connectors.

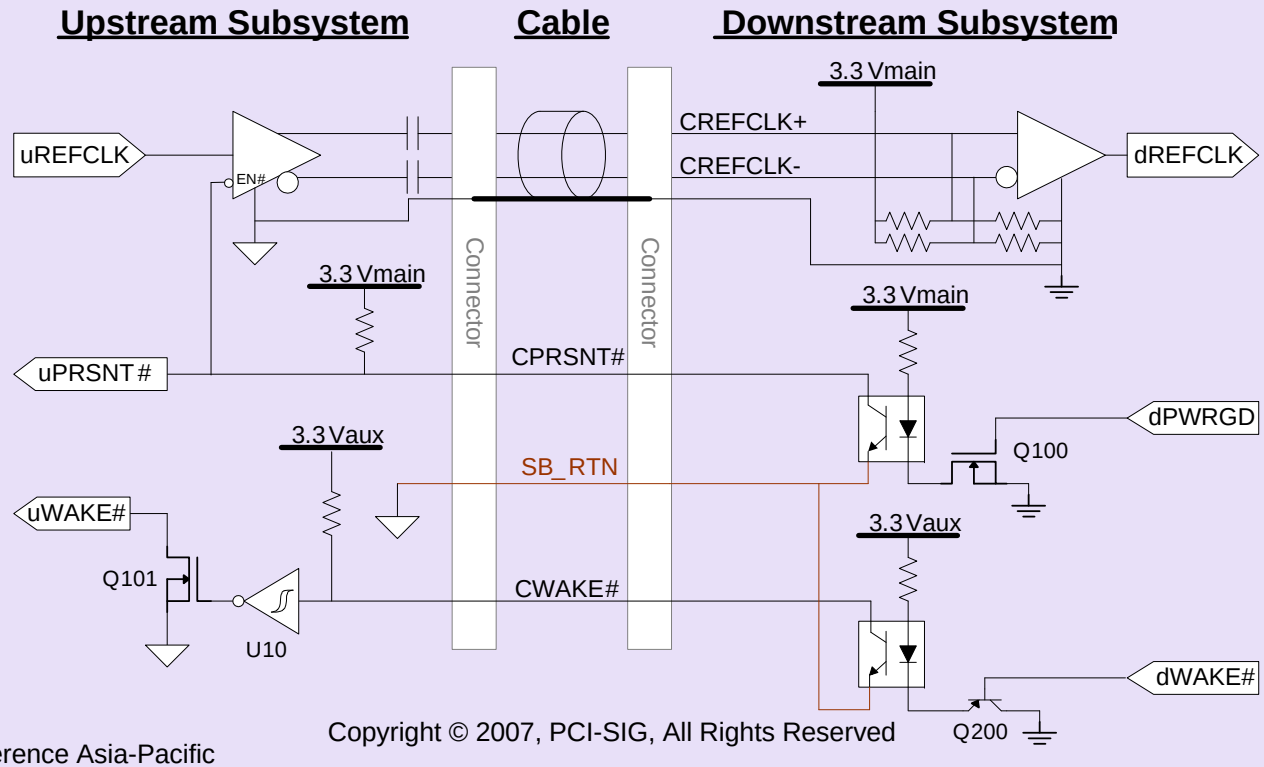


Sideband Signal List

- Objective: compatibility with existing silicon and software
- Signals and key reasons for their inclusion:
  - ✓ CREFCLK (Cable Reference Clock, 100MHz)
    - Supports spread spectrum clocking & Phase Jitter considerations
  - ✓ CPRSNT# (Cable Presence Detect)
    - Indicates a downstream subsystem is present
    - Provides a Power Good status of the downstream subsystem
  - ✓ CWAKE# (Cable Wake) ***[Optional for components]***
    - Needed for suspend / resume
  - ✓ CPWRON (Cable Power On)
    - Needed if downstream subsystem is essentially a slave to the upstream root complex, for suspend / resume functionality
  - ✓ CPERST# (Cable PCIe platform Reset)
    - Allows for full transparency with remote system expansion

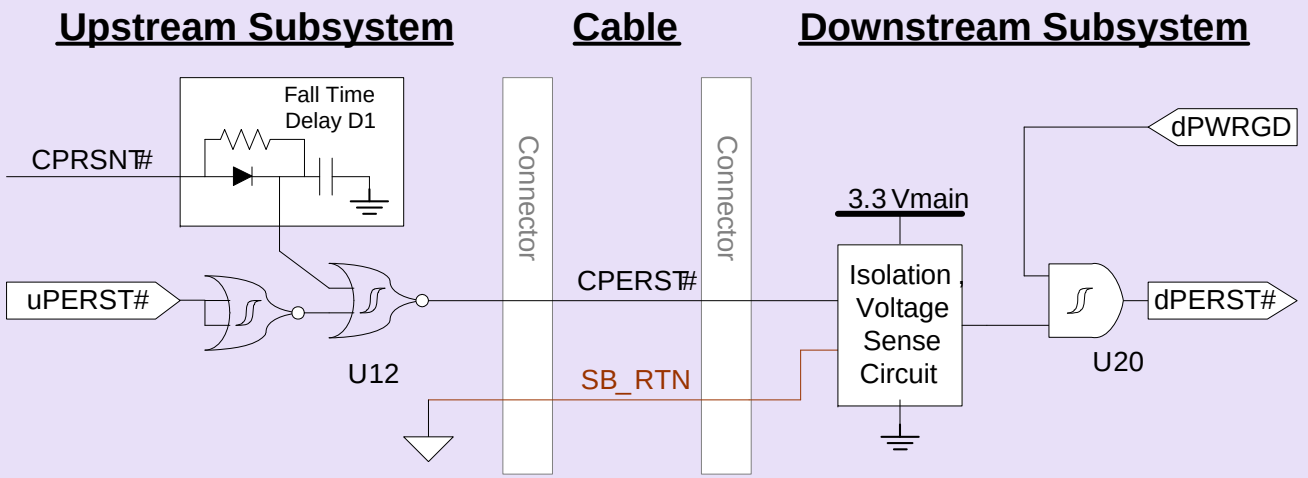
CREFCLK, CPRSNT# & CWAKE#

- CREFCLK is an AC-Coupled differential signal
  - ✓ Source and load termination on RefClk
    - – Block diagram for explanation only, source termination not shown
  - ✓ Requires receiver biasing
  - ✓ Output is enabled with CPRSNT#



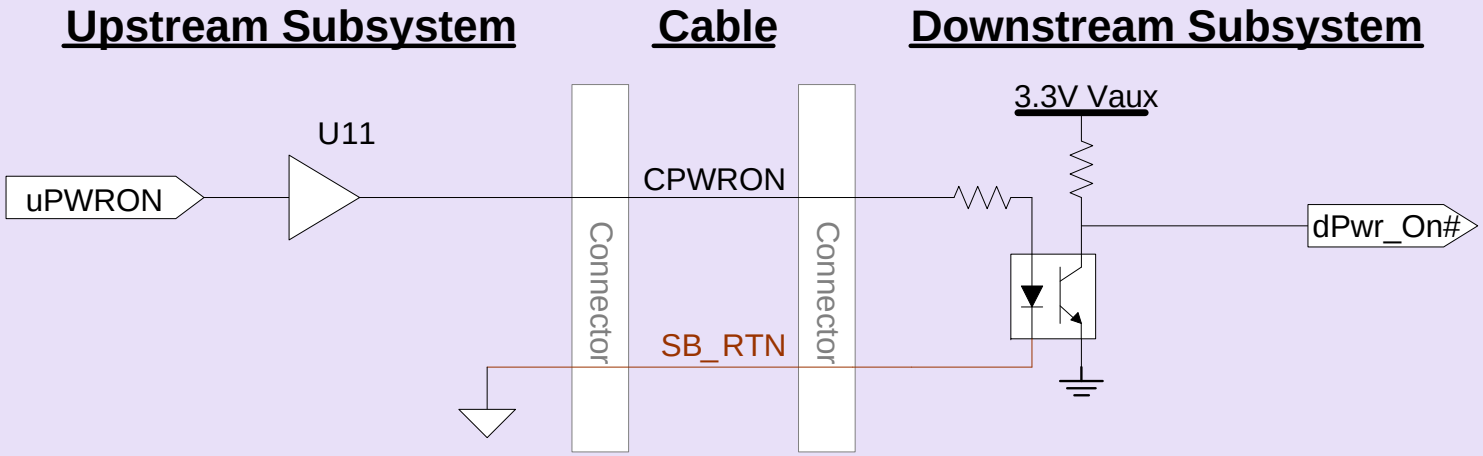
CPERST#

- CPERST# stays asserted until CPRSNT# is asserted and uPERST# is de-asserted
- The isolation / voltage sense circuit for CPERST# within the downstream subsystem might need to account for ground potential differences
- Delay D1 provides minimum CPERST# period following Hot Plug
  - ✓ Block diagram is for explanation purpose only



CPWRON

- Following two usage scenarios illustrate some key considerations:
  - ✓ Allows for automatic power sequencing of downstream subsystem (requires fast power-on at downstream device)
  - ✓ Transition main power in downstream subsystem when entering into and exiting from power management states
  - ✓ Block diagram is for explanation purpose only

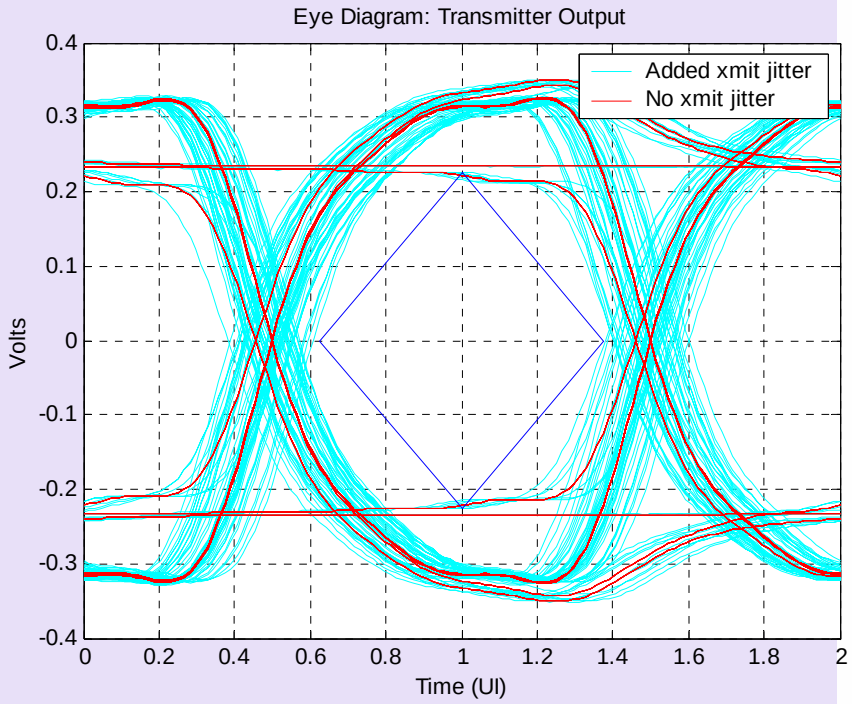


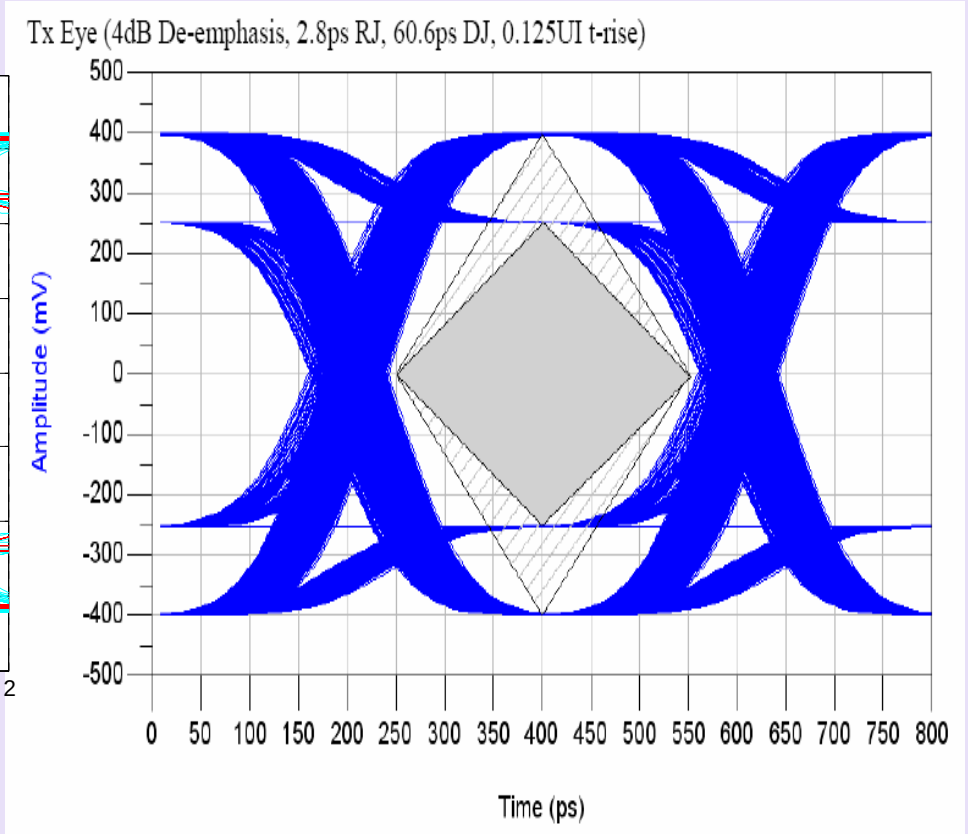
Electrical Specifications

PCI Express Interconnect Specifications

- The interconnect is characterized by s-parameters.
- Eye-diagram at output of interconnect generated utilizing transmitter models and s-parameter models.
- Compare eye-diagram to compliance mask.

PCI Express Base - Transmitter Compliance Eye





TTX-EYE = transmitter eye width including all jitter sources 0.75 (min) = 300 ps

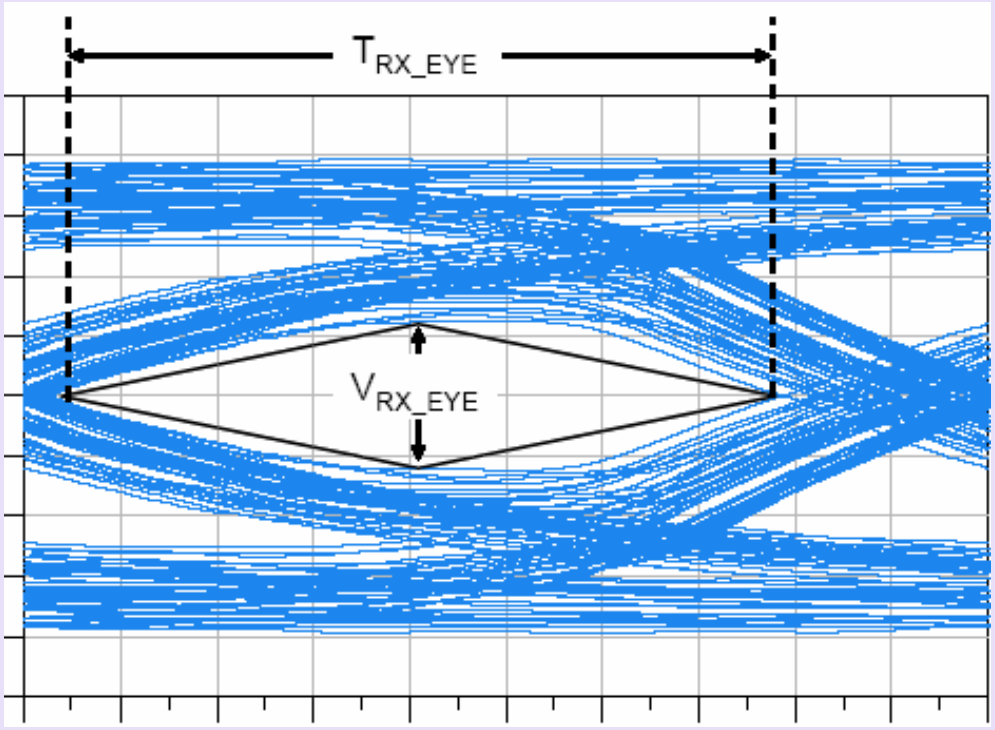
VTX-DIFF-PP = transmit eye height voltage swing 0.8 (min) 1.2 (max) min eye height with a 4 dB de-emphasis ~505 mV

PCI Express Base – Receiver Compliance Eye

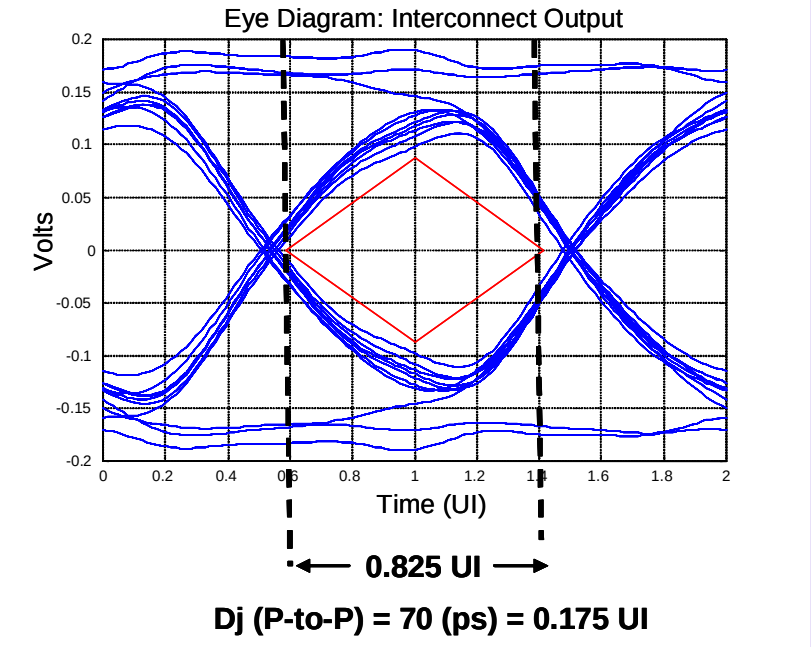
The eye diagram is measured during the transmission of a compliance pattern on one lane while simultaneously transmitting on all other lanes.

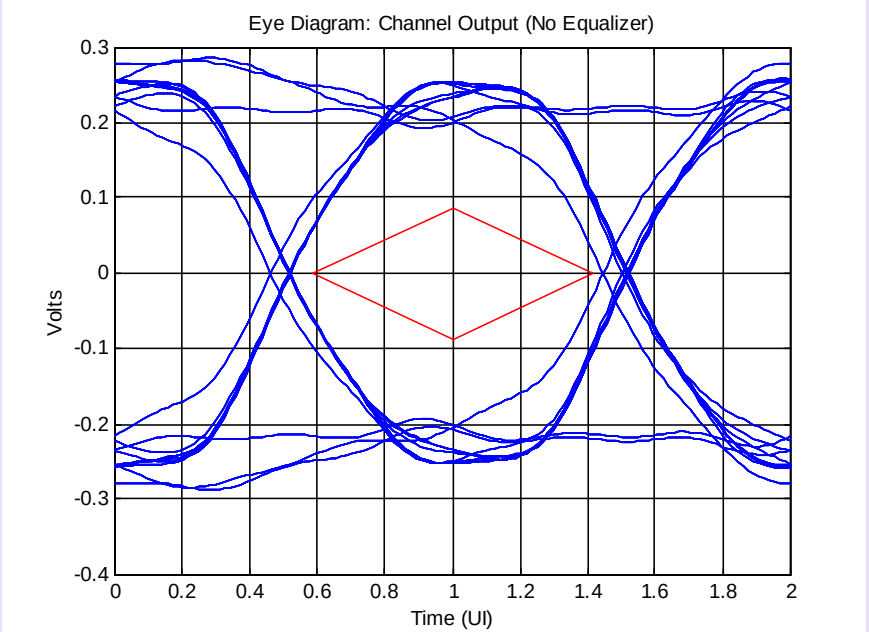
VRX-DIFF-PP - Differential receiver peak-peak voltage 175 mV (min)

TRX-EYE - Receiver eye time 0.40 (min) UI = 160 ps Minimum eye time at Rx pins to yield a 10-12 BER.



Simulation model results





7 meter assembly

.5 meter assembly

Cable Length

- Specification does NOT call out cable lengths
  - ✓ 0.5 meter to 7 meter cable range used in workgroup
  - ✓ Longer lengths facilitated but not specified
- Loss and jitter budgets are derived from PCI Express Base Specification
  - ✓ Very long cables could introduce jitter and signal loss beyond that comprehended in the specification
- PCI Express Protocol parameters are sensitive to round trip delay
  - ✓ Very long cable environments might desire components to vary replay timer values, replay buffer and credit provisioning, etc…

Specification Status

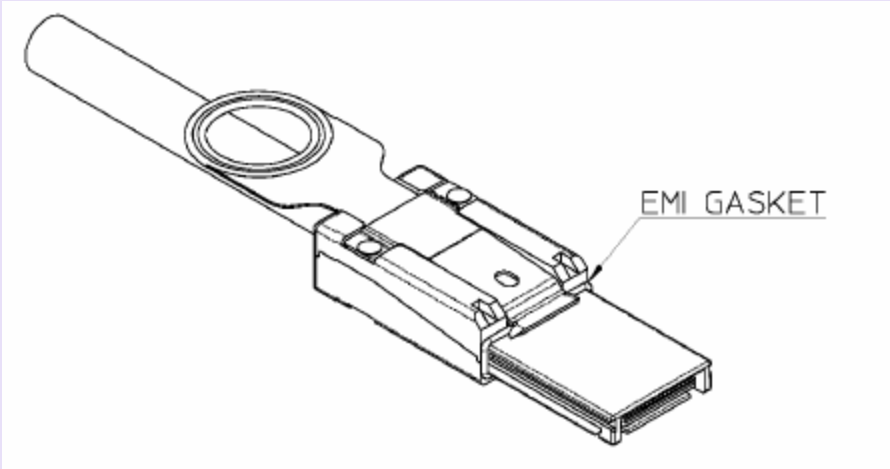
- Version 1.0 Released January 2007

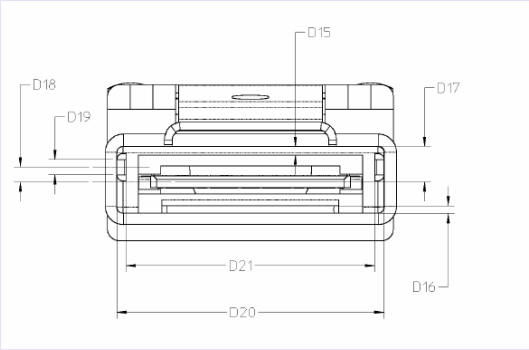
http://www.pcisig.com/specifications/pciexpress/pcie_cabling1.0

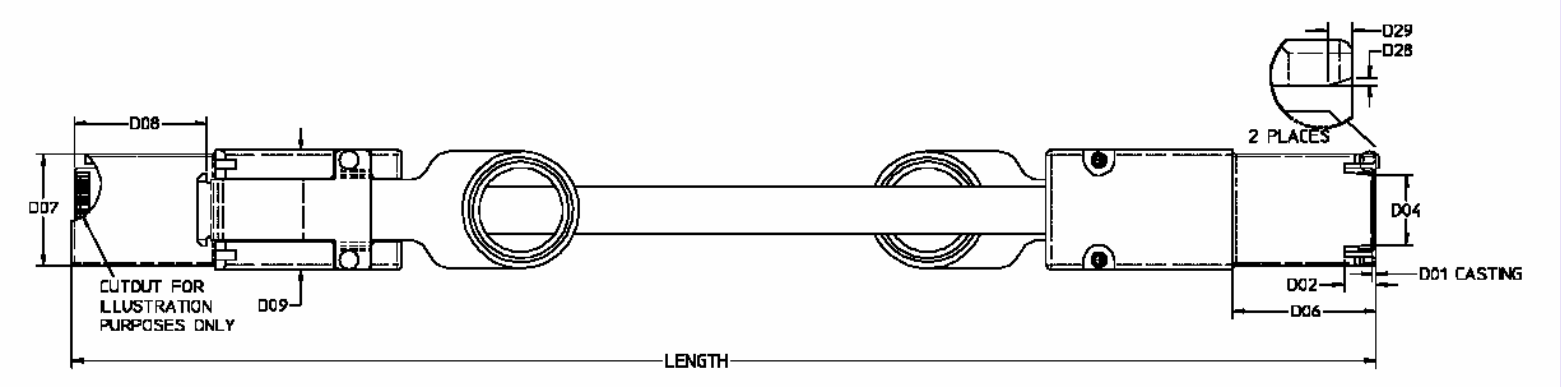
- Workgroup Developing 5GT/s specification

Cable Assemblies

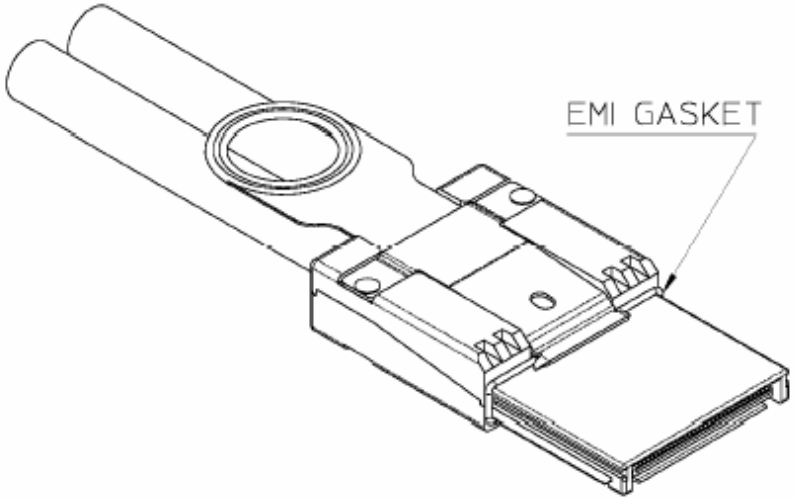
PCI express x4 Cable Assembly

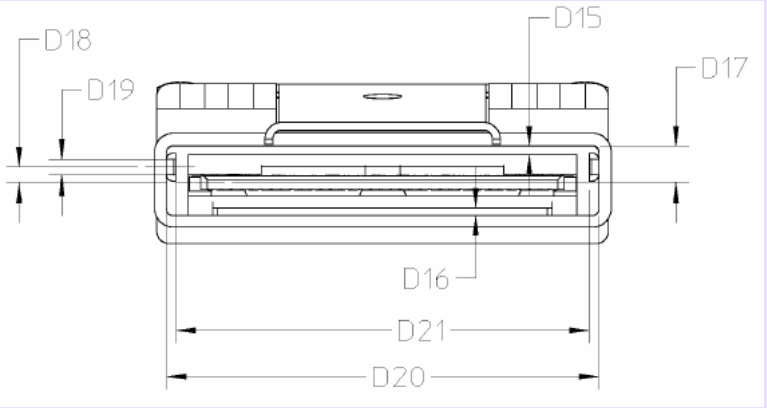


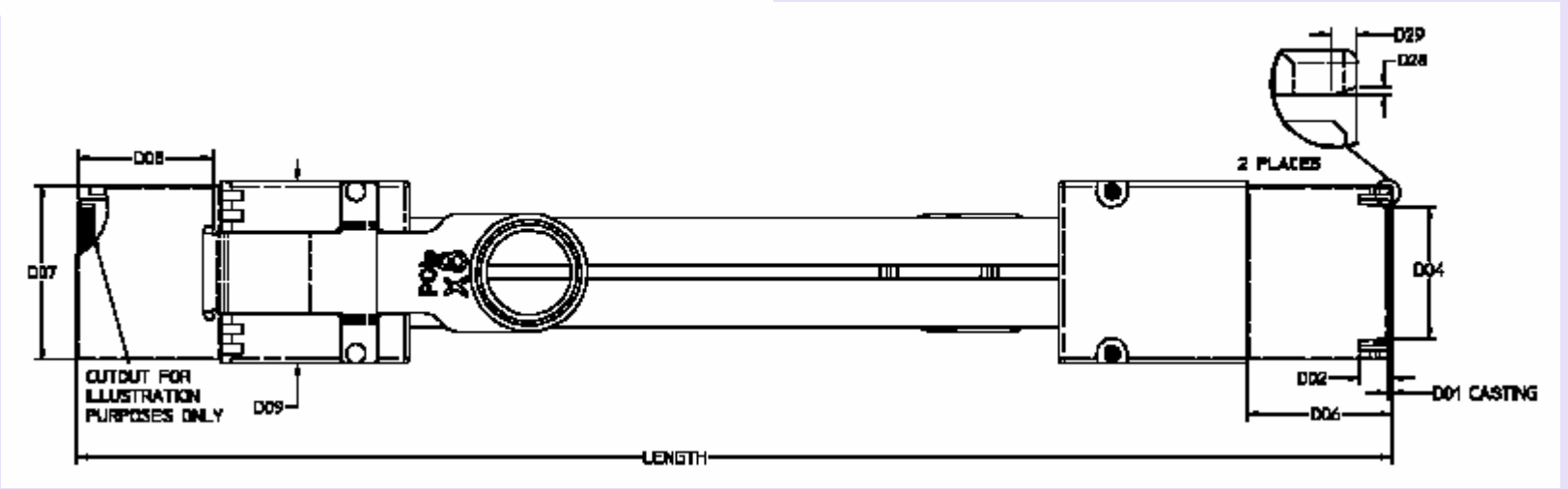




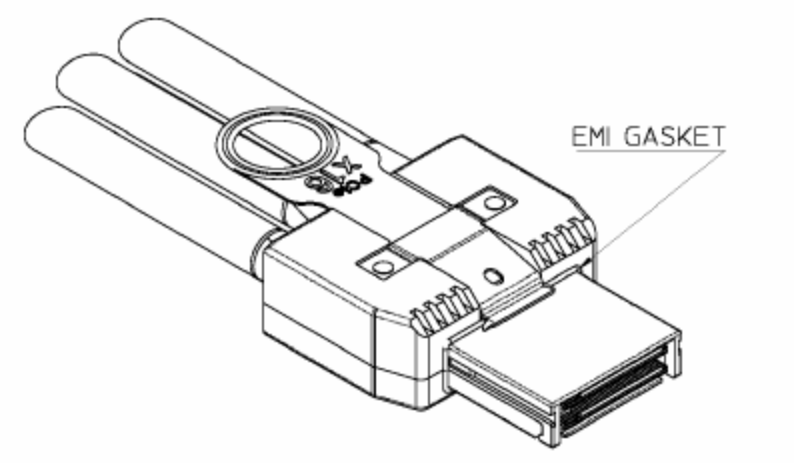
PCI express x8 Cable Assembly

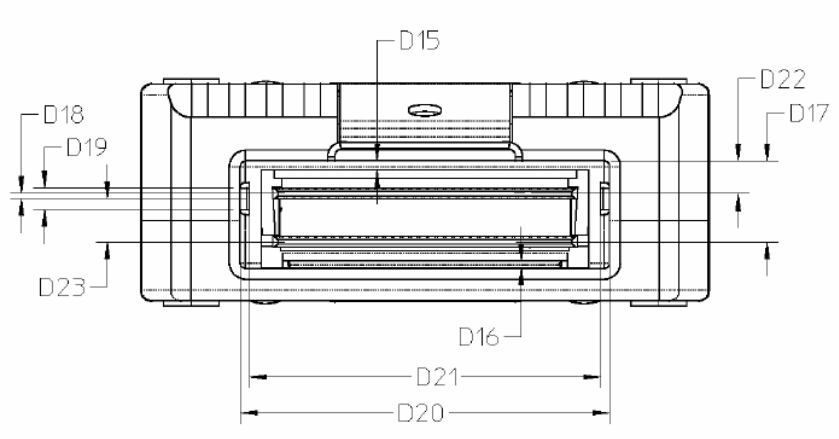


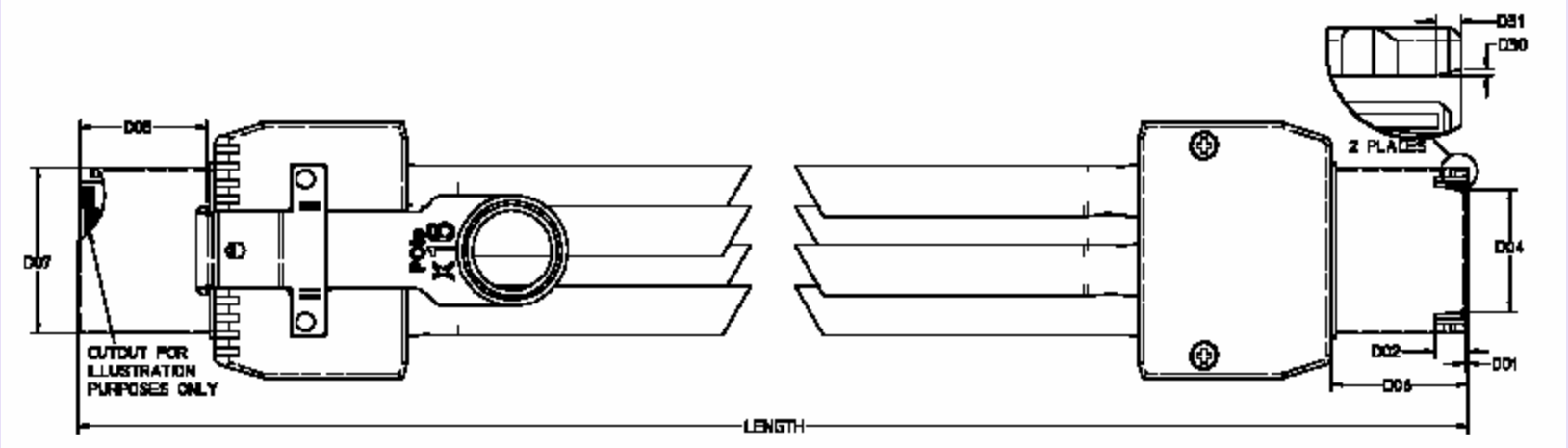




PCI express x16 Cable Assembly







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