



# PCI Express® 1.1 PHY Design Considerations

Milpitas, CA August 29, 2005

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# Agenda

- Logical Physical Layer
- Electrical Physical Layer
- Link Training and Initialization (LTSSM)
- Layout Considerations

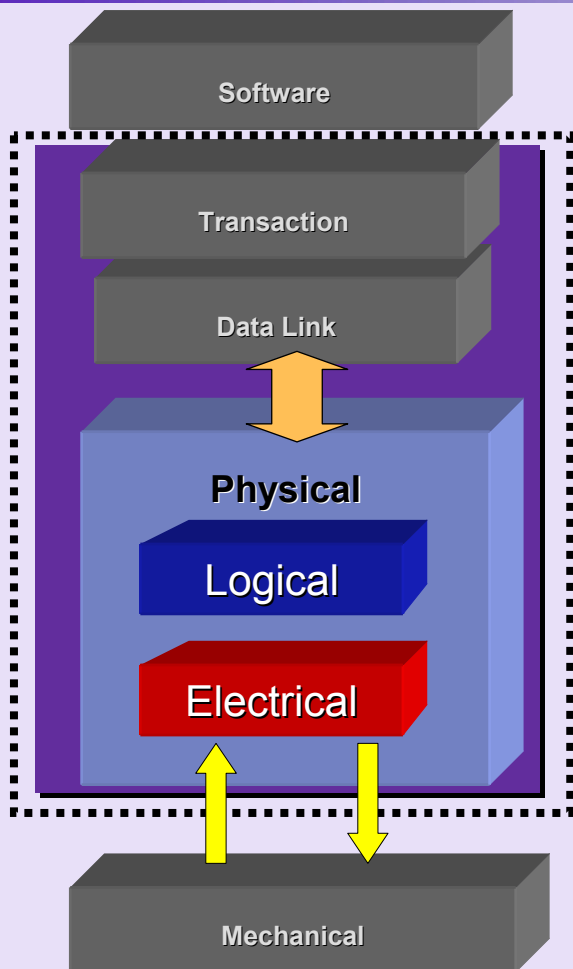
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# PCI Express Physical Layer

- **PCI – PHY is digital in nature**
  - ✓ Parallel multi-drop bus
  - ✓ Bits, a clock, setup and hold times...
    - Jitter essentially ignored
  
- **PCI Express – PHY is analog in nature**
  - ✓ Based on serial technology
  - ✓ Techniques developed by the communication industry
  
- **A transition for microprocessor based systems**
  - ✓ Microwave theory/physics challenges dominate
  - ✓ Two PLLs communicating directly

# PHY Layer Design Basics



## ■ Logical Functions

- ✓ Encoding/decoding/scrambling
- ✓ Reset, initialization, de-skew
- ✓ Built in test modes
- ✓ Configuration:
  - Speed, link width, lane mapping, Polarity
- ✓ Link power management

## ■ Electrical Functions

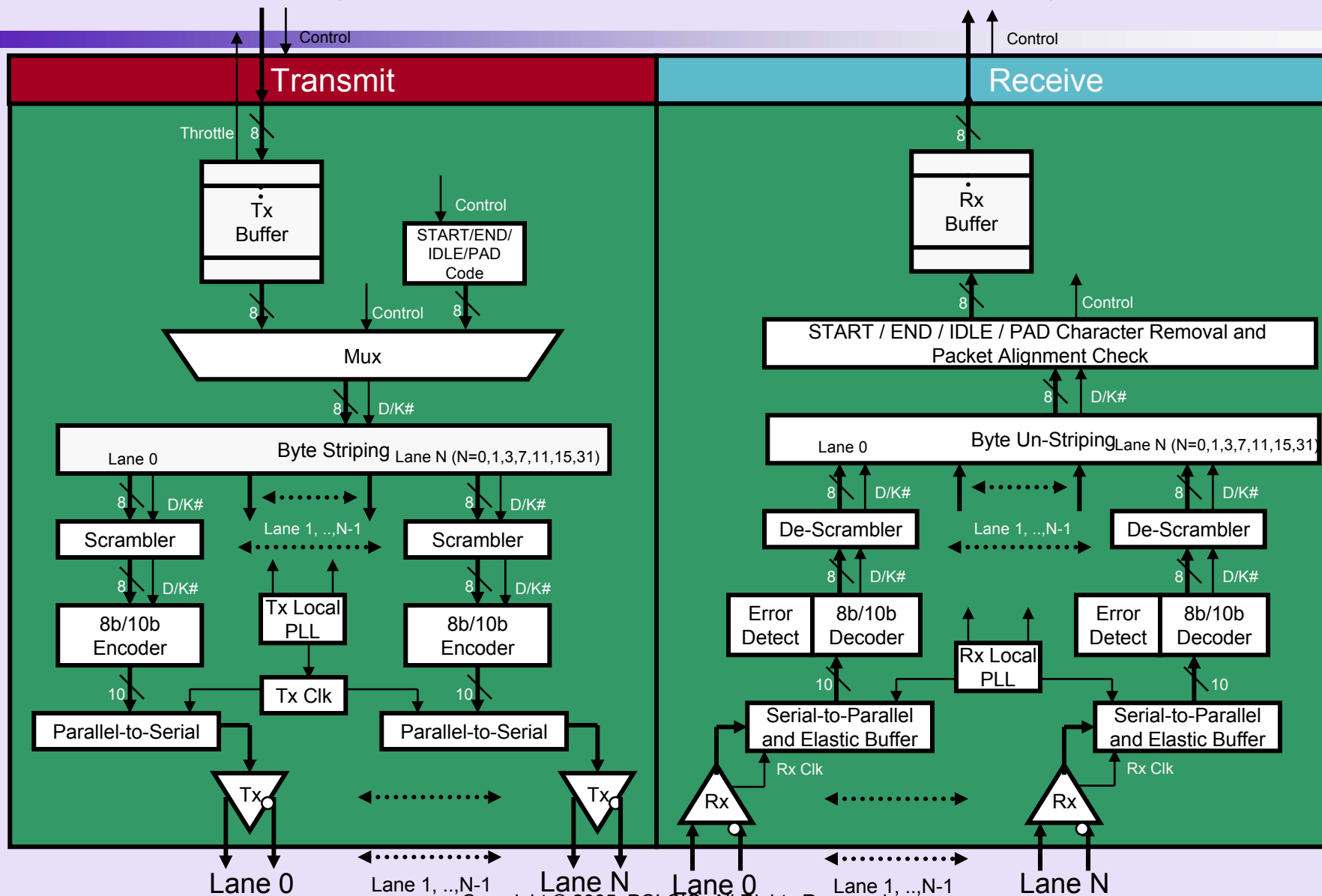
- ✓ Transmitter/receiver
- ✓ Clocks/PLLs
- ✓ Clock/data recovery

**PHY layer upgrades do NOT impact upper layers**

# Logical Physical Layer

From Data Link Layer

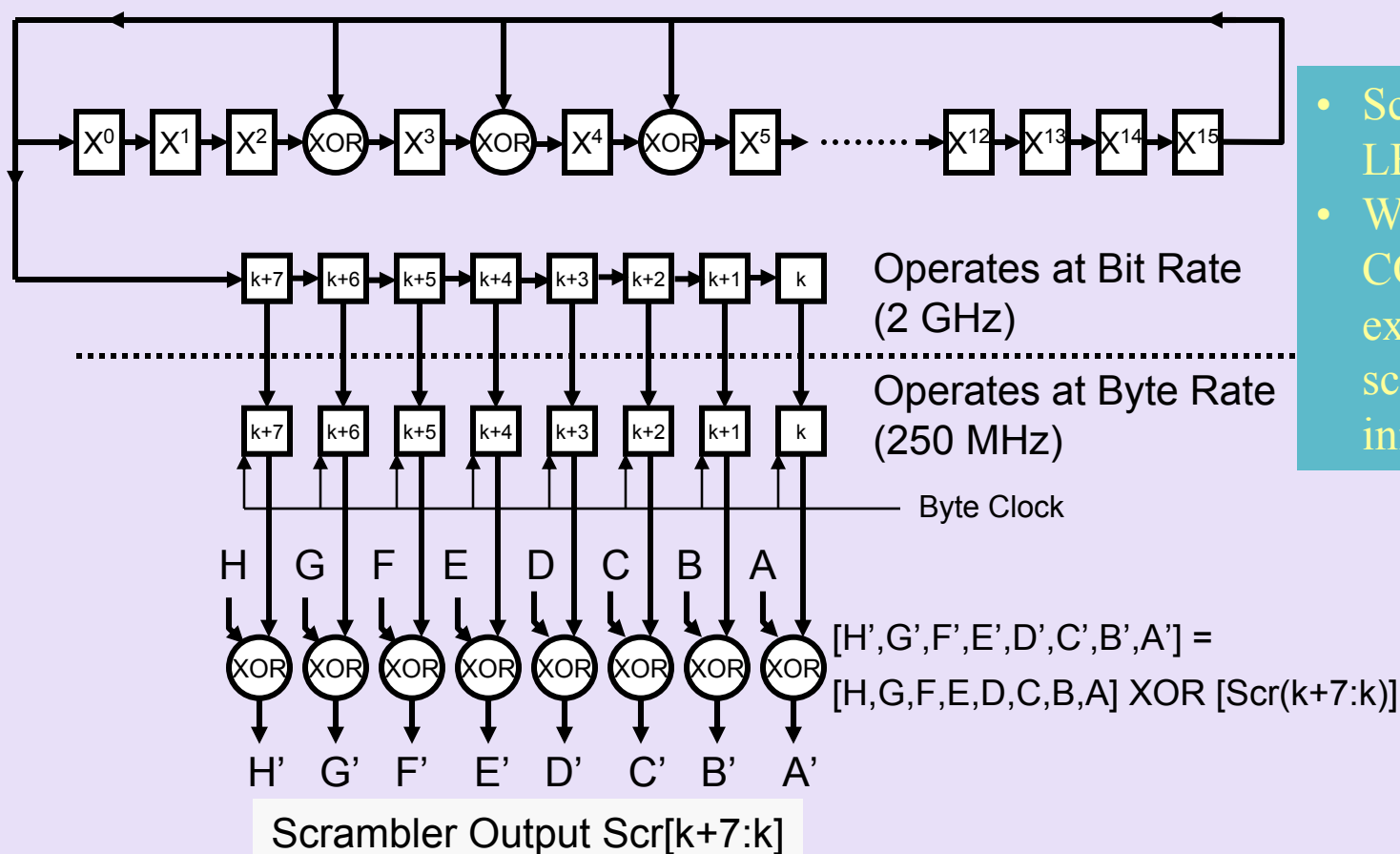
To Data Link Layer



# Scrambler Operation

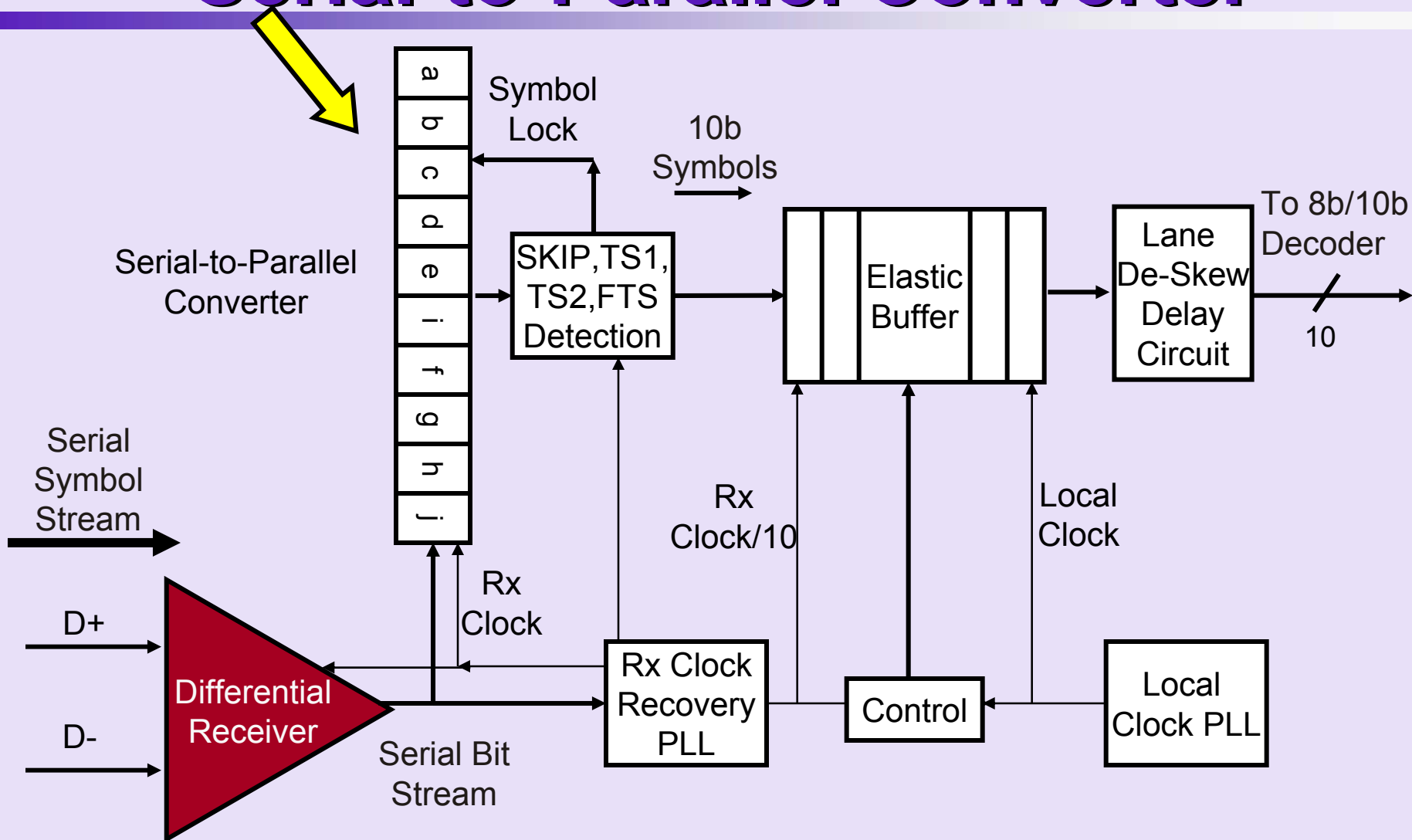
## ■ Scrambling polynomial:

$$G(x) = X^{16} + X^5 + X^4 + X^3 + 1$$

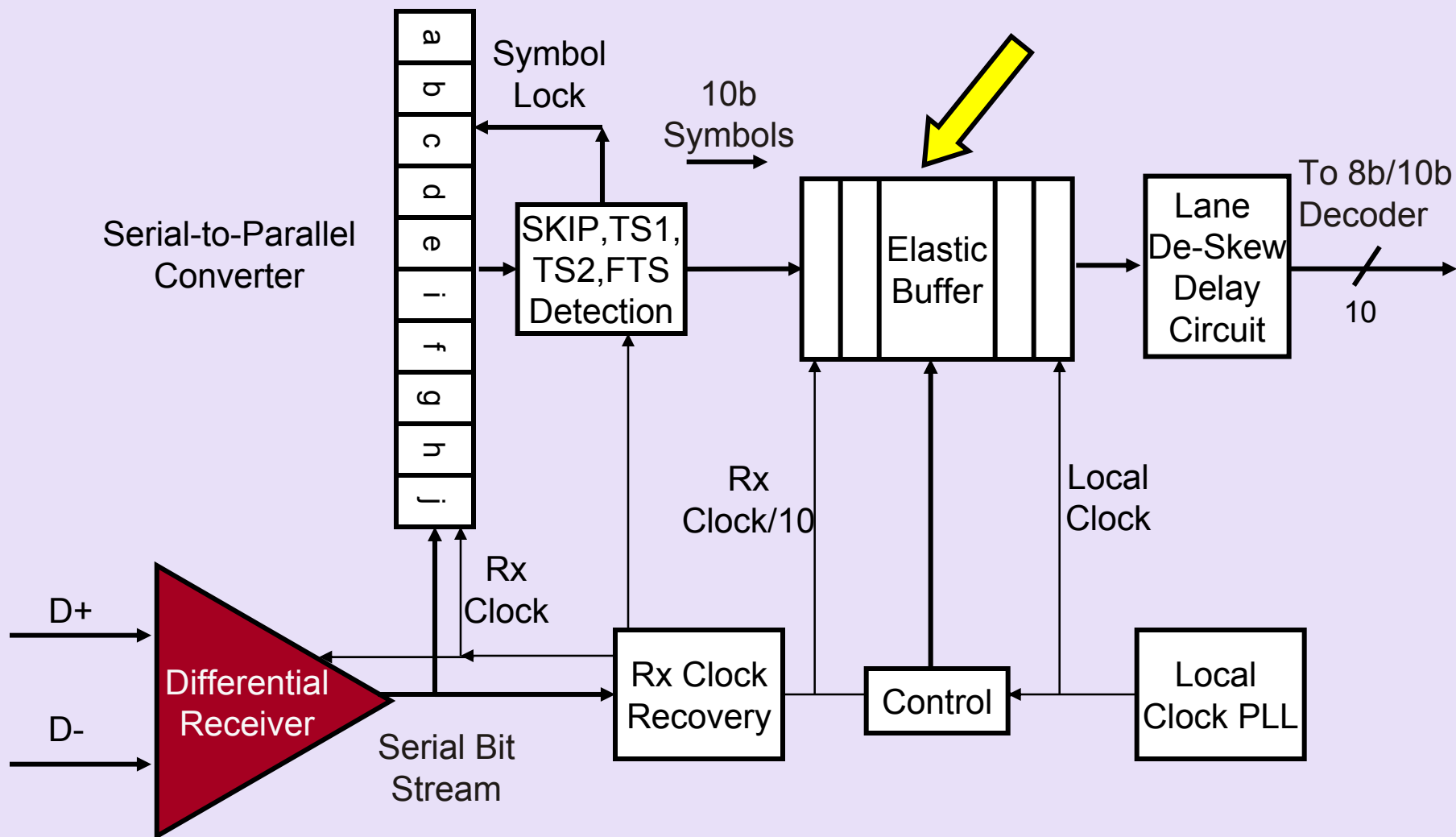


- Scrambler uses LFSR
- Whenever COM character exits scrambler, scramble is initialized

# Serial-to-Parallel Converter



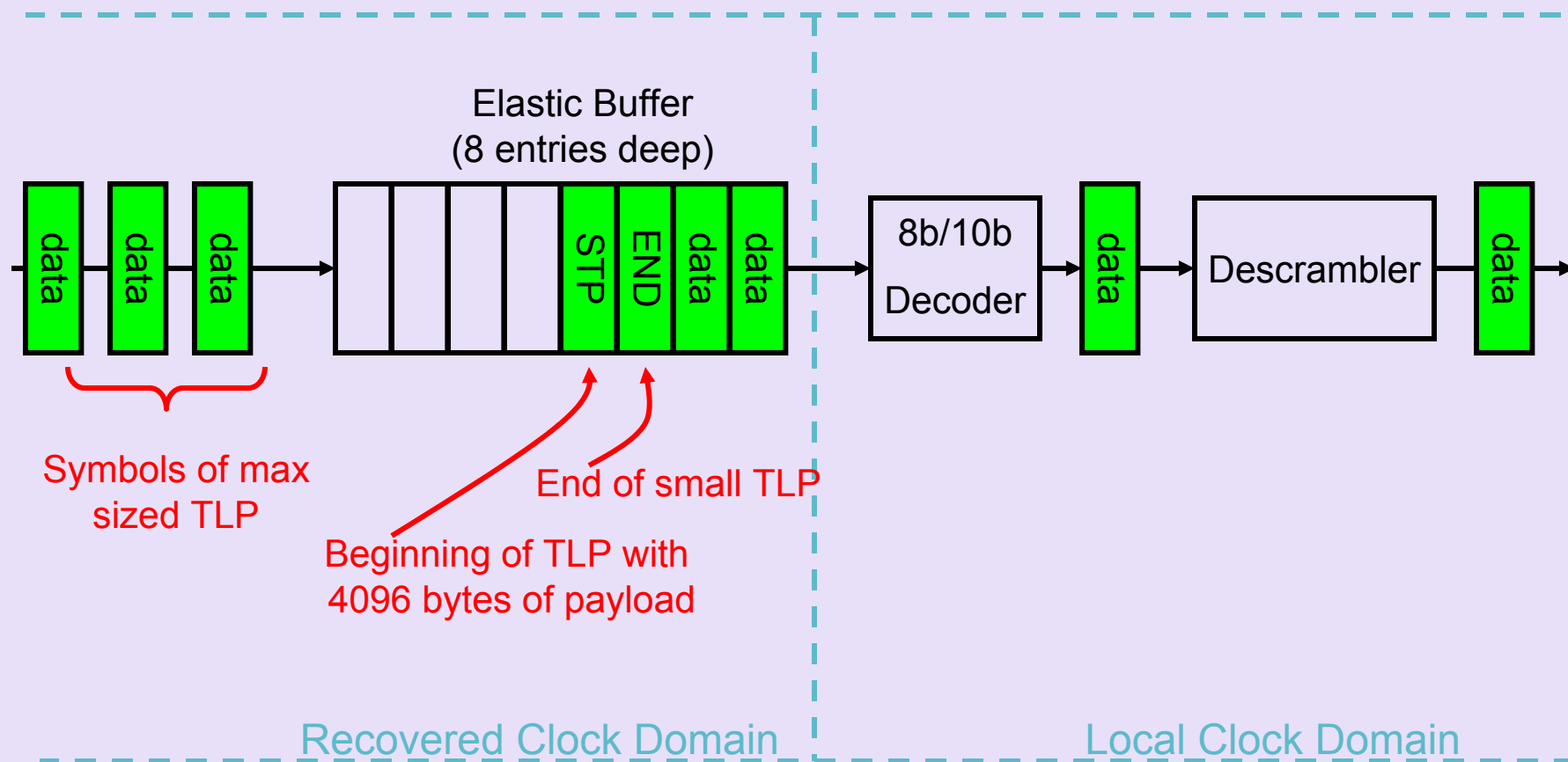
# Elastic Buffer



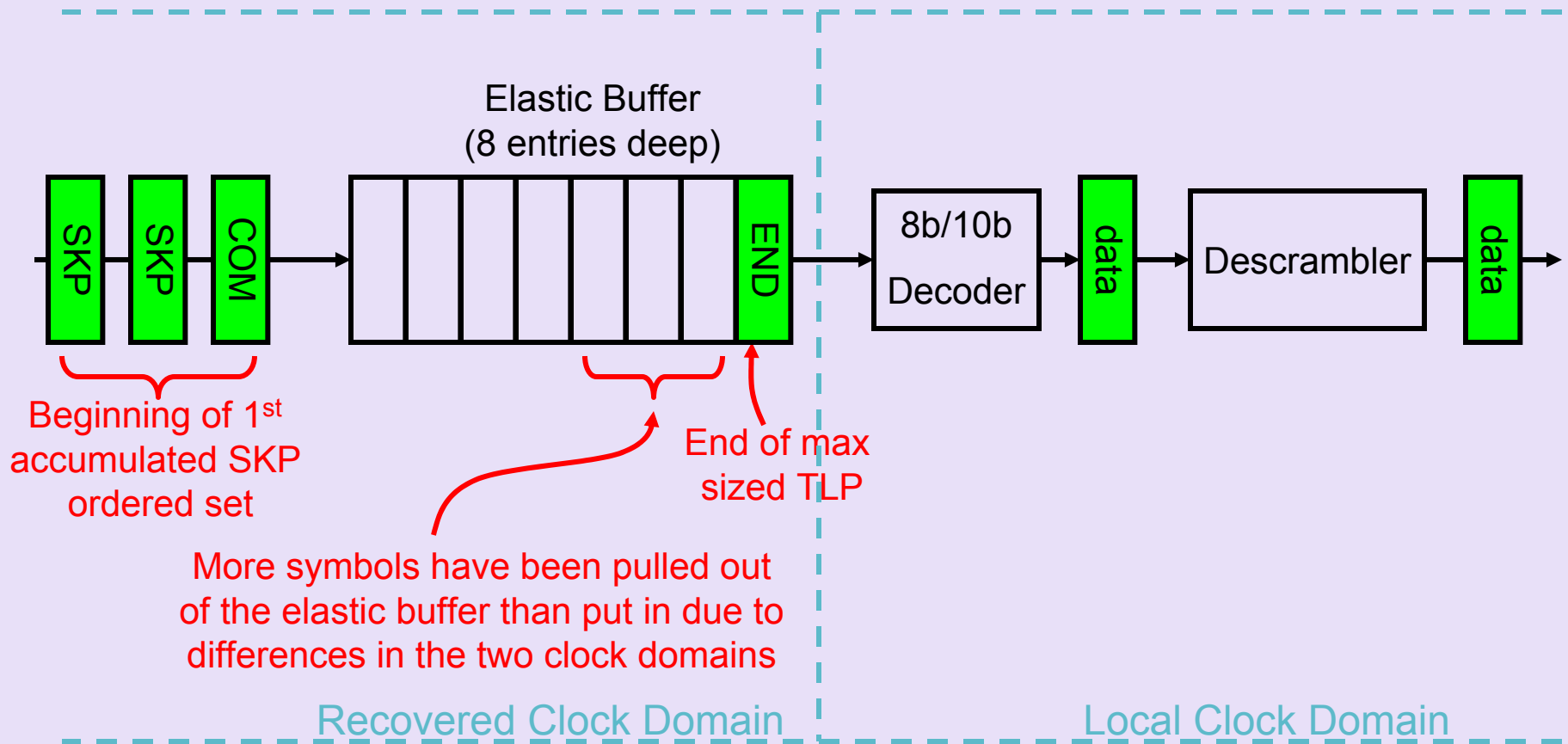
# Clock Tolerance Compensation

- Skip ordered-set used to compensate for differences in frequency of bit rate a packet is transmitted with, and the receiver clock frequency
- Frequency difference no greater than 600 ppm
- Skip ordered-set scheduled to be inserted every 1180 to 1538 symbol times and transmitted on a packet boundary.

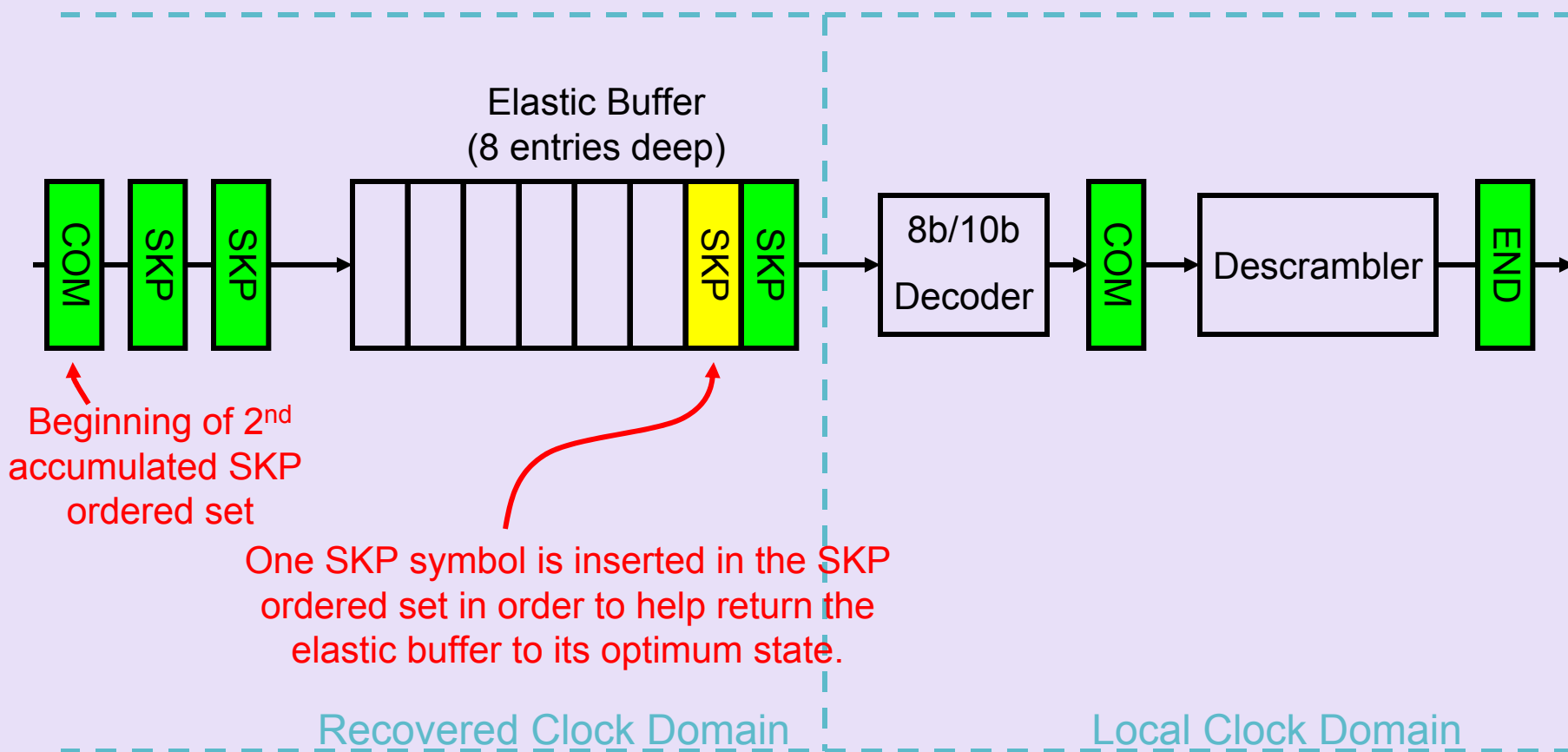
# Elastic Buffer Option 1, Example 1: Local Clock Faster than Recovered Clock



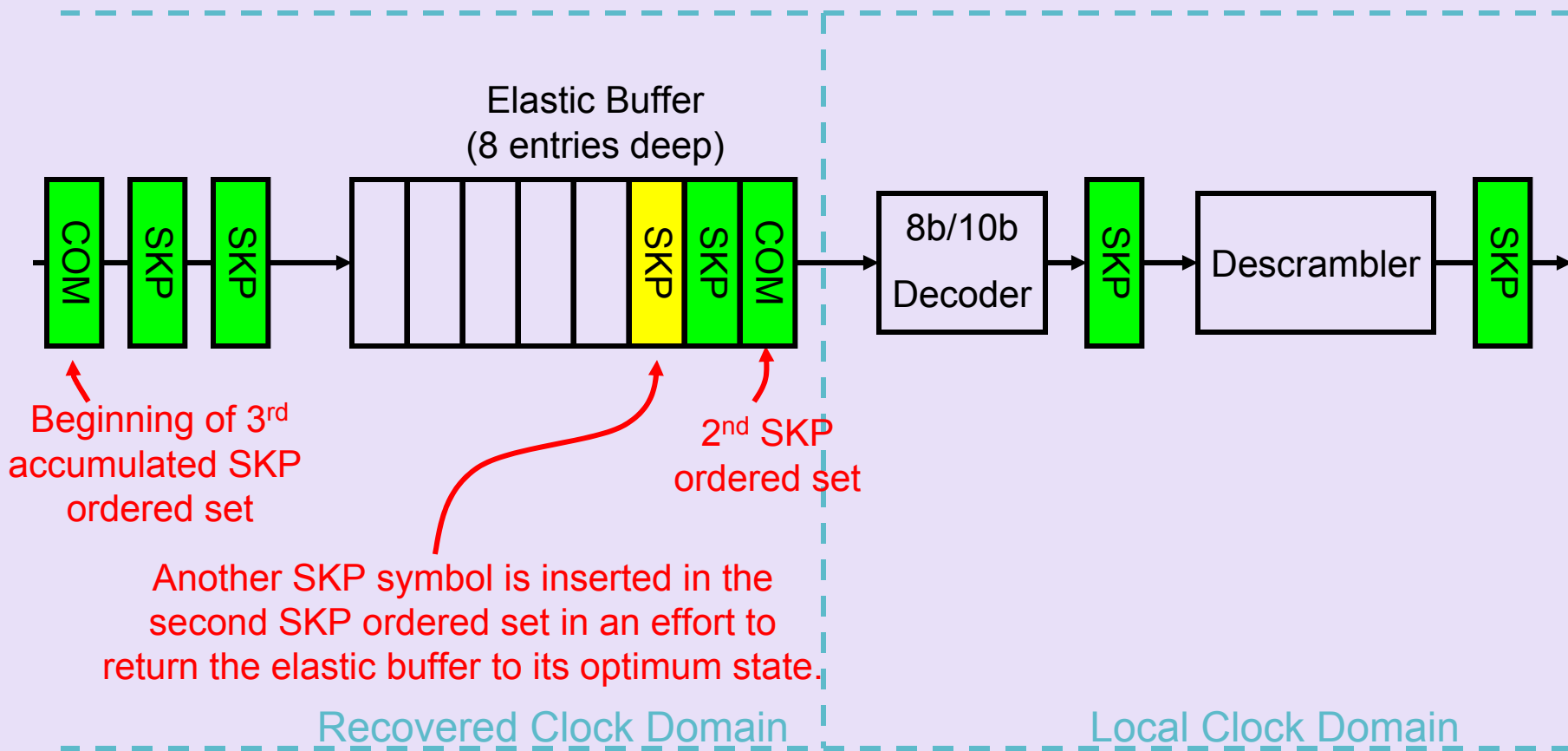
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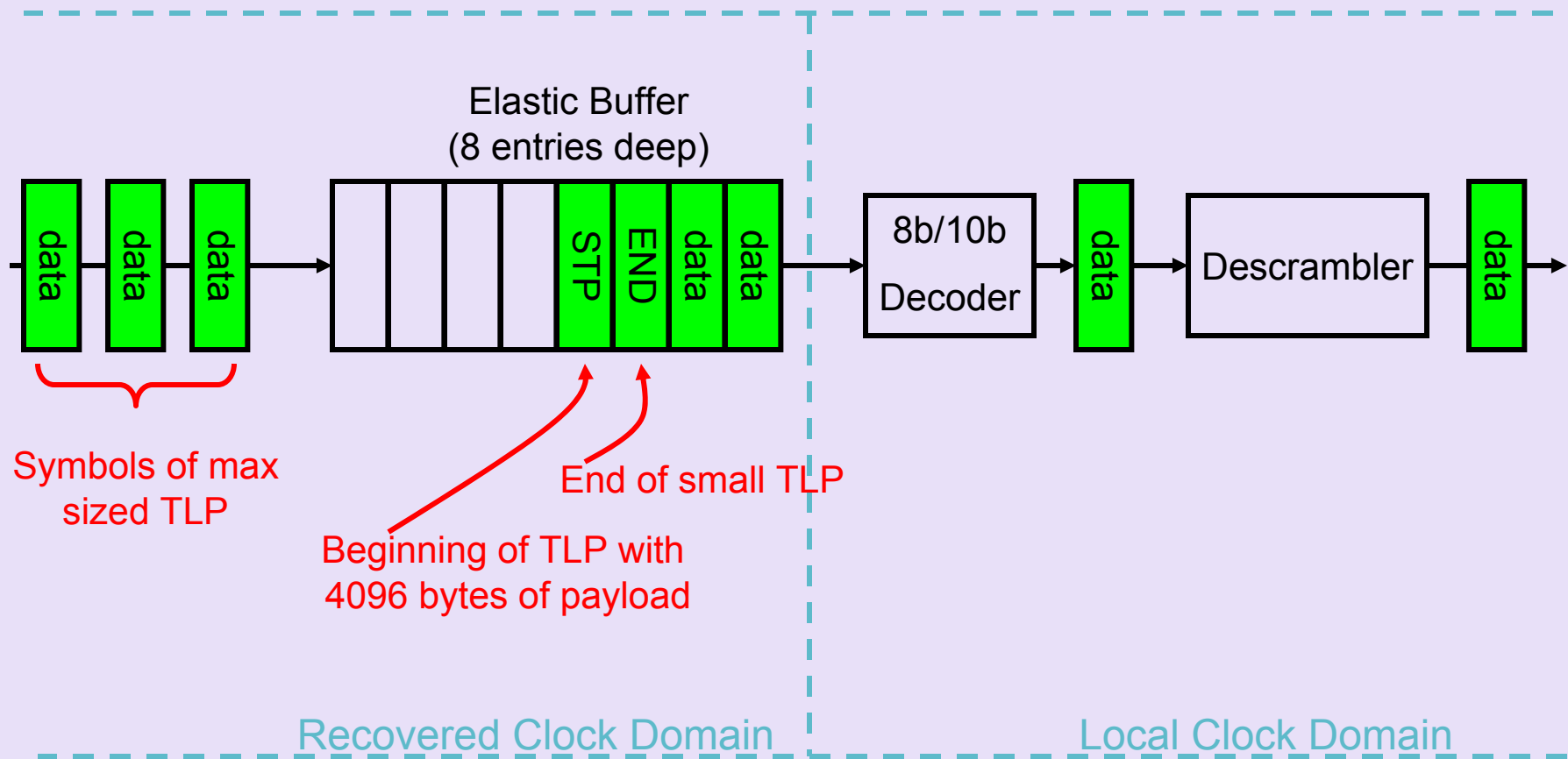
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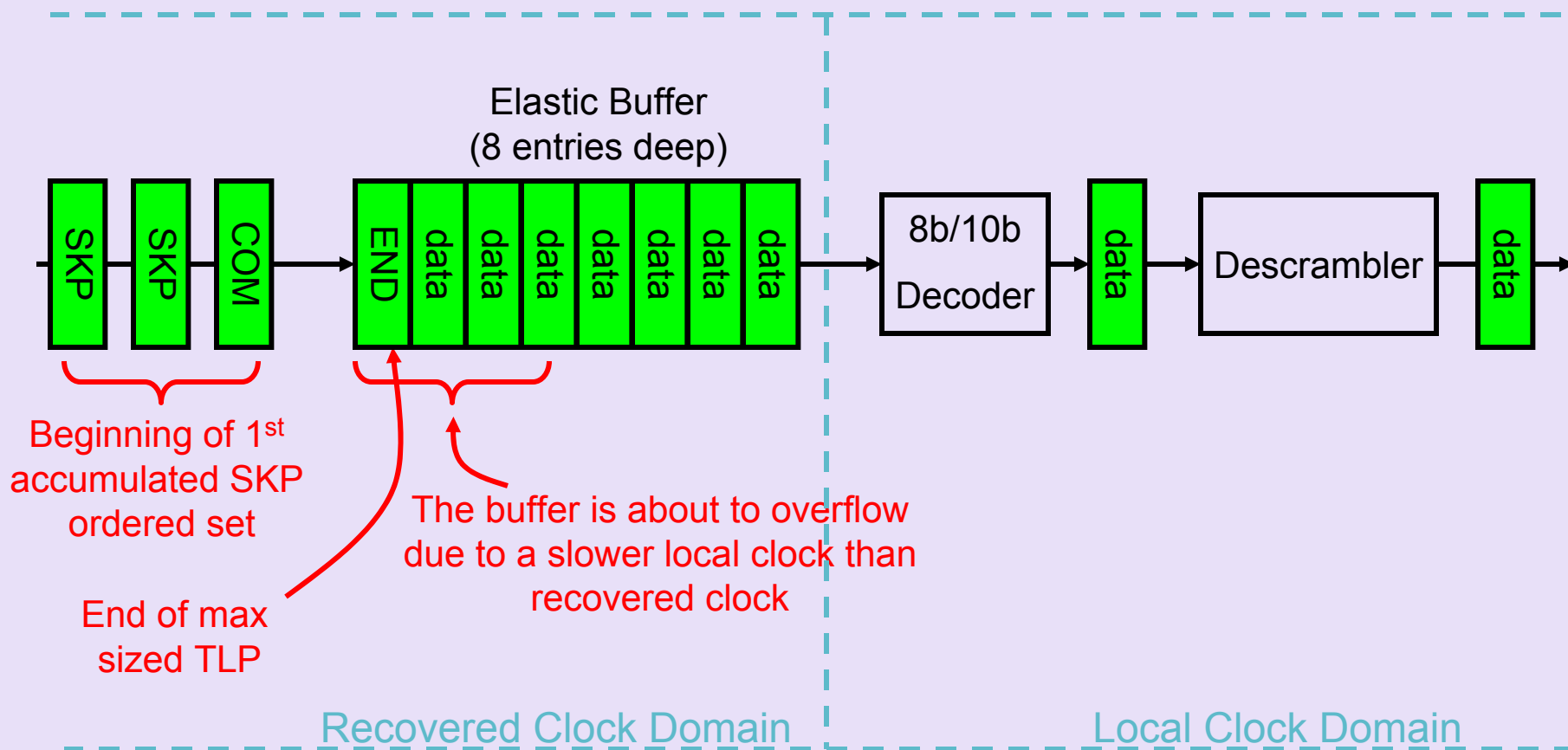
# Elastic Buffer Option 1, Example 1: Local Clock Faster than Recovered Clock



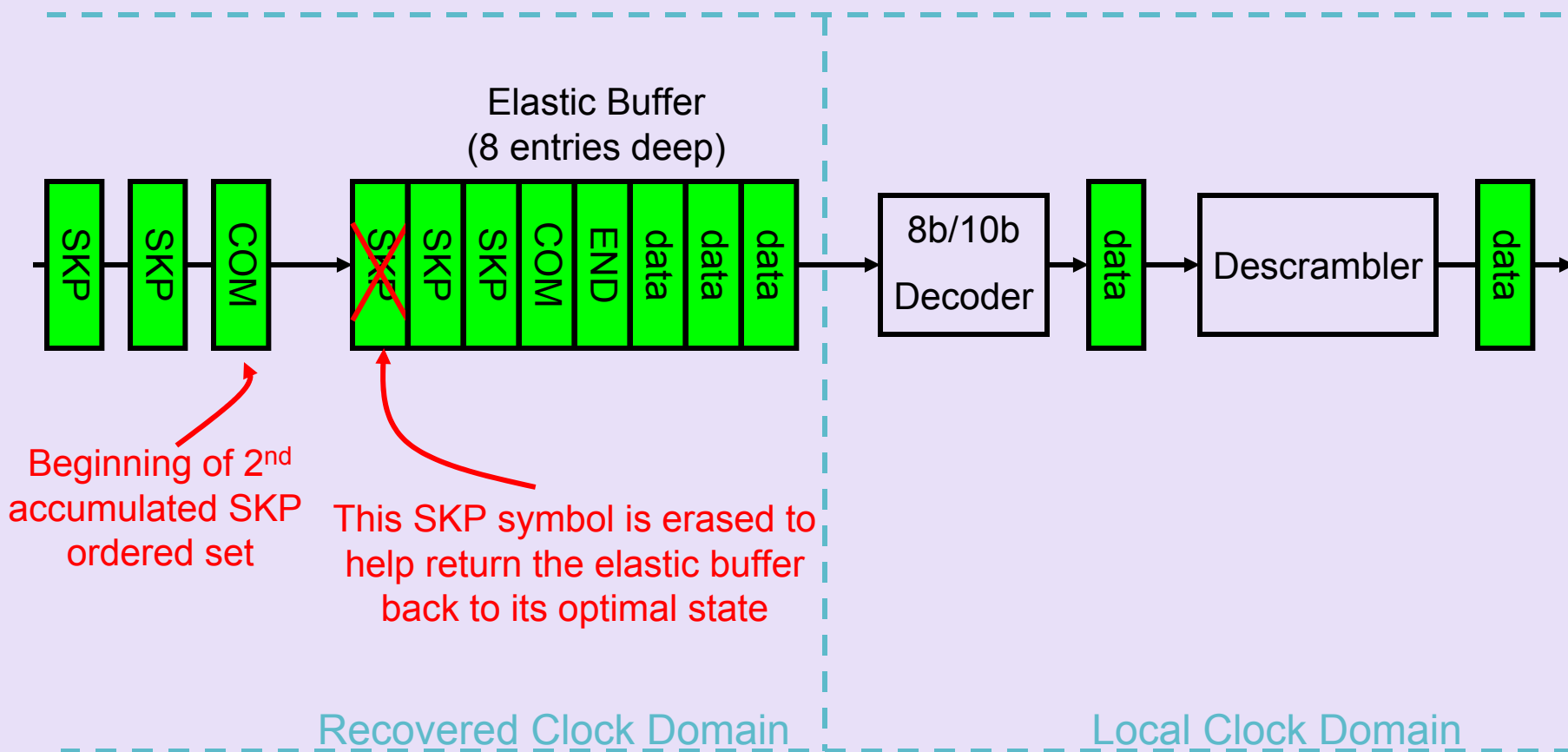
# Elastic Buffer Option 1, Example 2: Local Clock Slower than Recovered Clock



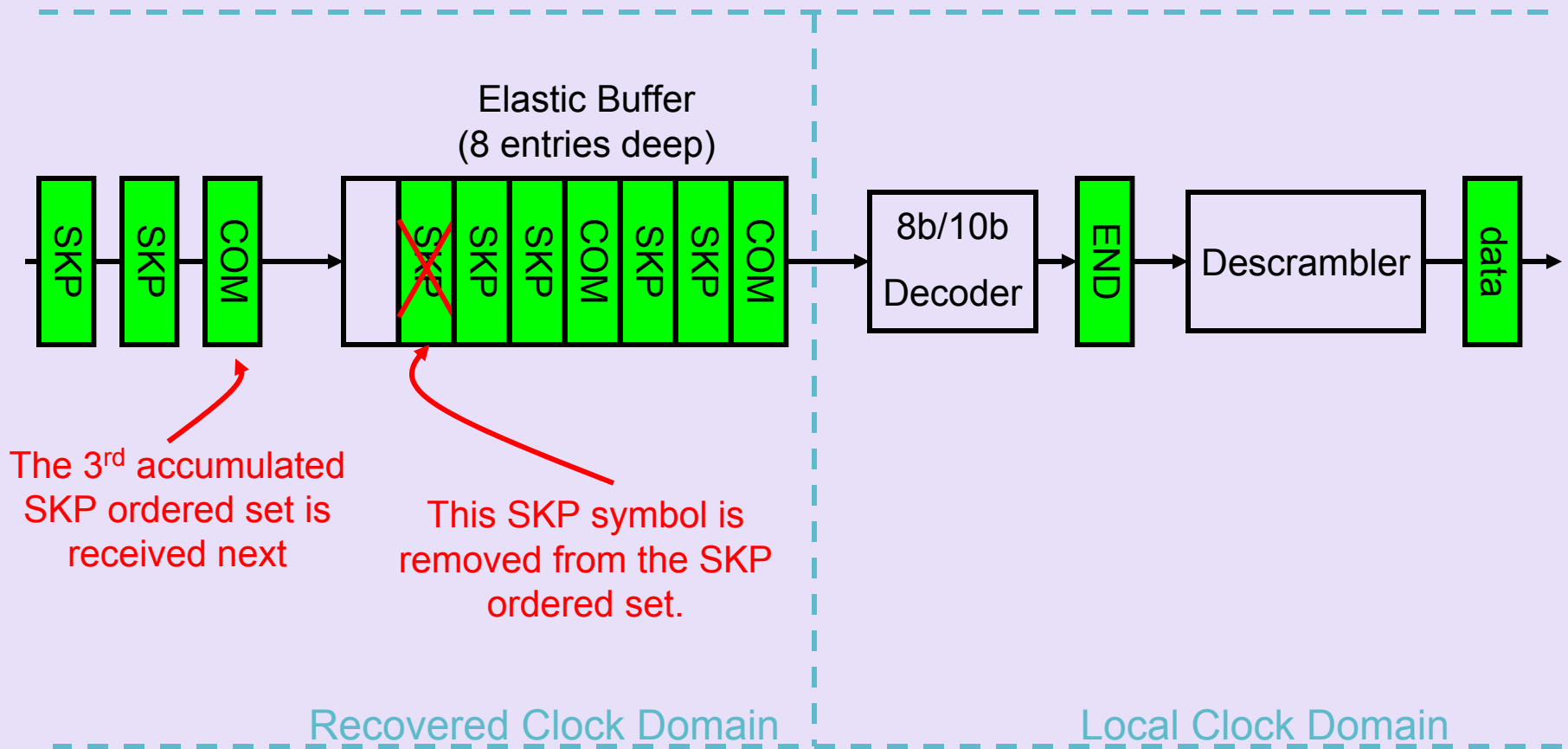
# Elastic Buffer Option 1, Example 2: Local Clock Slower than Recovered Clock



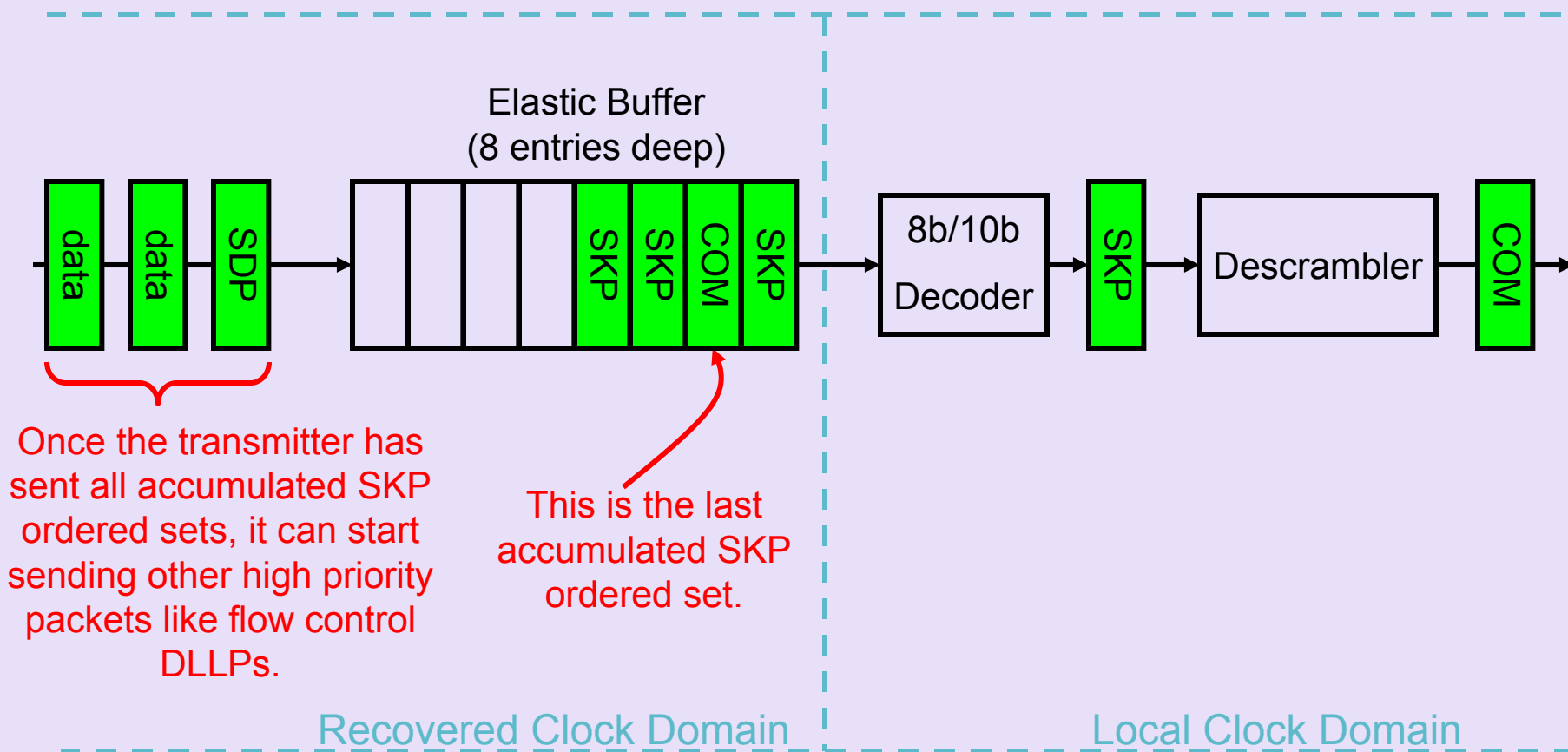
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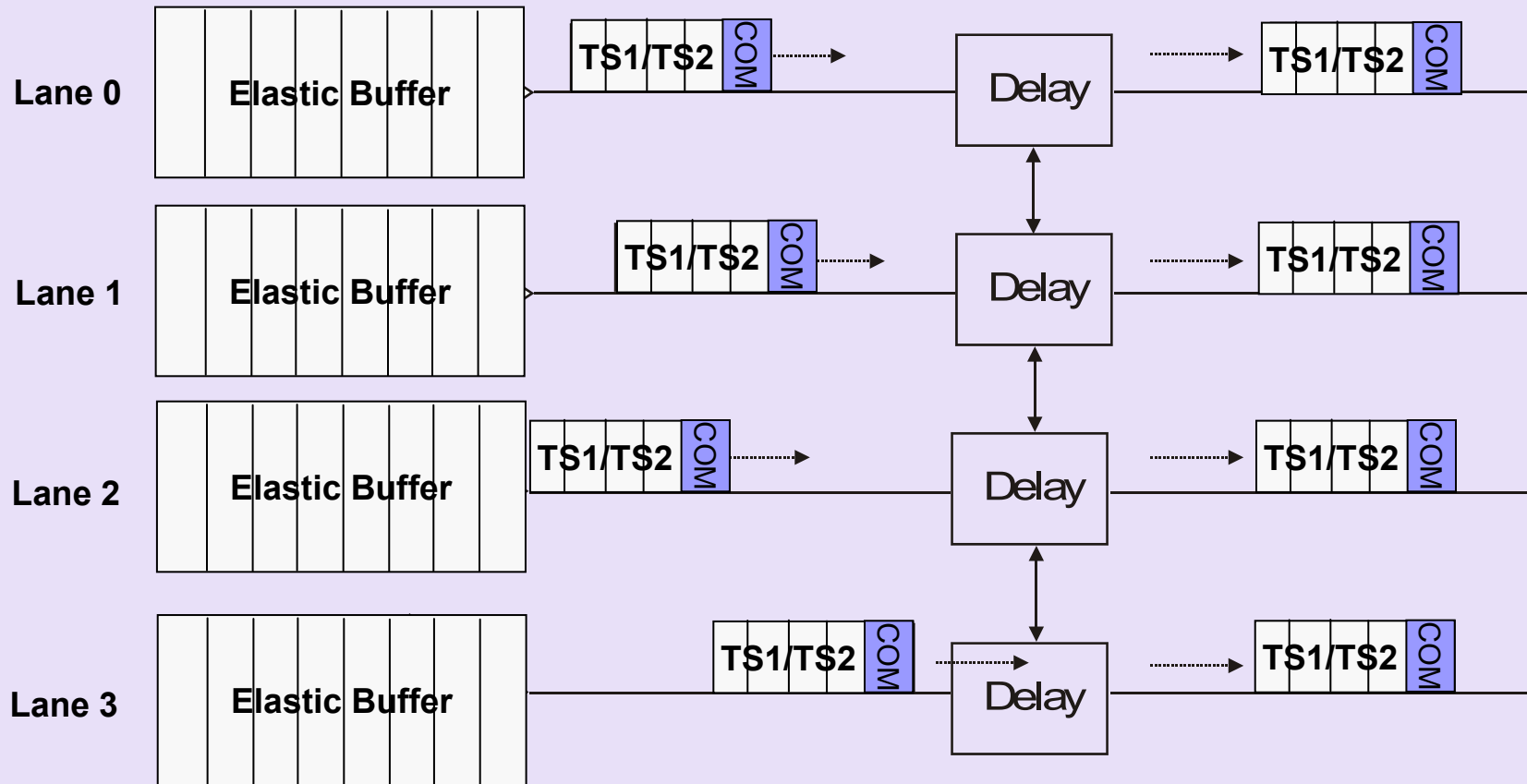
# Elastic Buffer Option 1, Example 2: Local Clock Slower than Recovered Clock



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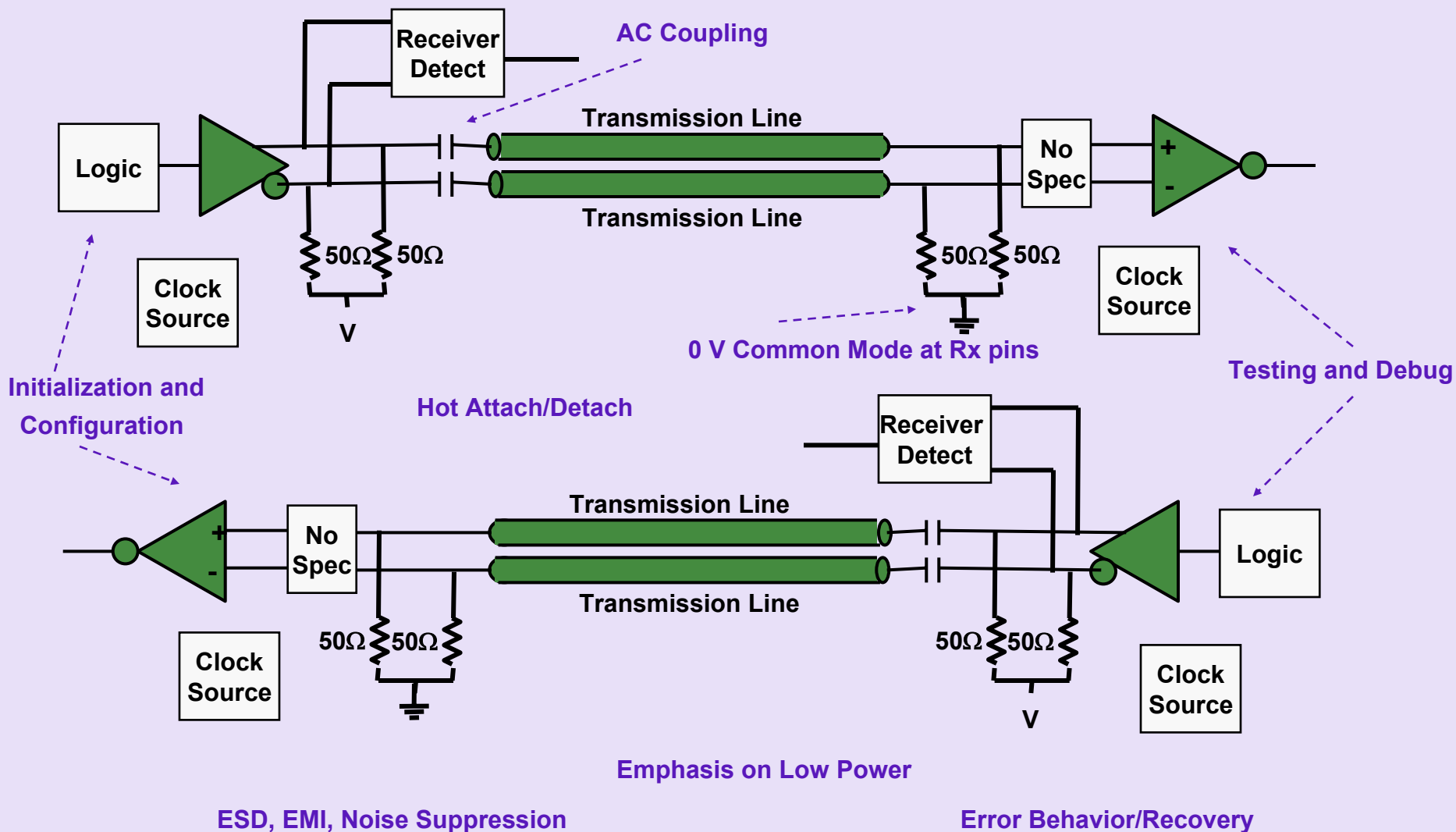
# Receiver Link De-Skew



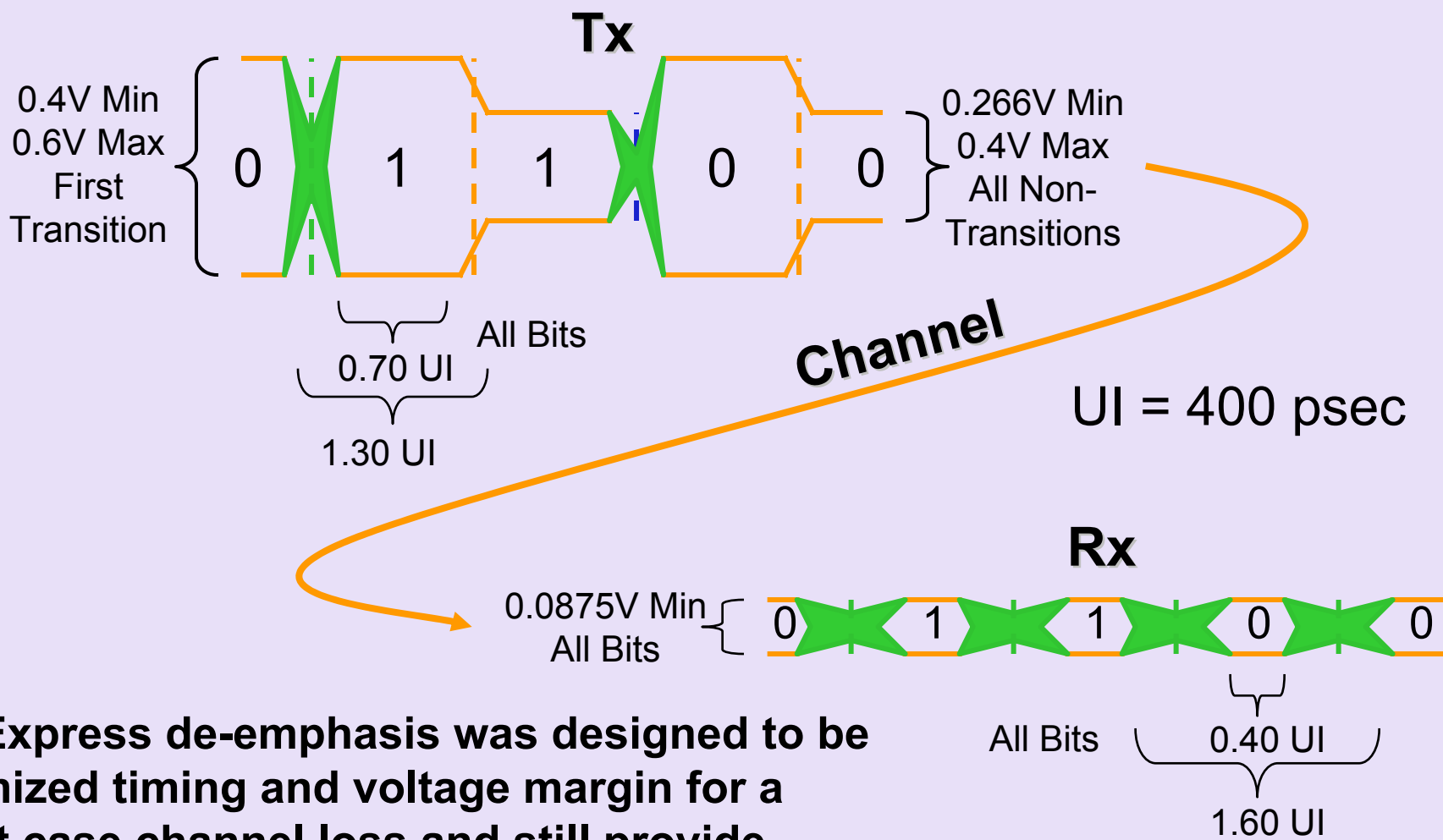
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- Layout Considerations

# Pictorial Summary

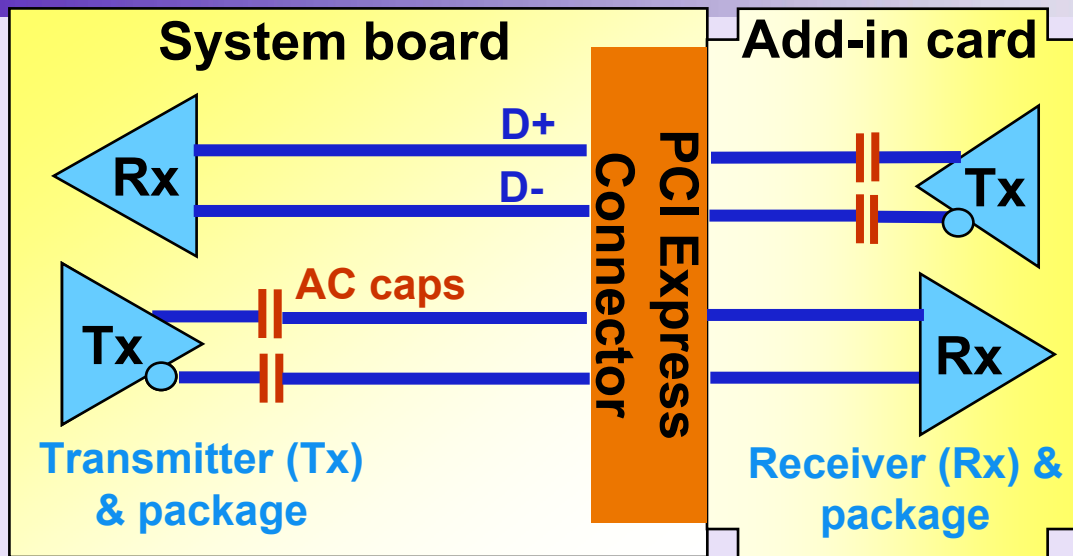


# Electrical Specifications

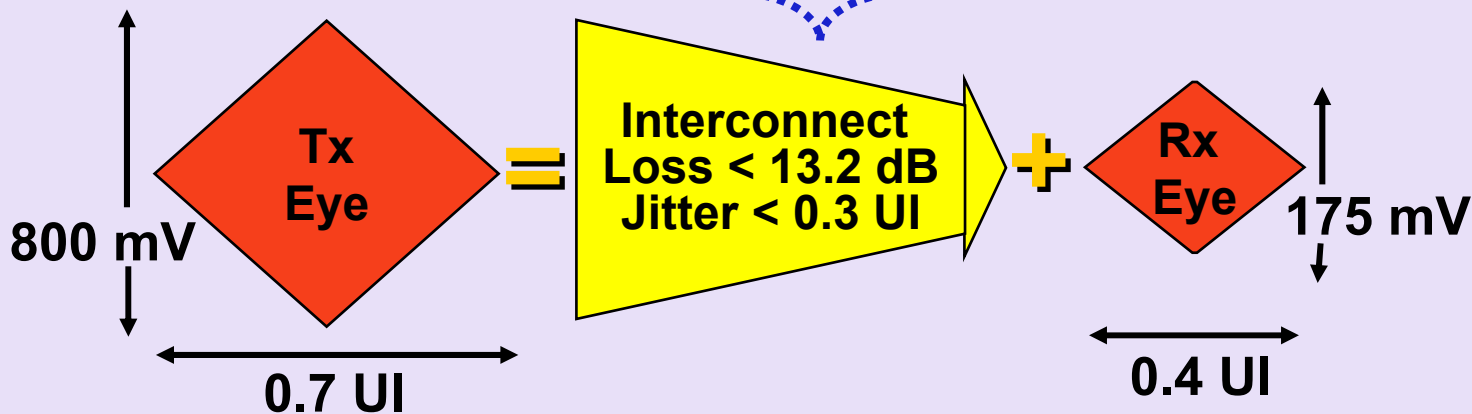


**PCI Express de-emphasis was designed to be optimized timing and voltage margin for a worst case channel loss and still provide adequate margin for the best case channel loss**

# System Budget



- ✓ Differential pairs
- ✓ AC coupled
- ✓ Lane-to-lane de-skew
- ✓ Polarity inversion
- ✓ On-chip equalization
- ✓ On-chip terminations

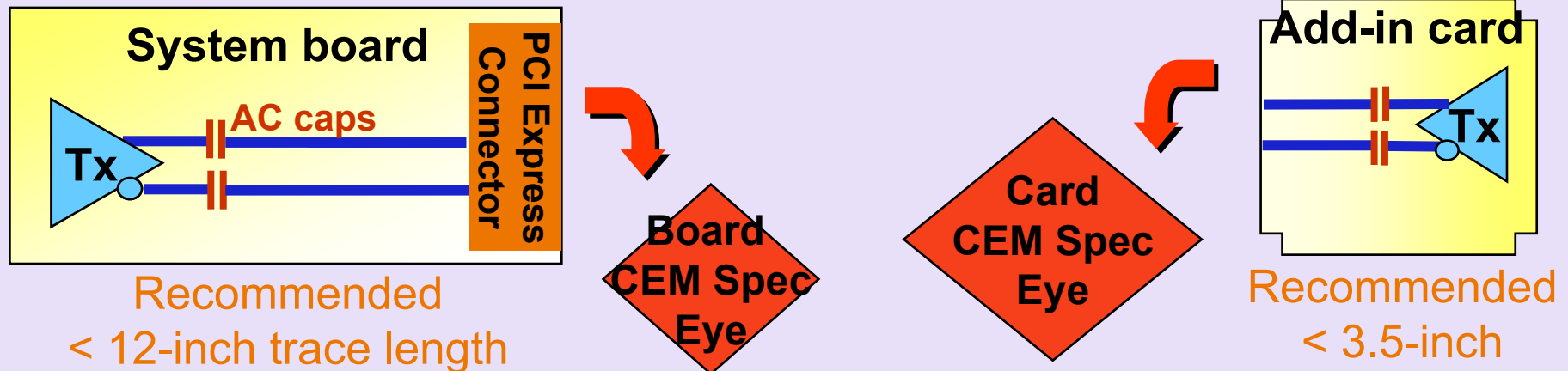


UI = Unit Interval as defined in the PCI Express Base 1.0a Specification

# Card Electromechanical Interconnect Budget

## ■ Card Electromechanical (CEM) 1.0a specification defines budget allocation

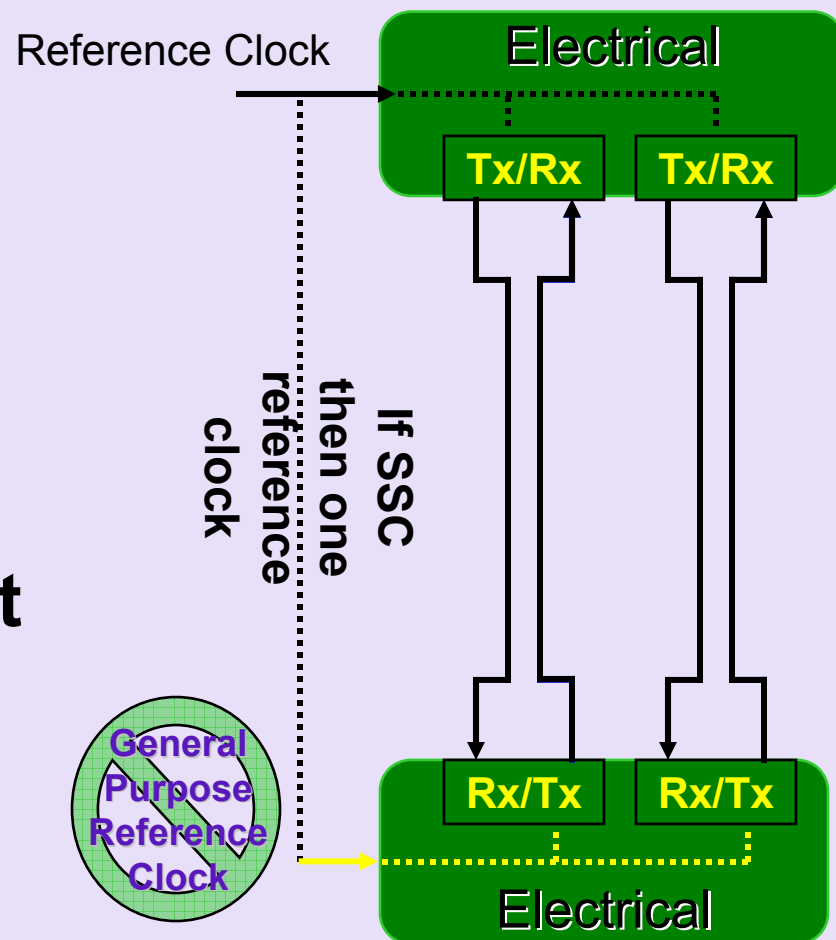
- ✓ Loss and *jitter* are key parameters
- ✓ Target impedance not as critical
- ✓ Maintain differential pair symmetry
- ✓ Design tradeoffs: loss vs. trace length, etc.



**Manage loss & jitter to meet budget**

# Clocking Options

- All lanes within a port must transmit data using one frequency
- The ports at each end of a link may transmit data at slightly different frequencies
  - ✓ Tolerance =  $\pm 300$  ppm each



**If SSC used to modulate data rate, then both ports must use same modulated clock source**

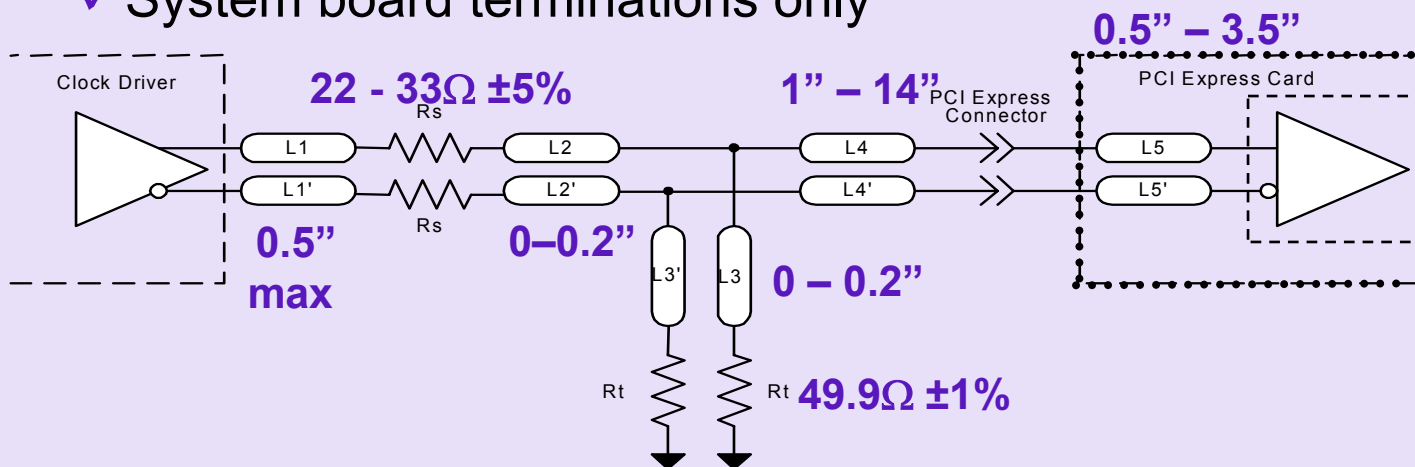
# Reference Clock Routing

## ■ Differential clock routing to each device and connector

- ✓ Use the same differential trace geometries
- ✓ Length matching to different devices *NOT* required!

## ■ Clock driver requirements

- ✓ 100MHz with SSC support (e.g. CK410)
- ✓ Choose low jitter components
- ✓ System board terminations only



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# Link Initialization and Training

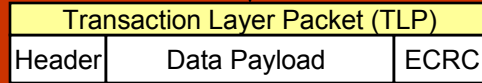
Core/Software layer

Memory, I/O, Configuration R/W Requests or Message Requests or Completions  
(Software layer sends / receives address/transaction type/data/message index)

Transmit

Receive

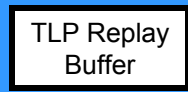
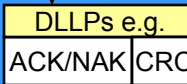
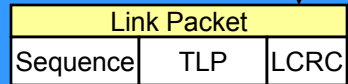
Transaction layer



Transmit  
Buffers  
per VC

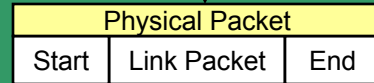
Flow Control  
Virtual Channel  
Management  
Ordering

Data Link layer



Mux

Physical layer



Encode

Parallel-to-Serial  
Differential Driver

Port

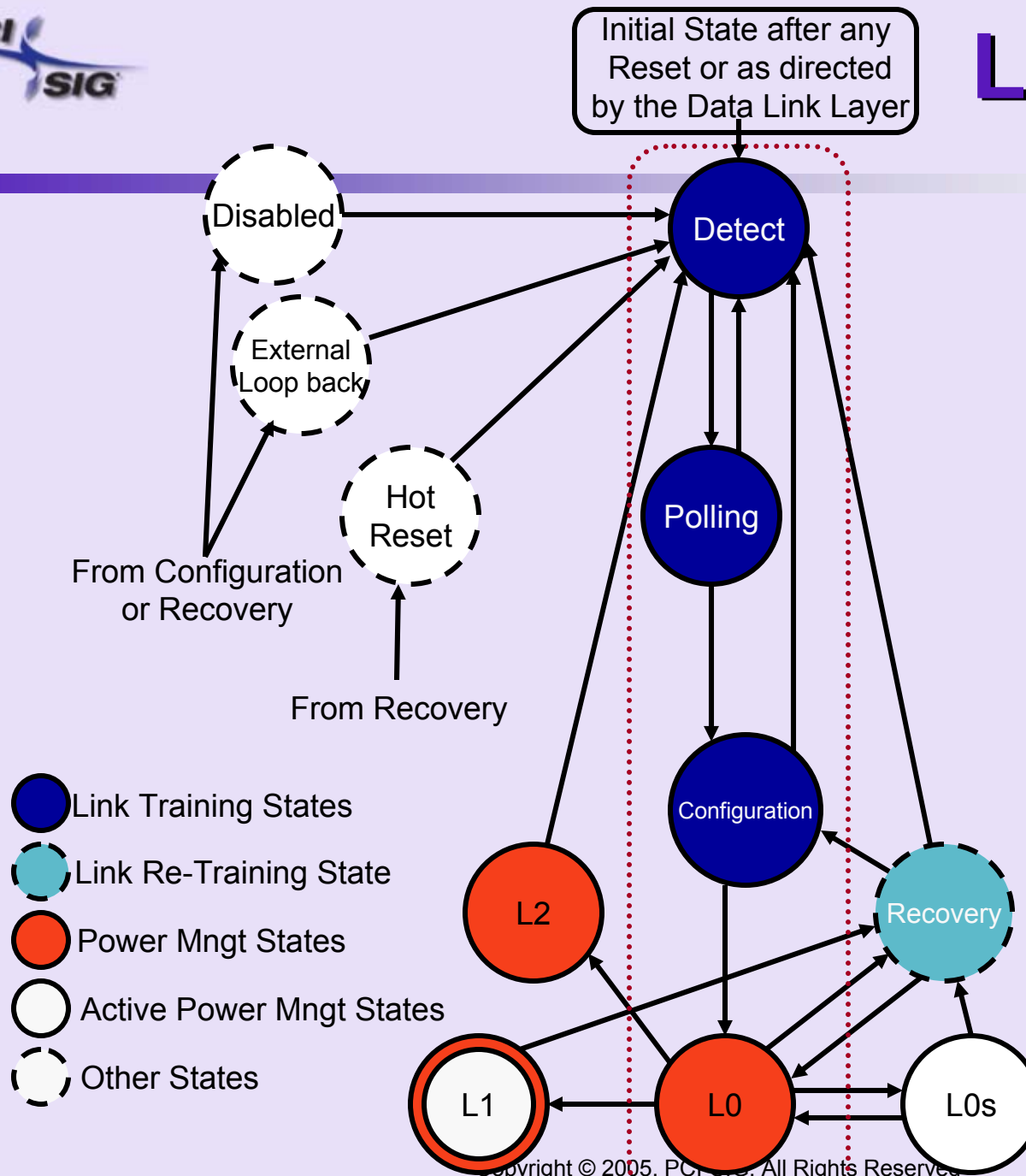
Link  
Training  
(LTSSM)

Decode

Serial-to-Parallel  
Differential Receiver

## Purpose of Link Training

- Receiver detection
- Bit lock
- Symbol lock
- Polarity inversion
- Link data rate
- Link width
- Lane reversal
- Link Numbers (on multi-Link device)
- Lane Numbering
- Lane-to-lane de-skew

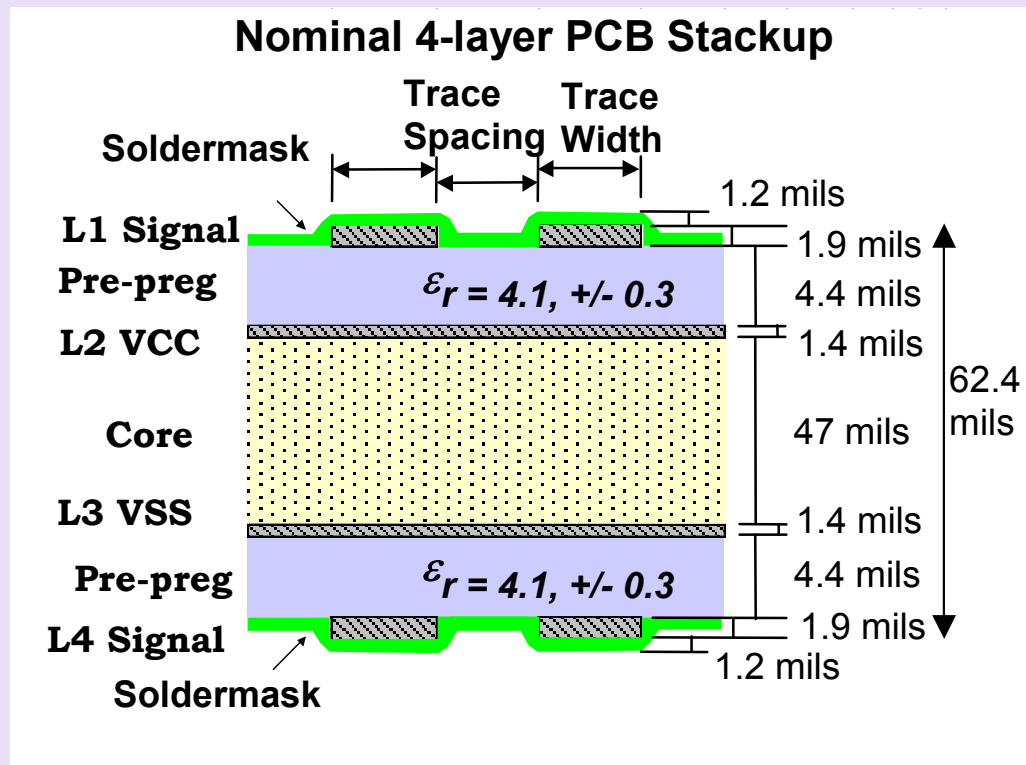


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# Stackup Design

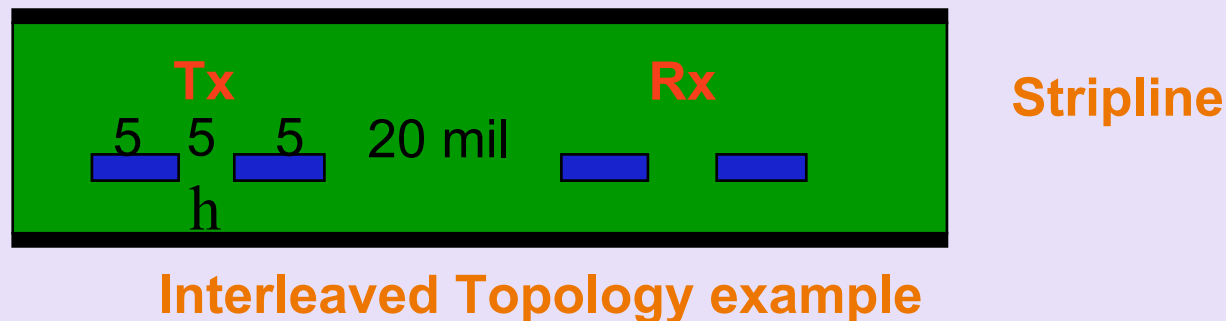
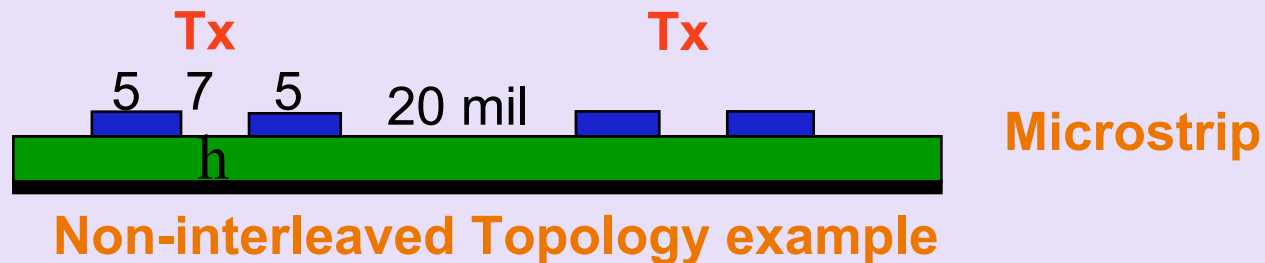
- No new PCB technology required
- Standard 4-layer stackup 0.062" thick PCB
- Microstrip 1/2 oz Cu plated **Ok**
- Stripline 1 oz Cu (6+ layers) **Better**



**Follow simple layout rules & design tradeoffs**

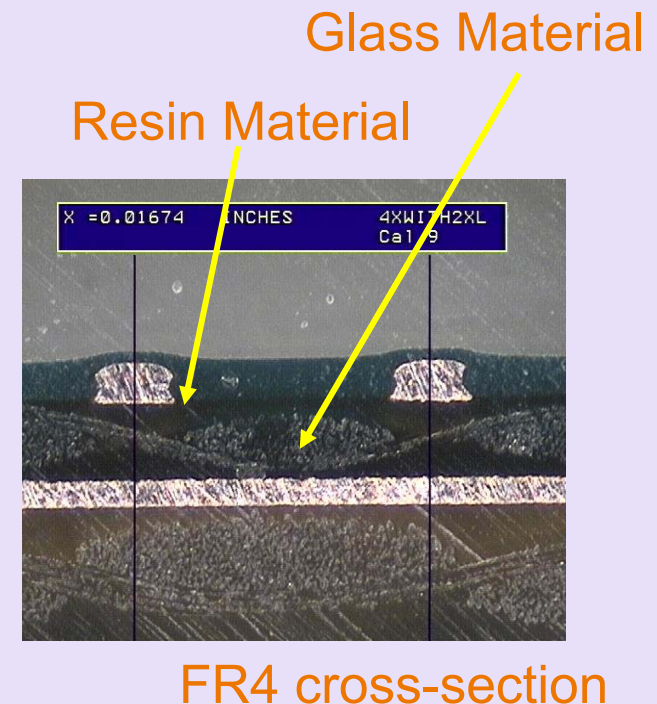
# Trace Geometry & Impedance

- Use wider trace width  $\Rightarrow$  Minimize loss
- Use wider traces for long routes
- More pair-to-pair spacing  $\Rightarrow$  Minimize crosstalk
- Target differential  $Z_0$  of  $100\ \Omega \pm 20\%$



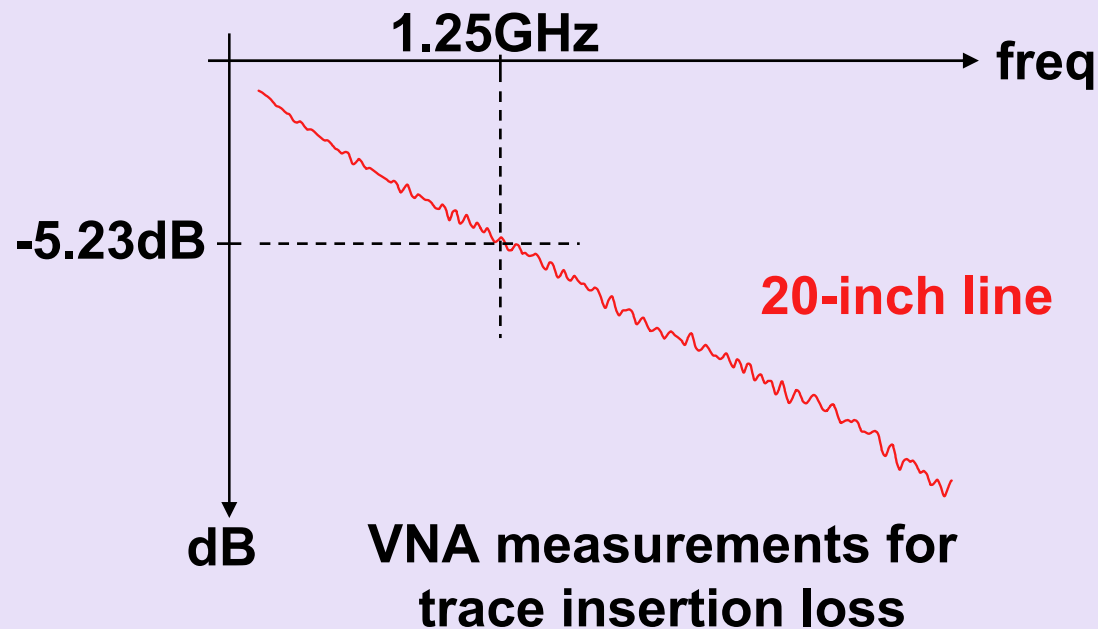
# PCB material dominates loss

- Stackup FR4 material
  - ✓ Copper roughness  $\Rightarrow$  loss  $\uparrow$
  - ✓ Thinner dielectrics  $\Rightarrow$  loss  $\uparrow$
- Non-homogeneous dielectric
  - ✓ Localized  $Z_0$  variation due to material weave  $\Rightarrow$  loss  $\uparrow$
- Wide differential Impedance variation on  $\mu$ strip
  - ✓ Etching and Plating process  $\Rightarrow$  loss  $\uparrow$



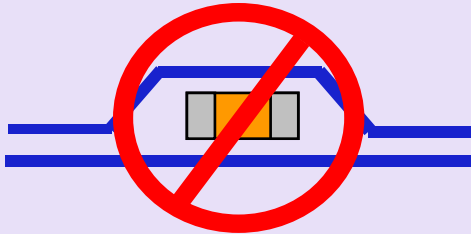
# Trace length

- Longer trace length  $\Rightarrow$  loss  $\uparrow$
- 0.25 to 0.35 dB inherent loss per inch for FR4 microstrip traces
- Limit motherboard trace to  $< 12$  inches and add-in card trace to  $< 3$  inches

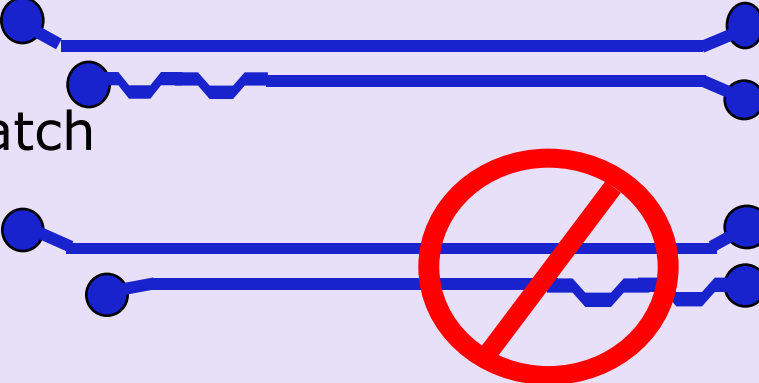


# Trace Symmetry & Matching

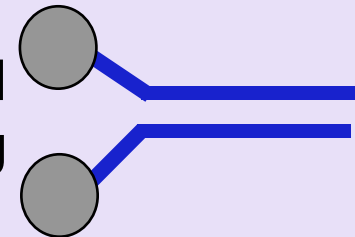
- Match each differential pair per segment
  - ✓ Match overall length  $\leq 5$  mils
  - ✓ Symmetric routing for each pair



Match  
near  
mismatch

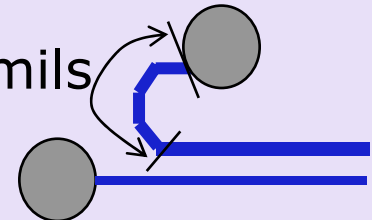


Preferred  
matching



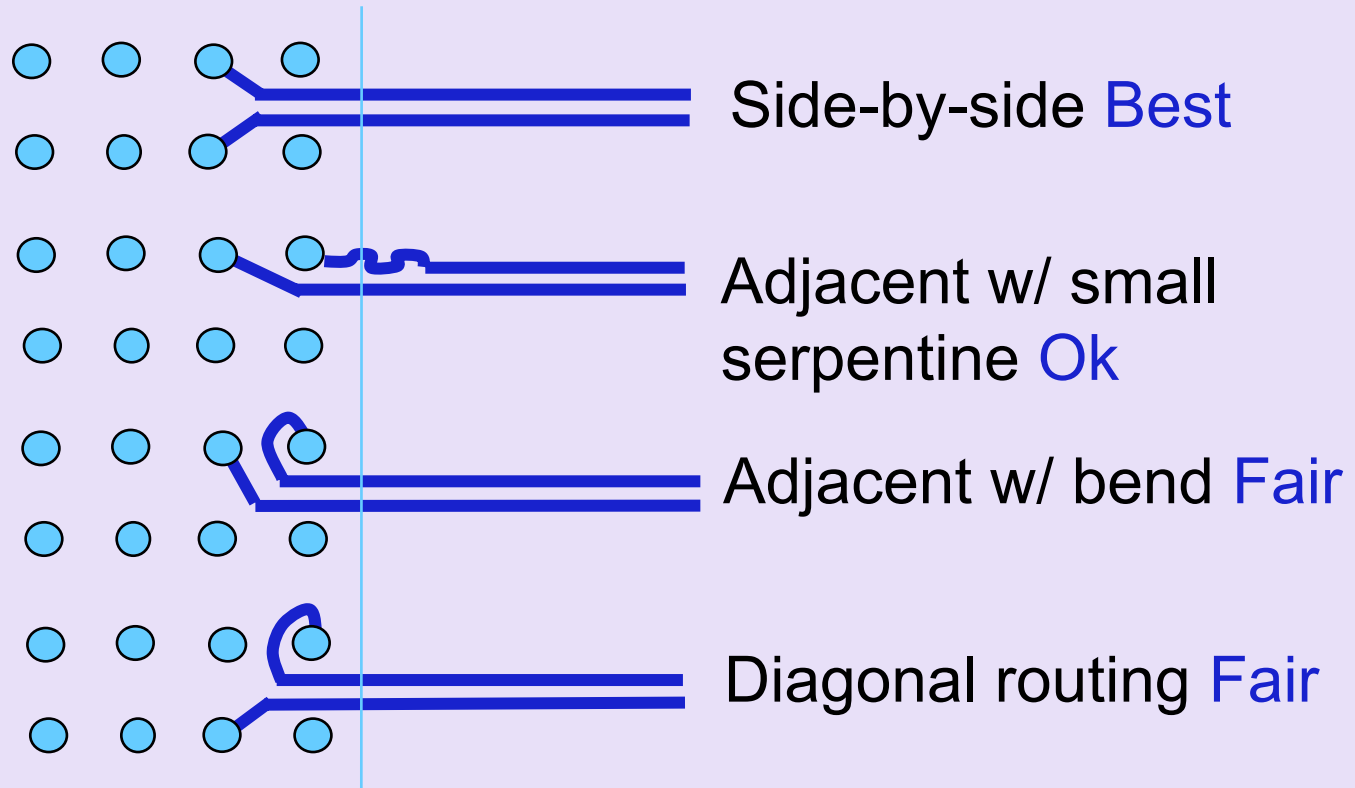
$\leq 45$  mils

Alternative  
matching



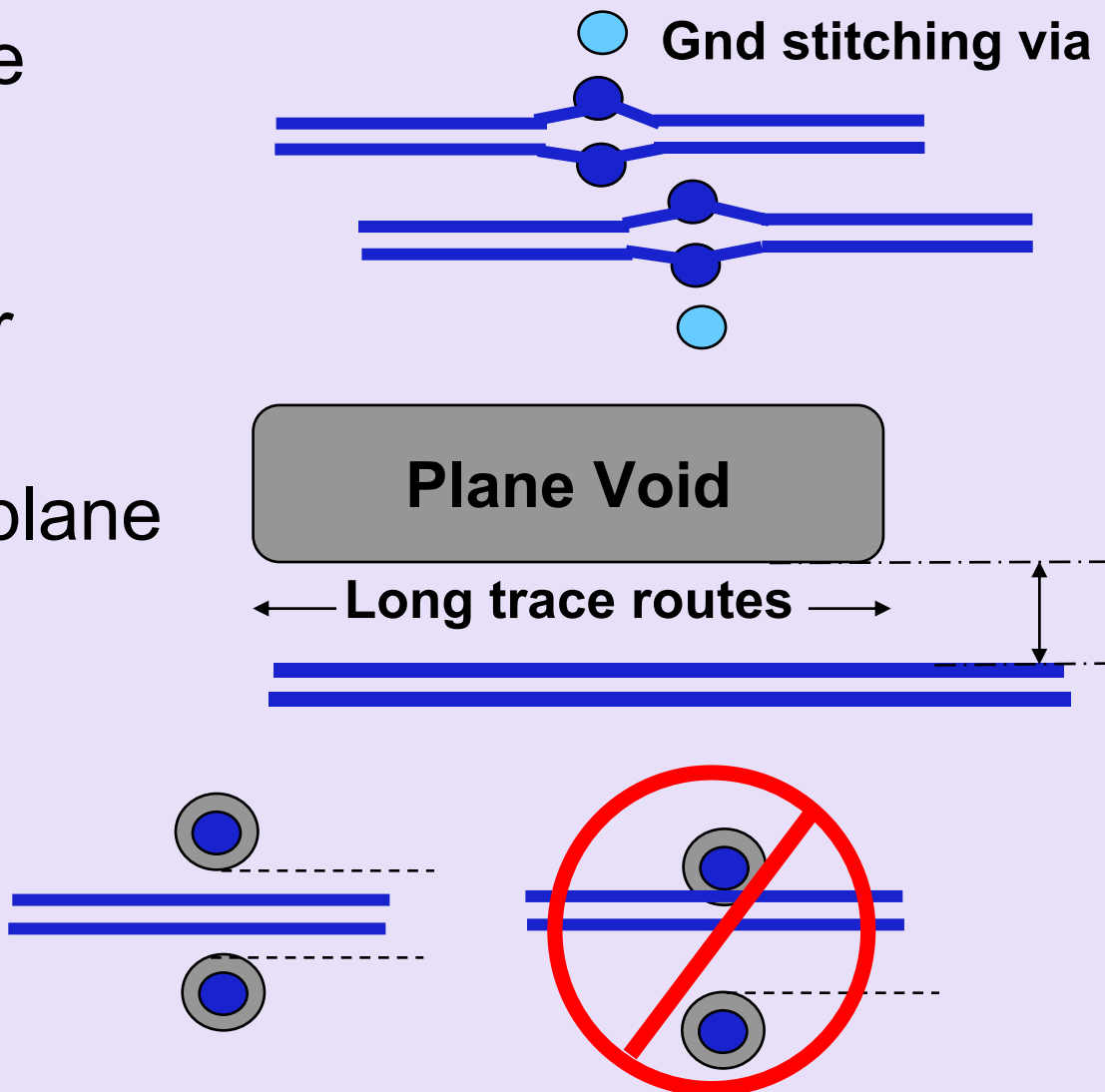
# Pin field breakout

- Use side-by-side breakout for package to maintain symmetry
- Avoid tight bends



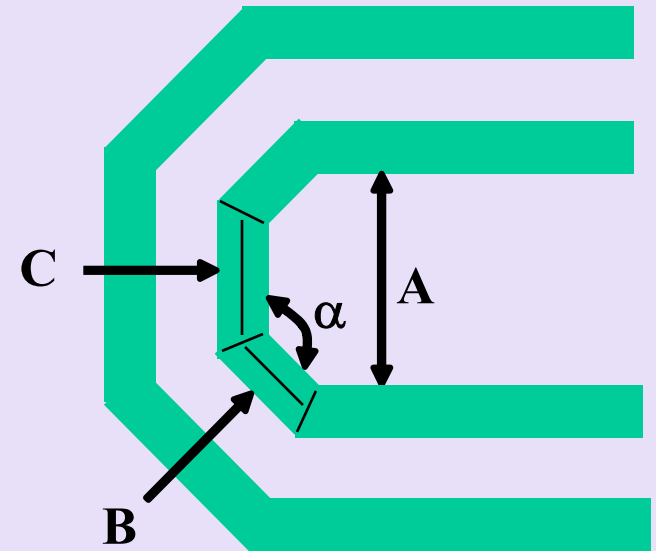
# Reference Plane

- Full ground plane reference
- Stitching vias required for layer transition
- Clearance near plane void
- Avoid trace over anti-pad



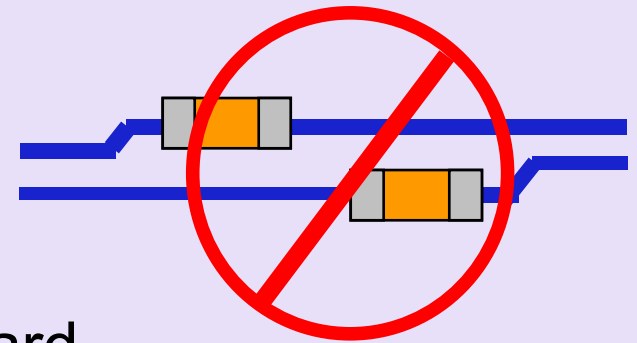
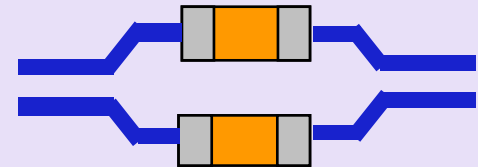
# Bend Guidelines

- Avoid tight bends
  - ✓ No 90° bends; impact to loss and jitter budgets
- Keep angles  $\geq 135^\circ$  ( $\alpha$ )
- Keep minimum air gap
  - ✓  $A \geq 3x$  the trace width
- Length of B and C  $\geq 1.5x$  the width of the trace



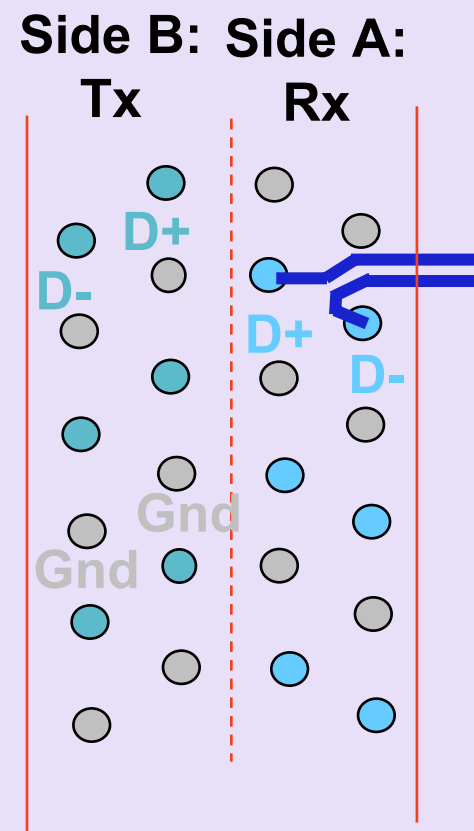
# AC coupling caps

- Size: 0402 **best**, 0603 **ok**
  - No 0805 size or C-packs
  - Symmetric placement
- 
- Cap Size: 0.1uF **best**
  - Cap location:
    - ✓ Along Tx pairs on Motherboard
    - ✓ Along Tx pairs on Add-in card



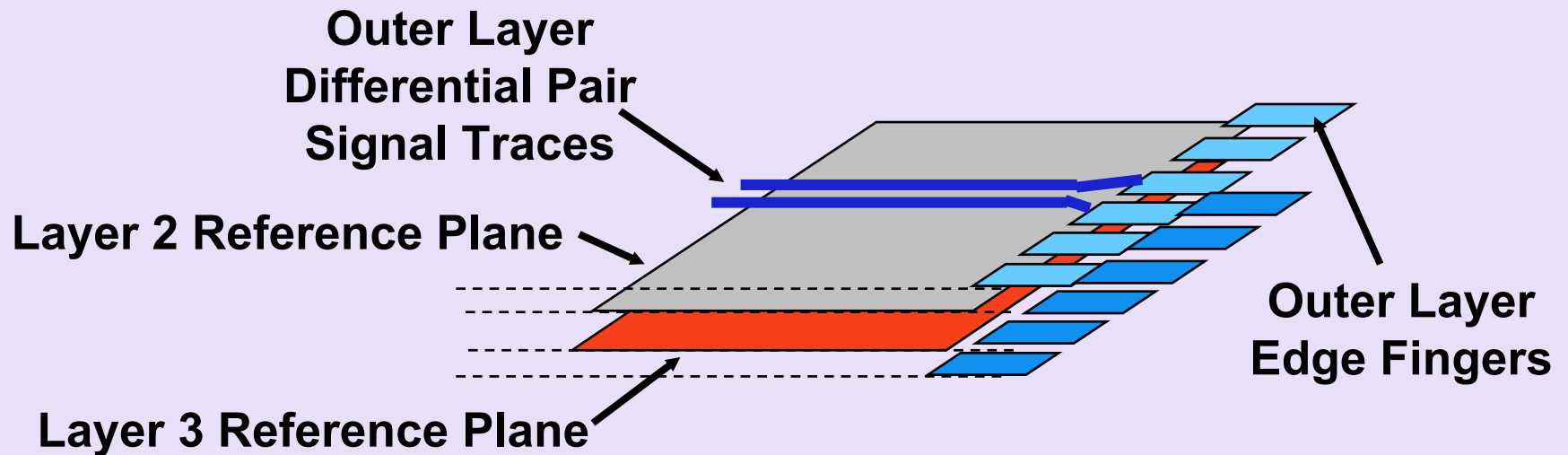
# Connectors

- New connector with standard PTH
- Pinout optimized for differential routing
- Loss & crosstalk part of baseboard budget
- Connector sizes: x1, x4, x8, x16



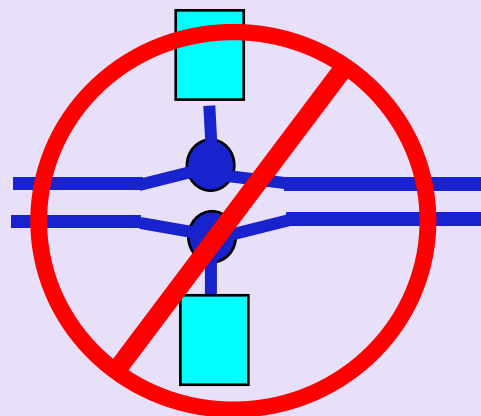
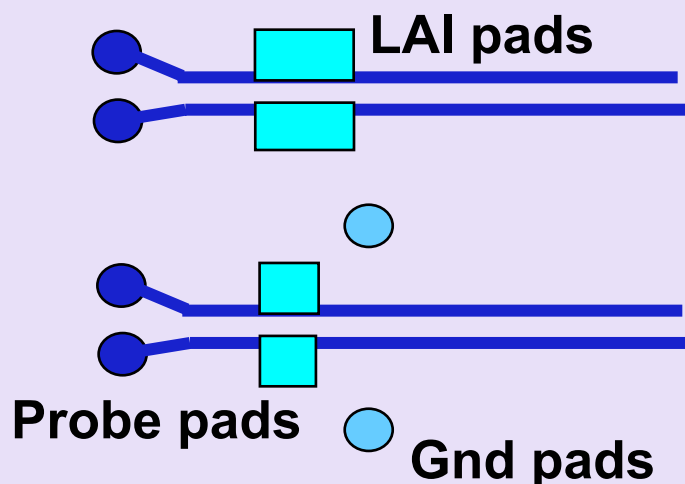
# Card Edge Fingers

- Remove ref plane under edge fingers pads
  - ✓ For better impedance/loss performance



# Test Points & Vias

- Minimize Vias usage
  - ✓ Up to 0.25 dB loss per via
  - ✓ Via pad size  $\leq 25$  mil, hole size  $\leq 14$  mil
- Put test points or LAI pads in series
  - ✓ No stubs
  - ✓ Provide Gnd pads for single-ended probing



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PCI-SIG Technology Seminar 2005.

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and

[www.mindshare.com](http://www.mindshare.com)



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