PCI Express™ Card ElectroMechanicals (CEM)

Chuck Stancil

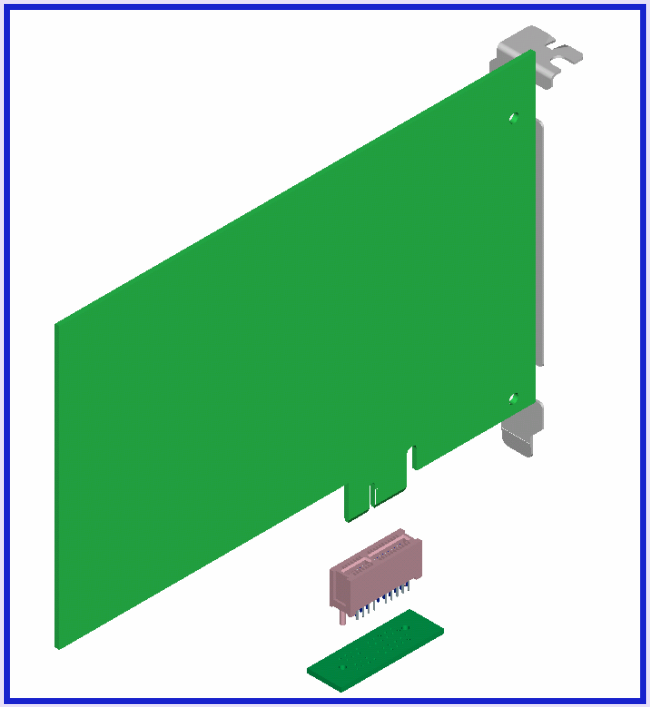
Hewlett-Packard Company
Chairman, PCI Express Electromechanical WG

Agenda

- Review of add-in card basics
- What's new for the CEM 1.1 spec?
- Summary
- Call to Action

Add-in Card Basics

Simple Add-in Card Design



Follows PCI Card form factors

Standard Height Cards, 4.20” (106.7mm)

Low Profile Cards, 2.536” (64.4mm)

Half Length Cards, 6.6” (167.65mm)

Full Length Cards, 12.283” (312mm)

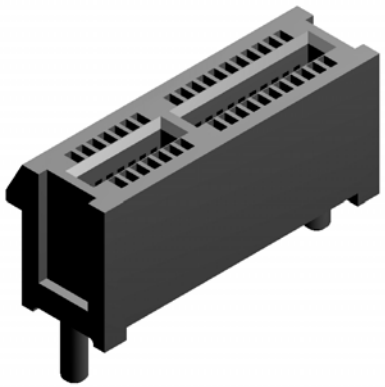
Uses PCI I/O Bracket

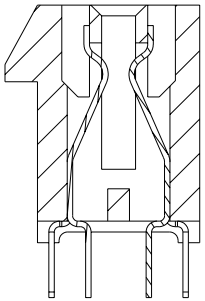
PCI Express Is Optimized for Cost

Add-in Card Size Exceptions

- Standard height x1 cards are limited to half-length (6.6”) for desktop applications
  - ✓ Push towards small form factor systems
  - ✓ 10W power limit
- For server I/O needs there is allowance for a 25W, standard height x1 card that MUST be greater or equal to 7.0” but less than or equal to full length

Low Cost Edge Card Connector





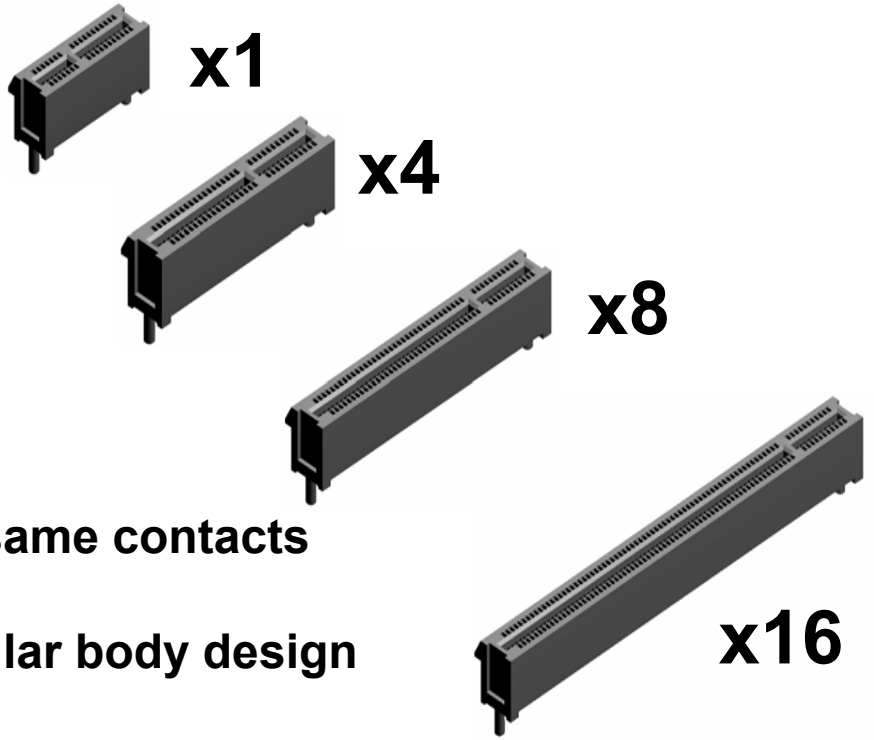
x1 connector 36 pins vs. PCI 120 pins

Simple Single Level Contacts

1mm Contact Spacing

Low Cost Connector Assembly

Scalable Connector Design



Use same contacts

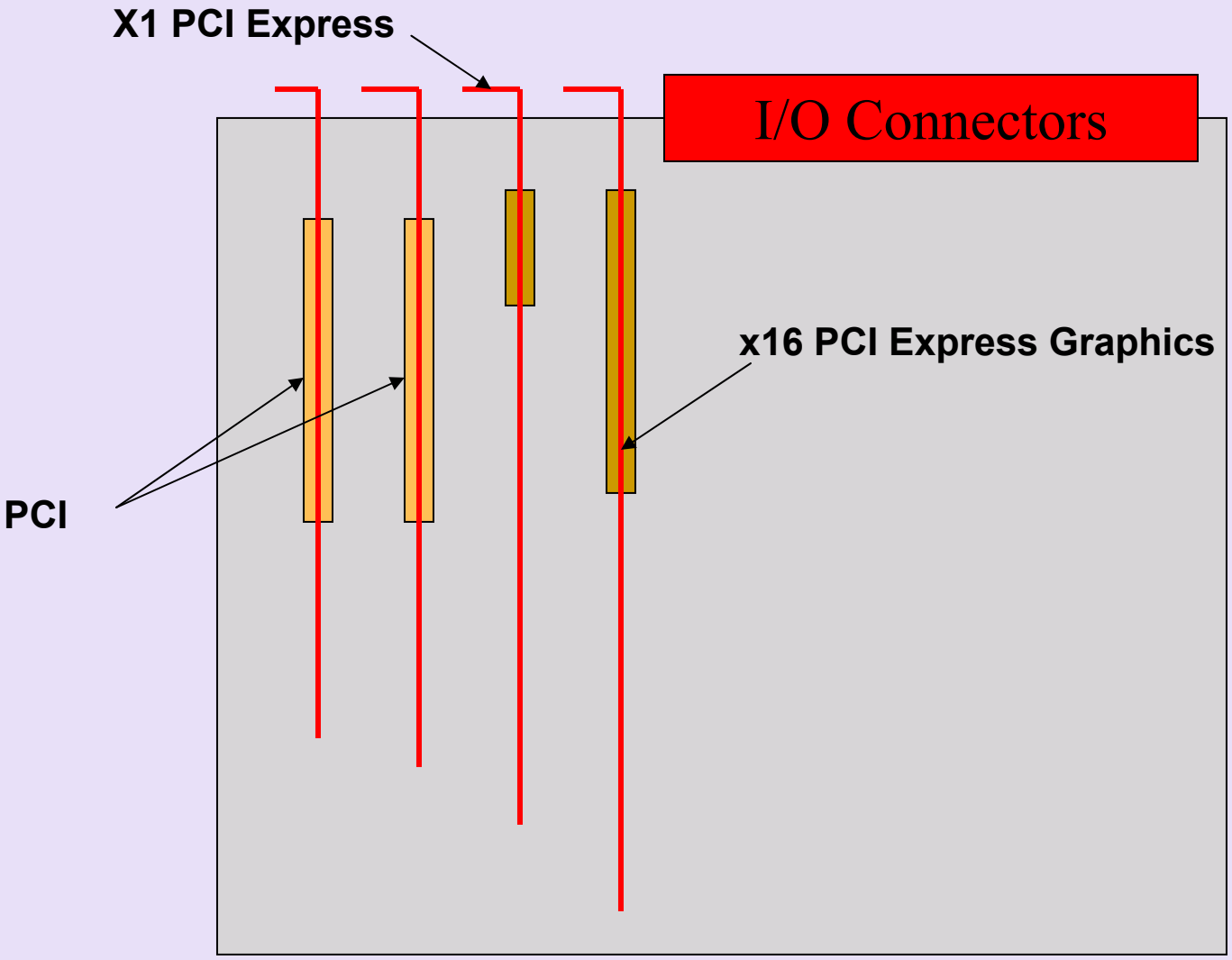
Modular body design

Use same connector manufacturing process

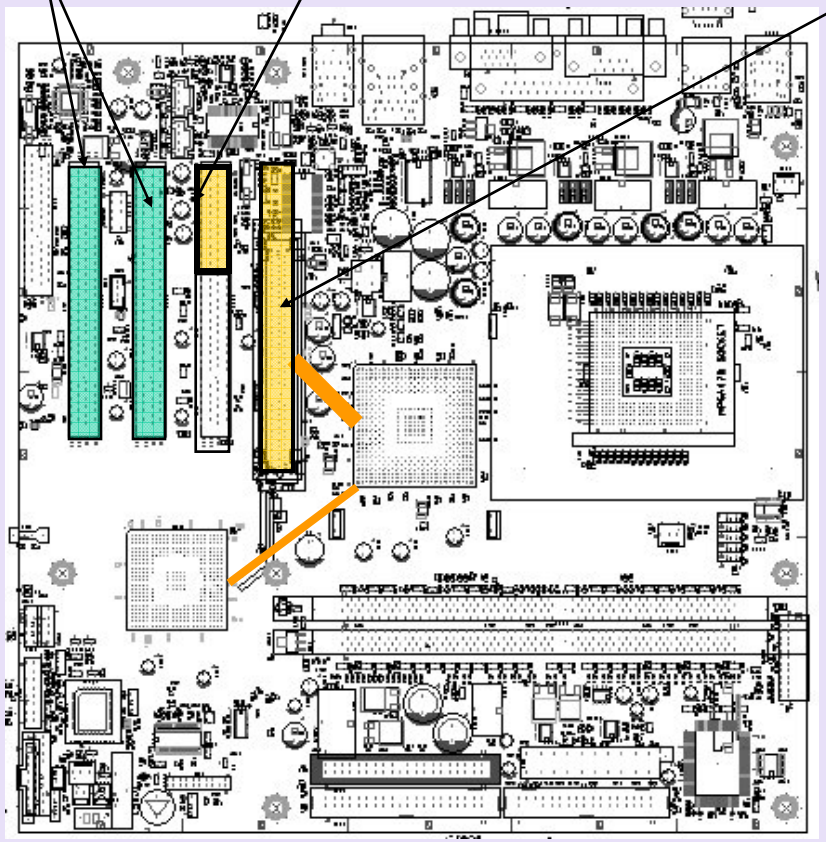
Scalable Design allows connectors from x1 to x16 to be easily designed

Smaller link-width cards can plug into larger link-width connectors

Slot Placement Strategy



Routing in 4-Layer Motherboards



µATX 4 Layer, P4 Motherboard

- PCI Express layout and connectors can be routed in 4 Layers
- Flexibility in routing PCI Express and PCI connectors on the same board
- Smaller connectors provide more room for routing and components

Power Delivery

Power Rail	*10W slot*	*25W slot*	*75W slot*
+3.3V ±9%	3A max	3A max	3A max
+12V ±8%	0.5A max	2.1A max	5.5A max
+3.3Vaux ±9%	375mA max	375mA max	375mA max

Notes:

- **3.3Vaux max current is 375mA when the add-in card is Wake enabled and 20mA when Wake disabled.**
- **An ECR to the CEM 1.0 spec changed the maximum slot power from 60W to 75W**

Compared to PCI and AGP:

- **Additional power from 12v rail**
- **+5V, -12V requirements are eliminated**

Power Rules

- System MUST provide +12V and +3.3V rails to ALL PCI Express slots in a chassis
- Systems may optionally provide +3.3Vaux but if supplied it MUST be provided to all PCI Express slots in a chassis
- If the platform supports the WAKE# signal then it MUST provide it and +3.3Vaux to all PCI Express slots in chassis
- Capacitive load rules:
  - ✓ +12V rail: 300µF @ 10W; 1000µF @ 25W; 2000µF @ 75W
  - ✓ +3.3V rail: 1000µF
  - ✓ +3.3Vaux rail: 150µF

Power Rules (Continued)

- Current slew rate: 0.1A/µs
- All x1 add-in cards must power up at a maximum of 10W; once configured as a High Power device, if applicable, a card can consume up to 25W
- All x16 add-in cards must power up at a maximum of 25W; once configured as a High Power device, if applicable, a graphics card can consume up to 75W

Power & Card Summary

- 10W: x1 cards (≤ 6.6” length)
- 25W: x1 cards (> 7.0” length), x4 cards, x8 cards, x16 low-profile graphics cards, x16 server I/O cards
- 75W: x16 full-height graphics cards

Add-in Card Interoperability

Slot / Card	x1	x4	x8	x16
x1	Required	Required	Required	Required
x4	No	Required	Allowed	Allowed
x8	No	No	Required	Allowed
x16	No	No	No	Required

- Up-plugging: Plugging a smaller link card into a larger link connector is fully allowed.
- Down-plugging: Plugging a larger link card into a smaller link connector is not allowed and is physically prevented.
- Down-shifting: Plugging a card into a connector that is not fully routed for all of the lanes. In general, this is not allowed. The exception is the x8 connector which the system designer may choose to route only the first four lanes. A x8 card functions as a x4 card in this scenario.

Reference Clock (REFCLK+, REFCLK-)

- Differential pair
- Nominal frequency of 100MHz (±300ppm)
- Point-to-point connection between each PCI Express connector and the clock source
- Within each differential pair the PCB trace lengths must be within 0.005”
- Spread Spectrum support is optional but likely needed to pass emissions testing!
- Termination resistors located at the clock source

Lane Reversal, Polarity Inversion

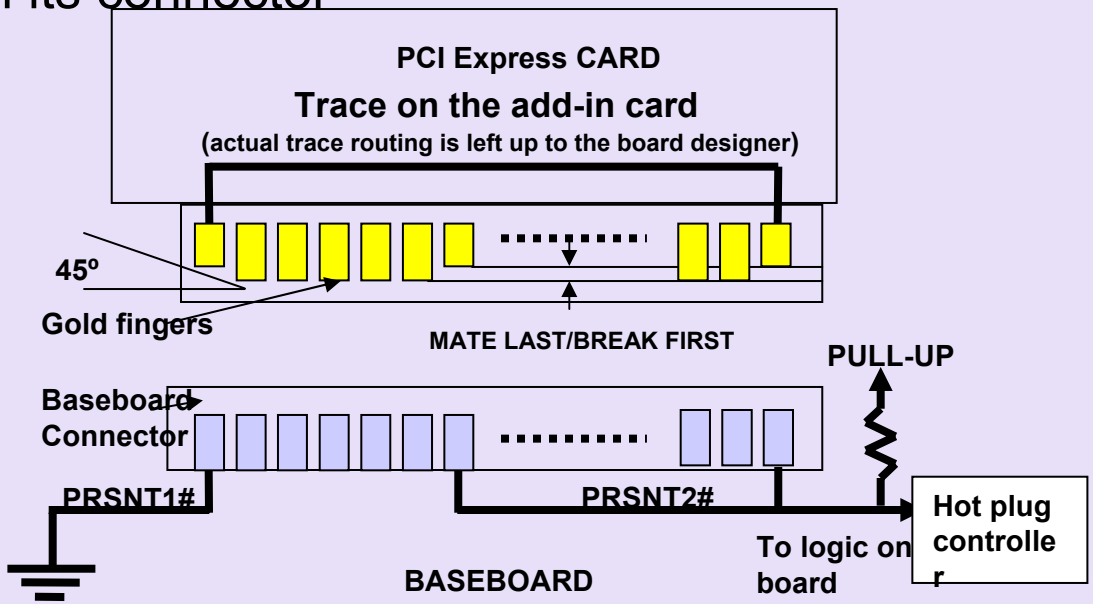
- The plus and minus connections from the system board's transmit differential pair (PETp/PETn) may be reversed
  - ✓ Simplification for board routing
  - ✓ Receiver is required to support Lane Polarity Inversion
- If a component does NOT support lane reversal then the board (system or add-in card) must adhere to strict connection ordering (i.e. Lane 0 to Lane 0, Lane 1 to Lane 1, etc) to the add-in card connector
- If a component DOES support lane reversal then the same lane ordering must be used for both the transmit and receive pair

What's new for the CEM 1.1 spec?

- Card Presence Detect
- REFCLK clarification
- Connector color
- Card retention
- Card edge chamfer tolerance
- PERST# clarification
- Default state for Active State Power Management Control

Card Presence Detect

- Supports the hot plug solution; ALL add-in cards must implement both gold fingers, PRSNT1# and the “furthest” PRSNT2#
- System use is optional for non-hot plug solutions
- There are multiple PRSNT2# pins on the connector – this is needed to support up-plugging
  - ✓ System buses them together
  - ✓ Add-in card connects PRSNT1# to the FURTHEST PRSNT2# pin on its connector



REFCLK clarification

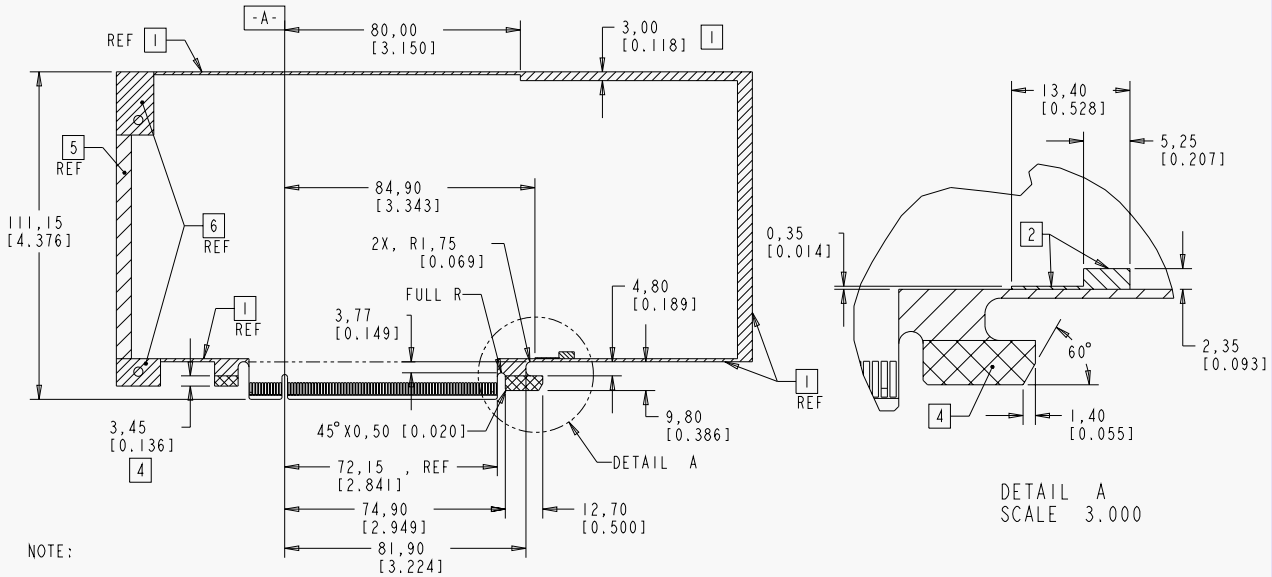
- The timing budget allows for approximately 4” of add-in card trace length
- Termination resistors on the add-in card ARE allowed but…
  - ✓ Not covered by the CEM spec!
  - ✓ The nominal voltage swing, and rise & fall times will be reduced in half!
- Consider shutting off the clock to empty slots!
- Additional details on REFCLK measurement configurations and data are being provided in the CEM 1.0a Errata document

Connector Color

- CEM 1.0 did not suggest or specify a color for the add-in card connector
- Approved ECN addresses this
- By default the recommended color should be black
  - ✓ This color hasn't been used for an add-in card connector since ISA was around)
  - ✓ Avoids any confusion with PCI connectors even though PCI and PCI Express cards are mechanically incompatible
- Other colors ARE allowed if a system OEM requires a particular color coding scheme

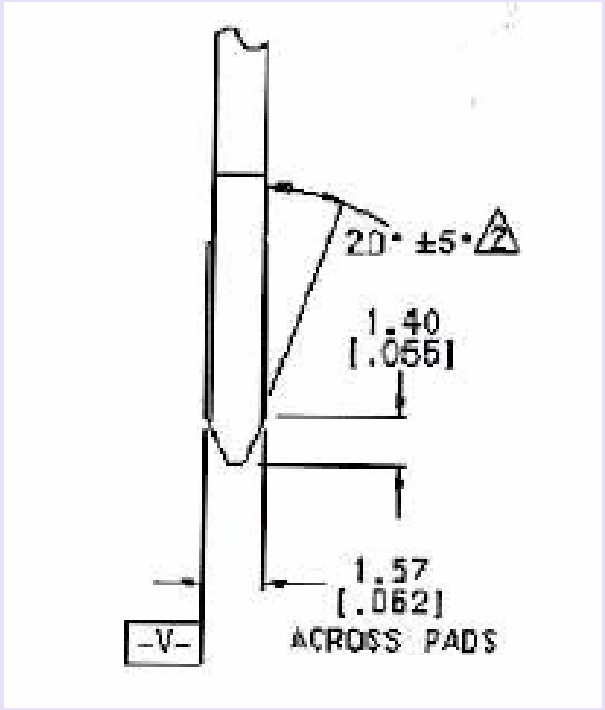
Card Retention

- ECN defines additional component keepout areas on add-in cards to support system-level card retention
- Focus is on full-height, x16 cards for Graphics



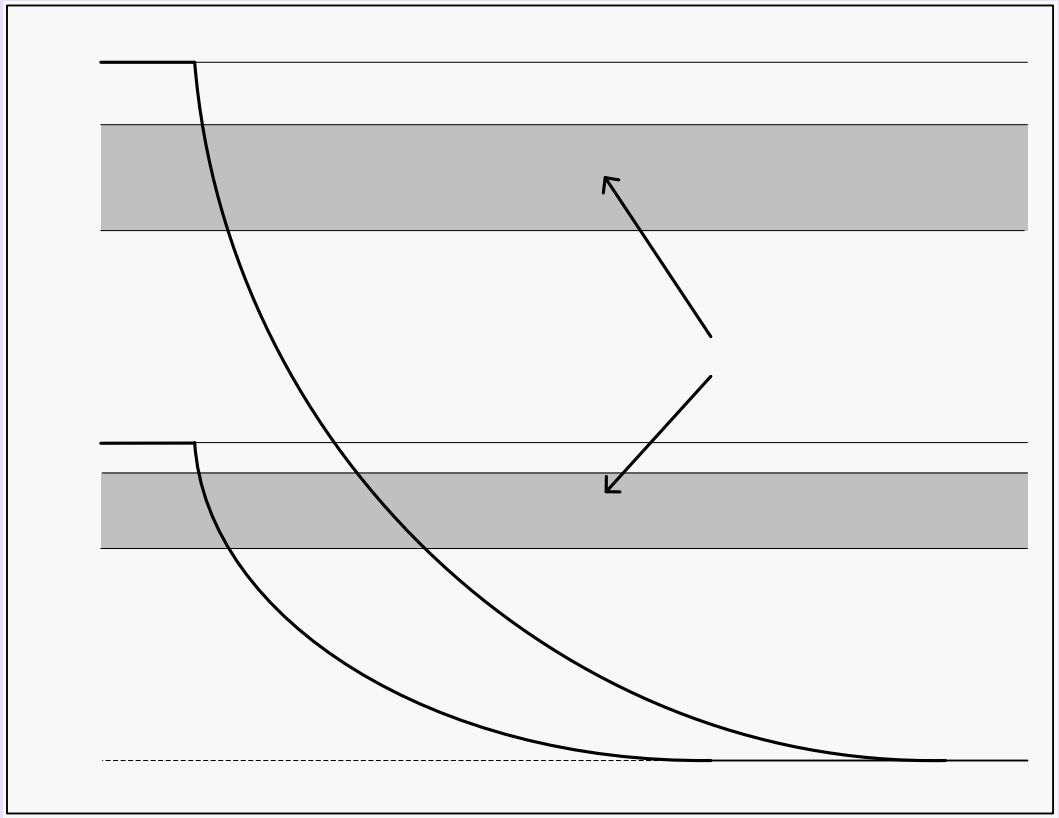
Card Edge Chamfer Tolerance

- The CEM 1.0a specification requires a tolerance of ±2° on the 20° card edge. It has been determined that this is too restrictive.
- The CEM 1.1 specification changes the tolerance to ±5°.



PERST# Clarification

- ECN defines threshold windows for PERST# activation
- Voltage monitoring circuitry will be able to reliably detect a power rail condition requiring the assertion of PERST#



Default State for ASPM Control

- The PCI Express Base Specification states that the default state for a PCI Express device's Active State Power Management (ASPM) Control is form factor-specific. The CEM 1.0a spec does not address this!
- The CEM 1.1 spec will now require the power-up, default state of the ASPM Control field (in the Link Control Register) to be set to 00b.
- The state of this field may be changed by the System BIOS or the Operating System only. Other software agents are not allowed to change this field.

Add-in Card Summary

- PCI Express is Optimized for Cost
  - ✓ Cost-effective for migration into commodity infrastructure
  - ✓ Replaces PCI over time with 15+ years of life
- PCI Express is Easy to Implement
  - ✓ Leverages existing form factors and standards
  - ✓ Transition with existing PCI form factors

Summary

- PCI Express functions will be available in a wide variety of form factors serving multiple market segments
- Each form factor addresses the specific physical, power, thermal and performance needs of the markets they are intended to serve
- Each form factor has a solid transition strategy for end-users/customers

Call to Action

- Prepare your product roadmaps to intercept the first launch of systems, cards, and modules

- Utilize the PCI-SIG (and other industry groups, as appropriate) for specifications and support

PCI Express™ Mini-Card ElectroMechanicals (CEM)

Ron Shaw

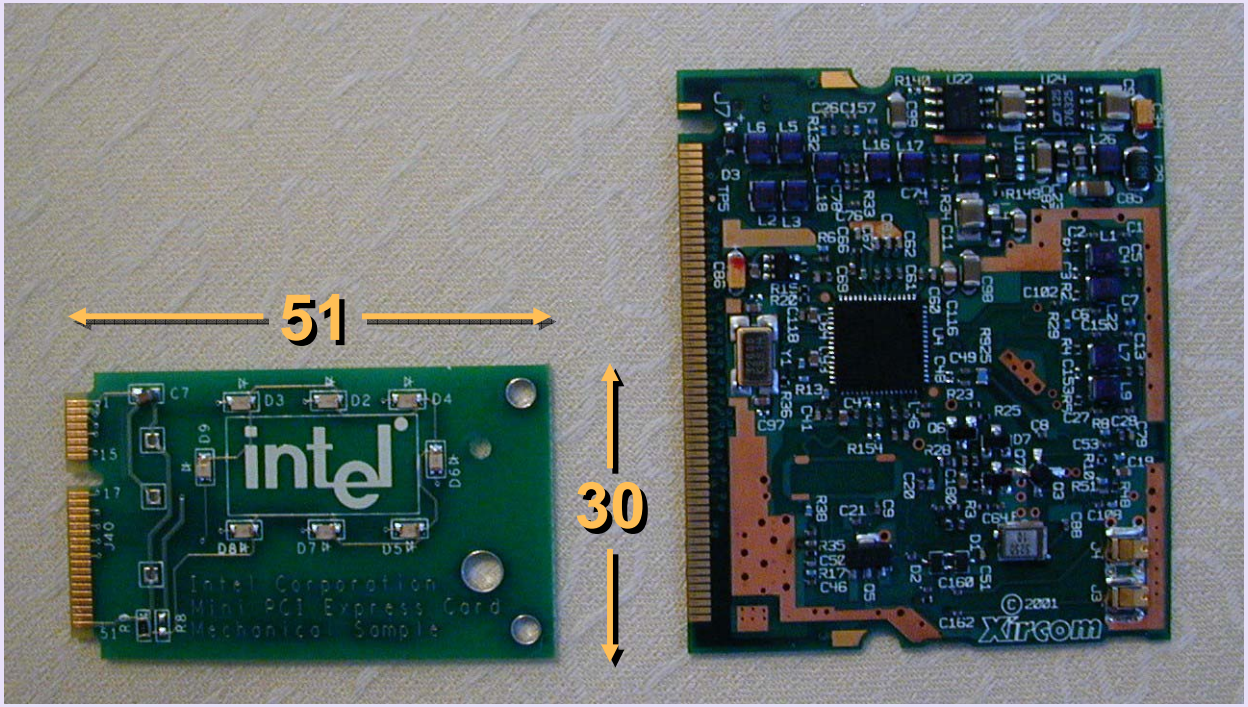
Chairman mini-CEM WG

Dell, Inc

What is PCI Express Mini Card

- Replacement for Mini PCI
  - ✓ Targeted for BTO/CTO solutions
- PCI Express and USB 2.0 enabled
  - ✓ Optimized for communication add-ins
- Card envelope: 30mm x 56mm x 5mm
  - ✓ Equal to ½ width of Mini PCI Type IIIa card

Half the Size of Mini PCI



PCI Express Mini Card

Mini PCI (Type IIIa)

Upgradeability / Serviceability

- Angled insertion and removal
- OEM optimized retention
  - ✓ Internal clips / screws / door attached clip
- BTO / CTO
  - ✓ Single connector
  - ✓ Multiple technologies
- Field replacement by service technicians
  - ✓ Reduce TCO / services costs

Targeted Applications

- Wireless-Personal Area Network (W-PAN)
  - ✓ Bluetooth / Ultra wideband
- Local Area Network (LAN)
  - ✓ 10/100/1G/10G Ethernet
- Wireless-LAN (W-LAN)
  - ✓ 802.11b/g/a, etc.
- Wide Area Network (WAN)
  - ✓ V.90/V.92 modem / xDSL / cable modem
- Wireless-WAN (W-WAN)
  - ✓ GSM/GPRS / UMTS / CDMA

Changes
Post Ver. 1.0

Changes from 1.0

- Editorial change
  - ✓ Power Sources
- CLKREQ# signal enhanced
  - ✓ Allows for additional power savings
- SIM / UIM pins defined
  - ✓ Allows for off card SIM / UIM
- Wireless Disable pin defined
  - ✓ Hardware disable of RF section of card
- Chamfer requirements changed
  - ✓ Manufacturability issues addressed

Editorial – Power Sources

- Section 3.2.1 Power Sources and Grounds
  - ✓ Corrected voltage sources text missed when +3.3VAux was added.

CLKREQ# signal enhanced

- Add functionality to CLKREQ# signal
  - ✓ Enhanced PCI Express clock management
  - ✓ Power saving benefit when PCI Express links are idle.
- Defined Power-up requirements
  - ✓ Defined CLKREQ# to REFCLK +/-
  - ✓ Defined CLKREQ# to PERST# timing
- Defined idle entry and exit timings
  - ✓ Defined CLKREQ# to REFCLK +/-
- Host not required to turn off REFCLK+/-

SIM / UIM pins defined

- Defines additional signals on the system connector to a removable Subscriber Identity Module (SIM) / User Identity Module (UIM).
- Pins identified as reserved for SIM in version 1.0 of mini-CEM specification now defined.
  - ✓ UIM_VPP (16) / UIM_RESET (14) / UIM_CLK (12)
  - ✓ UIM_DATA (10) / UIM_PWR (8)
- These are reserved for future SIM/UIM usage
  - ✓ UIM_C4 (19) / UIM_C8 (17)

W_DISABLE# pin defined

- Add pin to allow the host system to directly disable wireless (RF) operation to meet regulatory requirements.
- Active low signal.
- Defined timing relationship to disable RF and resume normal operations.

Chamfer relaxation

- Address manufacturability issues that have been identified with the chamfered edge. The change is to increase tolerance such that it is still effective, but more producible.
- Produce the chamfer to a +/- 5 mil tolerance as vendors have demonstrated capability (Cpk > 1.0) with a 10 mil range.

New Signals

PIN	Signal Group	Signal	Dir	Description
8	SIM / UIM	UIM_PWR	Output	Power source for the UIM
10		UIM_DATA	Output	UIM data signal
12		UIM_CLK	Output	UIM clock signal
14		UIM_RESET	Output	UIM reset signal
16		UIM_Vpp	Output	UIM variable supply voltage
17		Reserved (UIM_C8)	N/C	
19		Reserved (UIM_C4)	N/C	
20	Comms	W_DISABLE#	Input	Active low signal. This signal is used by the system to disable radio operation on add-in cards that implement radio frequency applications.

Mini Card Summary

- Higher performance and smaller F/F replacement for Mini PCI
- Optimized for communications applications
  - ✓ IHVs can select the serial interface appropriate for their device
  - ✓ Support for LED status indicators
- Outstanding power management features

Question & Answers

Thank you for attending the
2004 PCI-SIG Developers Conference.

For more information please go to
www.pcisig.com


PCI
SIG™