PCI Express™ Compliance Lab

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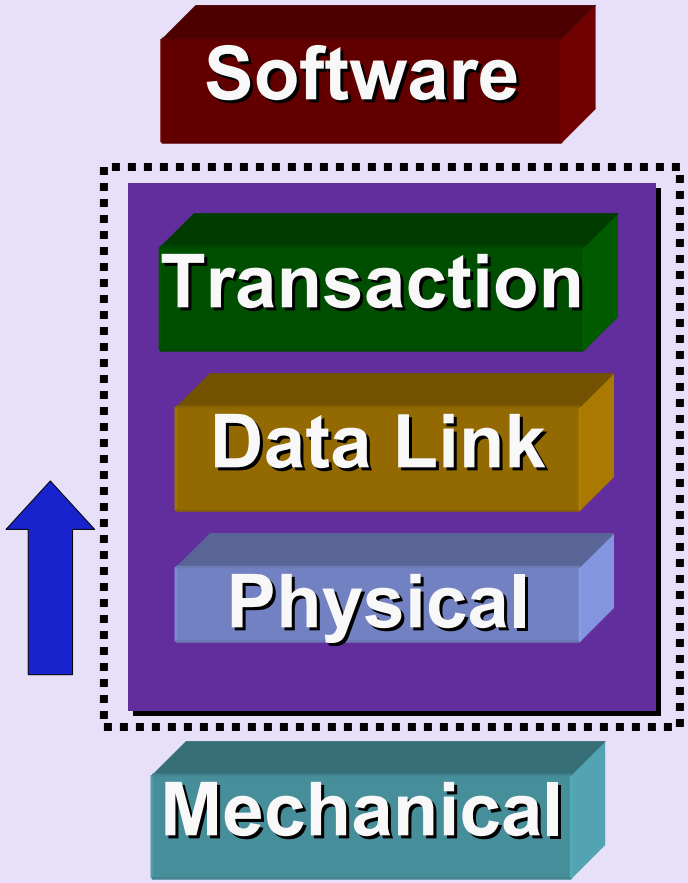
Agenda/Introduction

Compliance Test Areas

- Physical (Electrical)
- Configuration
- Link
- Transaction
- Platform BIOS
  - ✓ Demo

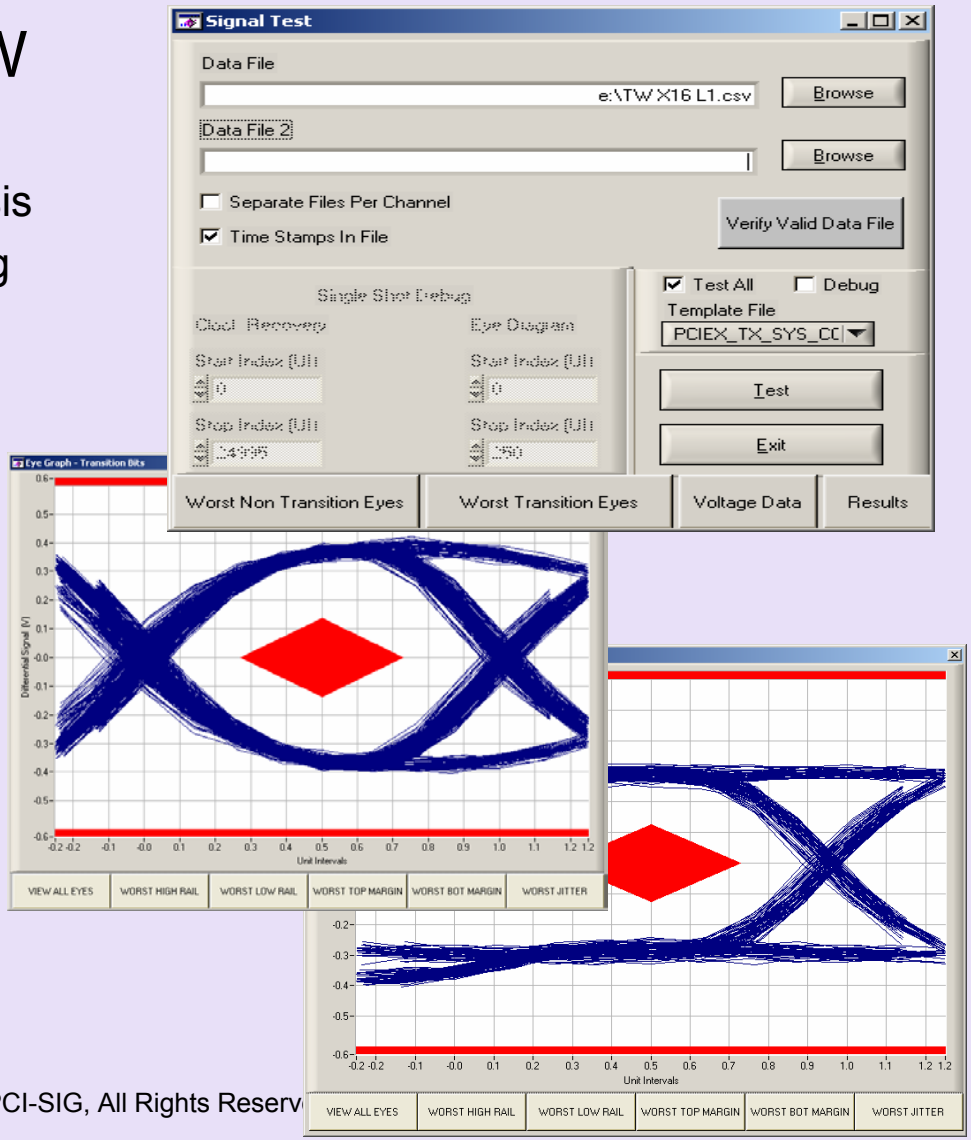


Electrical Tests

- Transmitter Signal Quality
  - ✓ Eye Diagram
    - Voltage margins
    - Jitter
  - ✓ Signal Rate
  - ✓ Common Mode Measurements
- Link State Timings
- Receiver Sensitivity
- Power Consumption
- Power Distribution

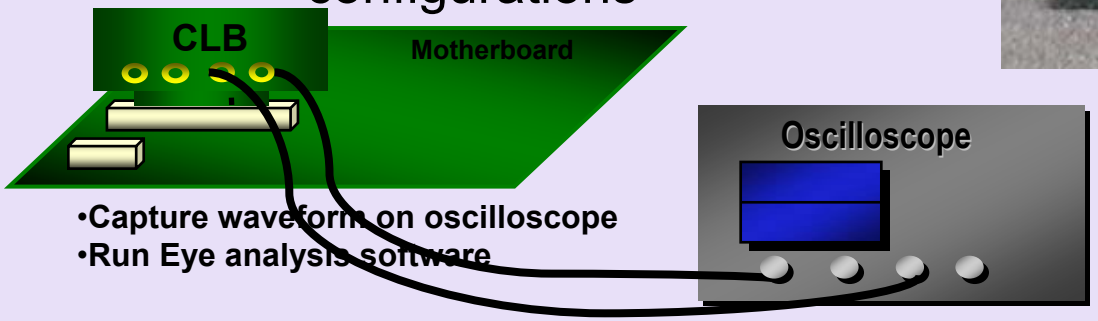
Electrical Tests and Tools

- Signal Quality Analysis H/W and S/W
  - ✓ Eye pattern, jitter and bit rate analysis
  - ✓ Upstream and downstream signaling
  - ✓ Electrical compliance base board
  - ✓ Electrical compliance load board
  - ✓ Stand-alone Windows-based eye diagram analysis S/W
  - ✓ Electrical test procedures and Oscilloscope setup files
- Jitter Analysis DLL
  - ✓ Clock Recovery
  - ✓ Interpolation
  - ✓ Transition/non-transition eye points
  - ✓ Goal - Promote consistent solutions



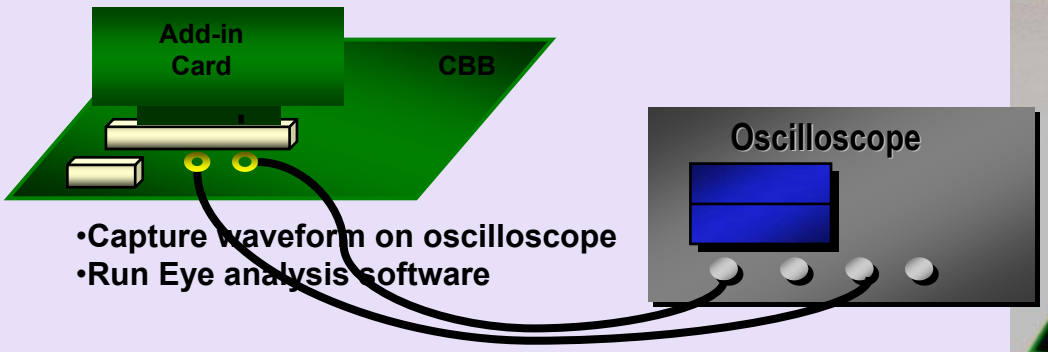
Motherboard Electrical Tools

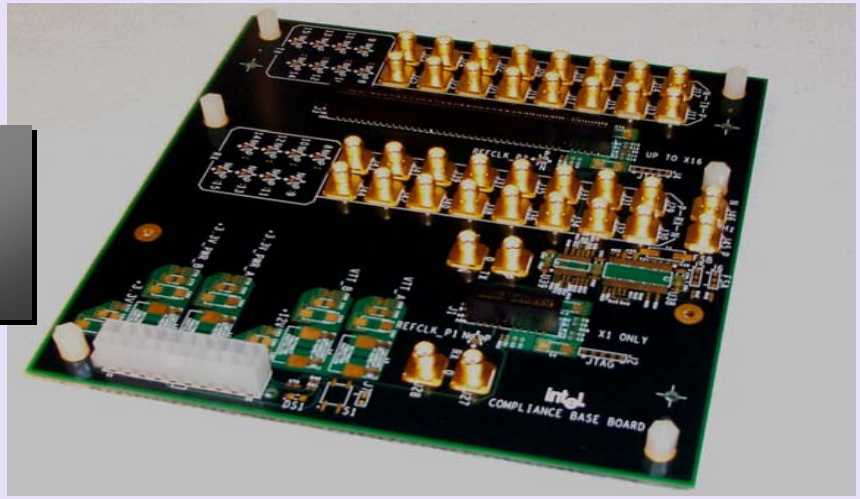
- Compliance Load Board
  - ✓ Root Complex electrical signal quality
  - ✓ Systems & Motherboards
  - ✓ Terminates Transmitter to utilize CMM mode
  - ✓ X1, X4, X8, X16 test configurations



Add-in Card Electrical Tools

- Compliance Base Board
  - ✓ X1, X16 connectors
    - – X16 provides termination X16 through X1
  - ✓ Power adaptor + current measurement
  - ✓ RX for X1 up to X8
  - ✓ Reference clock or external input

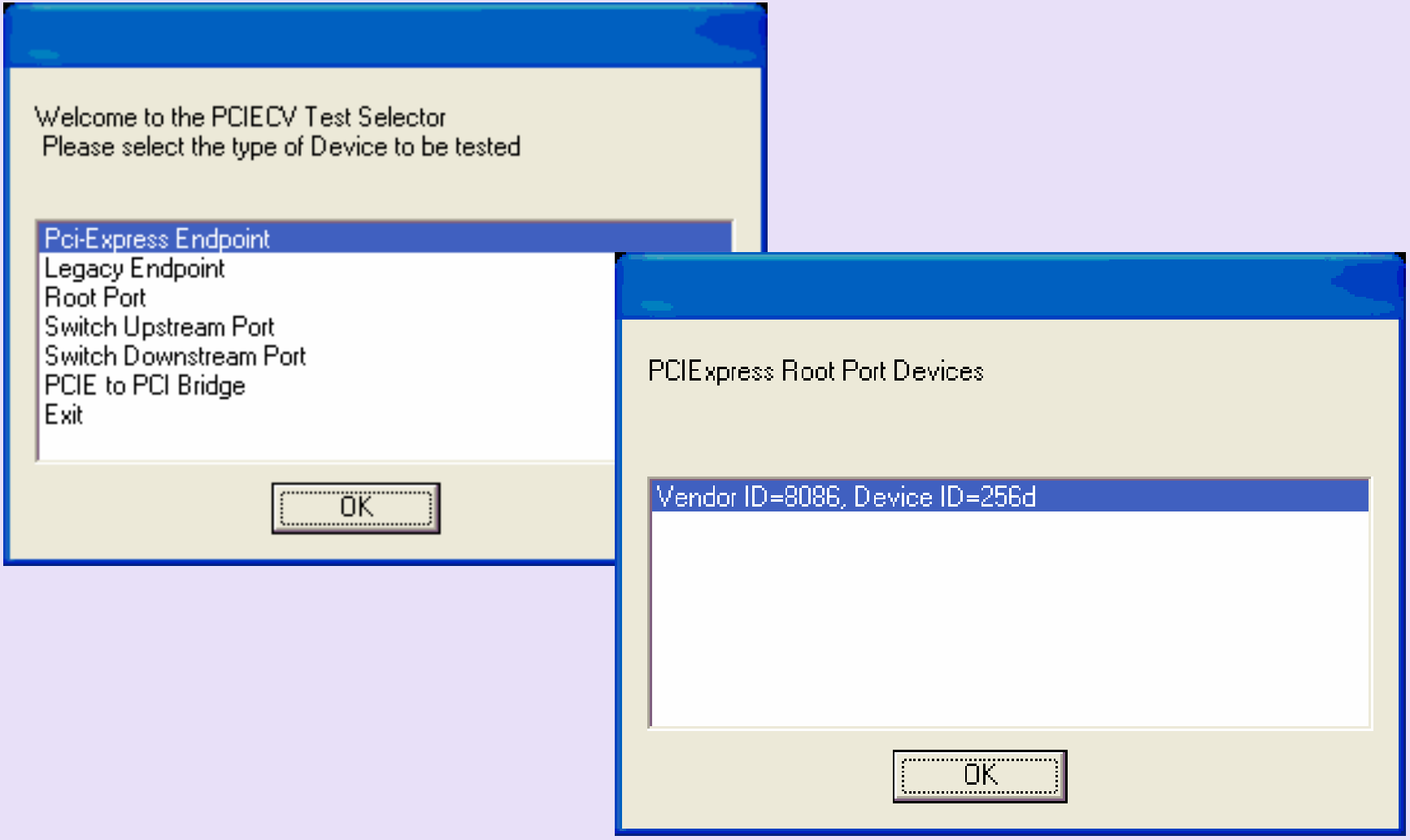




Config Tests

- Registers and Capabilities
  - ✓ Default Values
  - ✓ Characteristics
  - ✓ Required registers and capabilities
- Functional
  - ✓ Configuration Stress
    - Earliest Allowed Requests
    - Different Upstream/Downstream ASPM Combinations
    - Power Indicator/Control Messages
- System
  - ✓ Accurate Slot Reporting
  - ✓ Basic Hot Plug Event Reporting

PCIECV – Device Type Selection

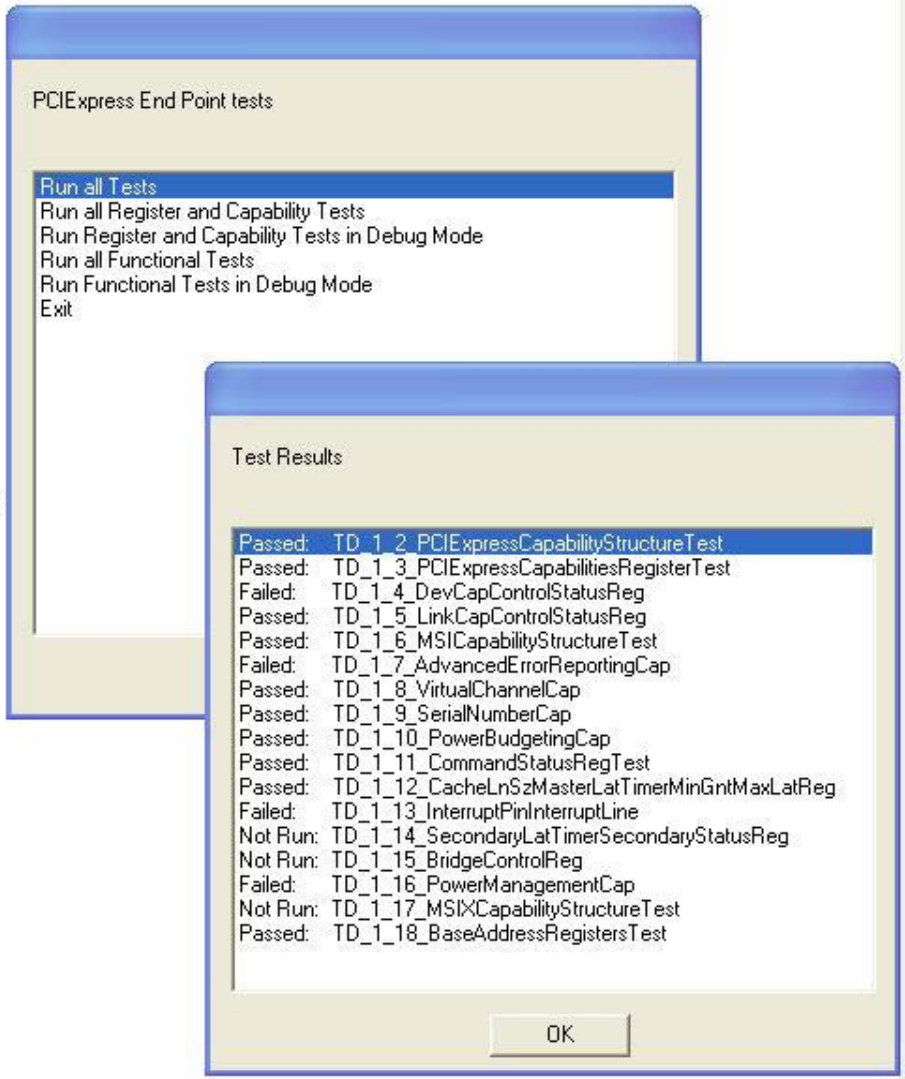


PCIECV_TestLog-040129-17h13m.txt - Notepad

File Edit Format View Help

```
INFO    Test End Point was Selected..
INFO    Device selected: Vendor ID= 11c2,  Device ID= beef
                    Bus number= 0001,  Device Number= 0000,  Function= 0000
INFO    Beginning Register and Capability Tests
INFO    TD_1_2_PCIExpressCapabilityStructureTest Selected.
INFO
    Starting Test: TD_1_2 PCIExpress Capability Structure Test
******************************
INFO    PCI Capability ID value:  0x10
INFO    Capability Offset value:  0x60
INFO    Next Capability Pointer value:  0x84
INFO    Device Capability Register value:  0xfa5
INFO    Device Control value:  0x2810
INFO    Device Status value:  0x0
INFO    Link Capabilities value:  0x3f411
INFO    Link Control value:  0x0
INFO    Link Status value:  0x11
INFO    Slot Implemented bit is not set.
INFO
    Stopping Test: TD_1_2 PCIExpress Capability Structure Test
    Number of: Fails (0); Aborts (0); Warnings (0)

INFO    TD_1_3_PCIExpressCapabilitiesRegisterTest Selected.
INFO
    Starting Test: TD_1_3 PCI Express Capabilities Register Test
******************************
INFO    PCI Express Port/Device Type value:  0x0
INFO    PCI Config Space Header Type: 0x0
INFO    PCIE Slot Implemented Value : 0x0
INFO
    Testing Register: PCIExpress Capability List Register
INFO
    Beginning RO test: Capability ID
INFO    Initial value of the field is 0x10
INFO    Testing with inverse of original value.
INFO    Value read back from the field was: 0x10
INFO    Testing field with all ones.
INFO    Value read back from the field was: 0x10
INFO
    Beginning RO test: Next Capability Pointer
INFO    Initial value of the field is 0x84
INFO    Testing with inverse of original value.
INFO    Value read back from the field was: 0x84
INFO    Testing field with all ones.
INFO    Value read back from the field was: 0x84
INFO
    Testing Register: PCI Express Capabilities Register
INFO
    Beginning RO test: Capability Version
INFO    Initial value of the field is 0x1
INFO    Testing with inverse of original value.
INFO    Value read back from the field was: 0x1
```



Protocol

- Protocol
  - ✓ Link Layer
  - ✓ Transaction Layer
- Checklists
  - ✓ Posted to the SIG site a year ago at least
- Test Specifications
  - ✓ Posted to the SIG C&I library section about 4 weeks ago
  - ✓ Check the most important ones -
    - Important for interoperability
    - Important for basic robustness – error tolerance
    - Important for software to depend on when enabled

Hardware & Software

- Protocol Test Card (PTC)
  - ✓ Agilent® Technologies is the vendor
  - ✓ Shipping for the last 3 months
  - ✓ Field upgradeable
  - ✓ Supports Add-in card testing and BIOS testing with different images
    - Selectable by dip switches
  - ✓ Platform mode still under development
- Software
  - ✓ Development Test Kit (DTK)
    - Contains test harness and tests
    - Ready for Linux® and Windows® environments
      - Windows version not as thoroughly tested as Linux version
  - ✓ Agilent Packaging
    - Same executables as in DTK, with a different GUI
    - Shipped with PTC

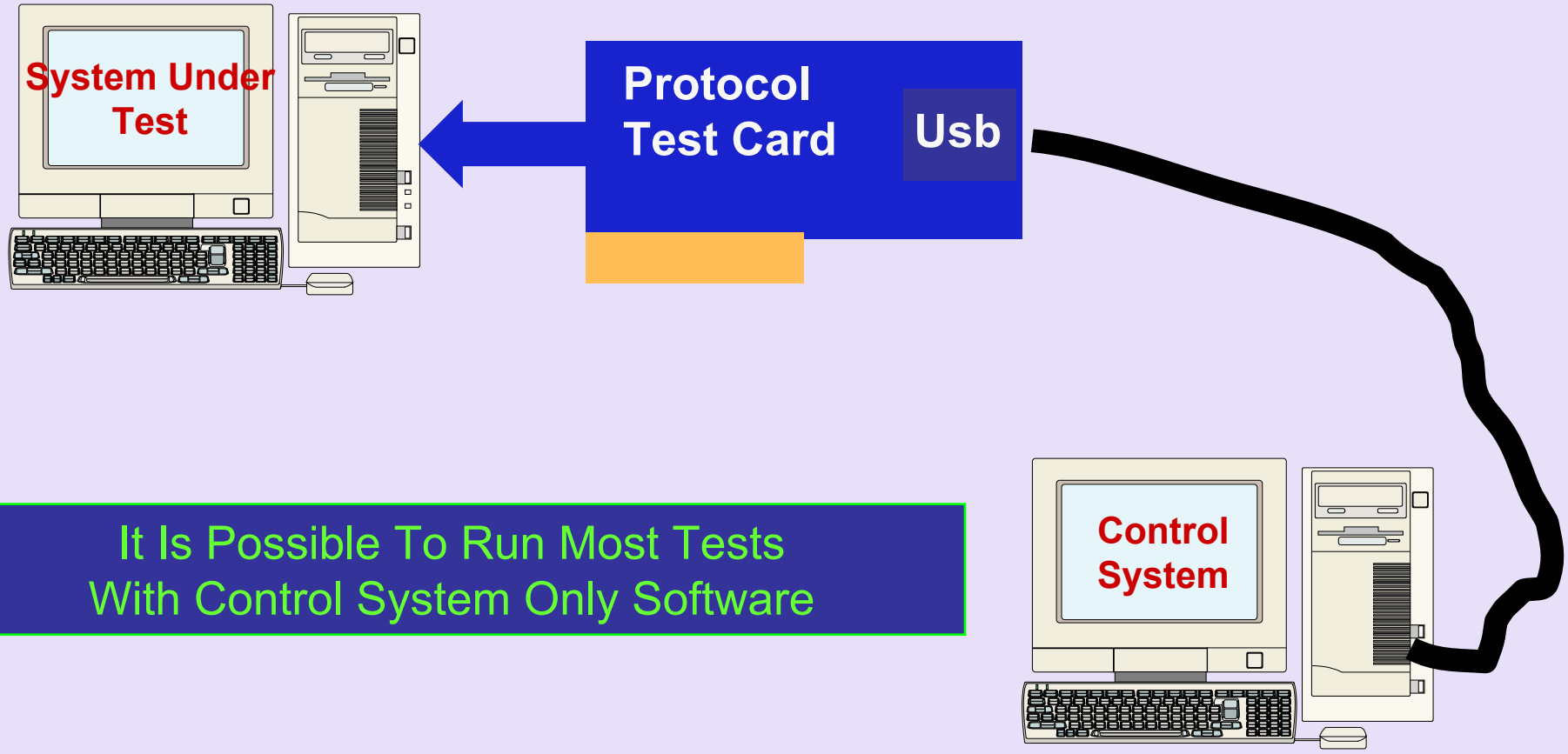
Link Layer

- 12 tests in total
- Check for
  - ✓ Response to Nak, No_Ack_Nak (Replay Timer expire)
  - ✓ Requirement of initiating soft link recovery
  - ✓ Response to CRC errors at DLLP and TLP layers
  - ✓ Response to Wrong Seq num at DLLP
- Base Error Reporting
  - ✓ Ensure correct error status bits are set in Device Status Register
  - ✓ Appropriate Error messages are sent
- AER bit setting if implemented

Transaction Layer

- 2 tests
- Check for
  - ✓ BDF info in completions coming back
  - ✓ Response to Unsupported Requests (UR)
  - ✓ Negotiated Link Width
    - Up/Equal Plugging, Down shifting
- Beta tests
  - ✓ Completion Timeout Mechanism
  - ✓ Legacy Interrupt Disabling

Platform BIOS Test Diagram



It Is Possible To Run Most Tests
With Control System Only Software

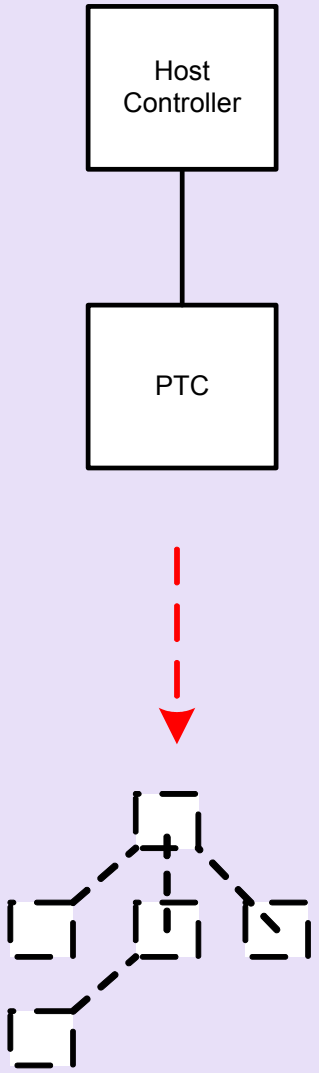
Platform Bios Tests

- Complex Topology Configuration
  - ✓ Complex Memory Assignments
  - ✓ Level of Bridge Support
  - ✓ PME
  - ✓ ASPM Support
- Interrupt Support
- Device Configuration Corner Cases
  - ✓ Non-responsive “bad” device
  - ✓ Worst case legal device response after reset
  - ✓ Config retry
  - ✓ Device doesn’t respond to shutdown requests

Platform BIOS: Topology Simulation

Single Device Can Represent Any Hierarchical Multi Device/Bridge Topology

Device Decodes All Type 0 and Type 1 Configuration Cycles.



Platform BIOS: Complex Topology Tests

- Configure Test Device For Topology Test On Reset
- Reset System Under Test
- Respond To Config Cycles From Control PC
  - ✓ Several Different Topologies – At least 3 Switches Deep
  - ✓ Record All Config Traffic.
  - ✓ Check Memory Assignments For Simulated Topology
  - ✓ Simulate Large Expansion ROMs and Boot Devices.
  - ✓ Check for incorrect L0s/L1 Enabling
  - ✓ Suspend System Under Test. (S3 or other supported states)
  - ✓ Simulate PM_PME (USB command to test device)

Platform BIOS: Max Device Response Time

- Configure Test Device For Single EP Platform Test On Reset
- Reset System Under Test
- Wait ~ 999 milliseconds for first Device Response.
- Ensure Device is configured correctly.
- Repeat with first response as retry

Monitor First Config Cycle Time

Platform BIOS: “Bad Device” Time-out

- Configure Test Device For Topology Simulation On Reset
- Reset System Under Test
- One Device In Topology is “bad” and does not respond.
- Ensure subsequent device is configured correctly.

Summary

- C&I testing is not a substitute for validation testing at the vendor site
  - ✓ Validation should incorporate C&I into its fold
- C&I testing should be done way ahead of coming to the SIG events
  - ✓ C&I tests are simple to run
  - ✓ Results and limitations could be worked out with SIG before coming to the event
  - ✓ Better predictability at the SIG event on getting onto the “integrators list”

RUN C&I Tests in your lab first

Thank you for attending the
PCI-SIG Developers Conference 2004.

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