
# Mastering Physical Layer Compliance Challenges at 5GT/s

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# Agenda

- ✓ Introduction
- ✓ PCIe® 2.0 changes from 1.0a/1.1 Spec
- ✓ 5GT/s Challenges
- ✓ Error Correction Techniques
- ✓ Test tool and fixture changes
- ✓ Agilent N5393A Compliance Application
- ✓ Additional Information Sources

# PCI-SIG® Compliance Testing

- ✓Physical Layer
  - Validate Signal Quality of TX
- ✓Configuration Space
  - Verify required fields and Values
- ✓Link Layer & Transaction Layer
  - Exercise protocol and boundary layer conditions
- ✓Platform Configuration
  - Validate BIOS correctly handling of PCI Express® Devices
- ✓Demonstrated Interop
  - Show that device drives load and device operates in actual PCI Express System

Focus of This Presentation

# PHY Testing Goals for PCIe 2.0

- Goals for PHY testing are unchanged
- Achieving those goals is more challenging
- Additional requirements added to increase confidence that designs are robust
- Verify designs achieve critical specification targets
  - ✓ Jitter
  - ✓ Eye mask
  - ✓ Reference Clock
  - ✓ Voltage and Jitter margining
  - ✓ Receiver Margining

Predictor of interoperability

# Changes Implemented under the PCIe 2.0 Specs

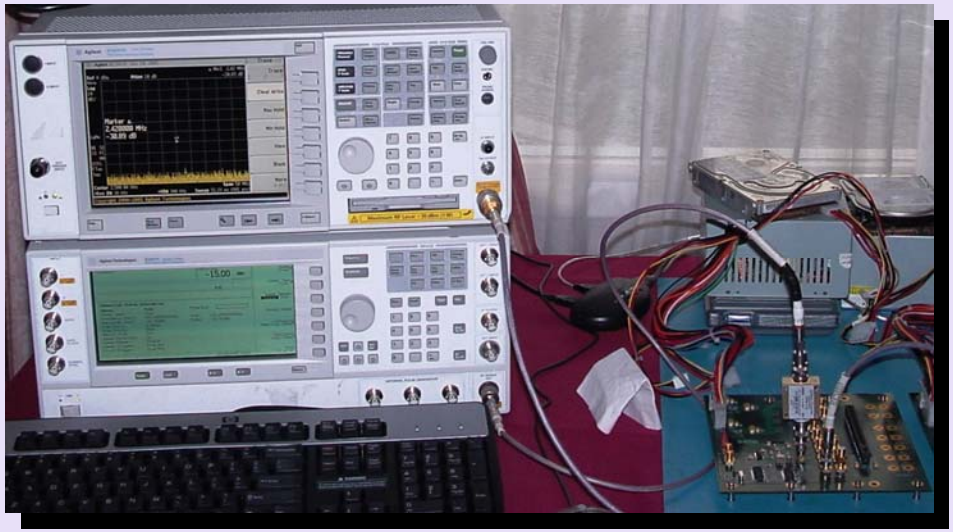
- Changes to the PCIe Base Specification
  - ✓ 5GT/s
  - ✓ Different de-emphasis levels
  - ✓ PLL bandwidth (BW)
  - ✓ Backward compatibility
- PCIe Card Electromechanical (CEM) Specification Changes
  - ✓ Rj / Dj tables and new jitter budgets
  - ✓ Changes to Reference clock phase jitter specification
  - ✓ 2 port measurement method for systems

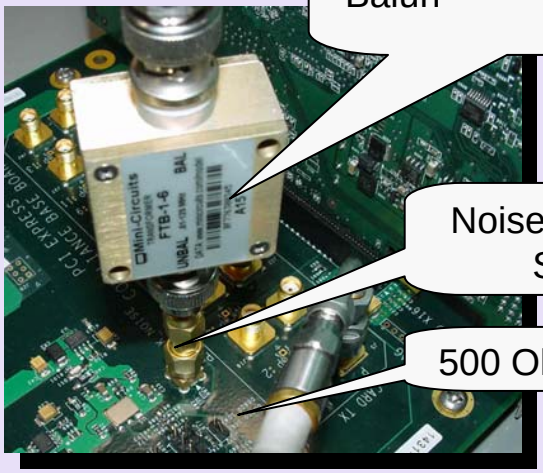
# Signal Level and BW

- 2.5GT/s de-emphasis = -3.5 +/- 0.5
- 5GT/s de-emphasis = -3.5 +/- 0.5 OR -6.0 +/- 0.5
- Low swing voltage levels = no de-emphasis

- BW dependant peaking requirements
  - ✓ 3dB for 8 to 16M
  - ✓ 1dB for 5 to 8M
  - ✓ 2.5GT/s same as 1.1

# PLL Loop Bandwidth Testing



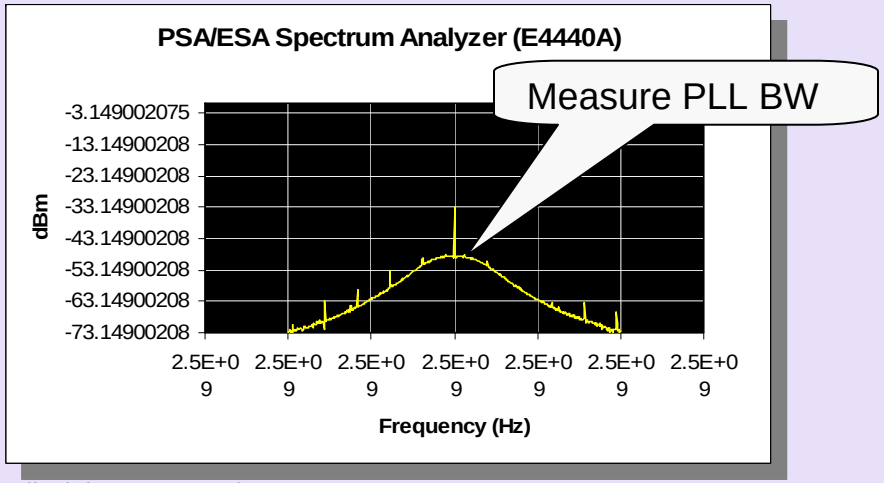



## Equipment Required:

- Sine Wave Source (1GHz min)
- Spectrum Analyzer (3 GHz min)
- Microcircuits FTB-1-6 Balun
- Modified CBB

## Steps:

- Sweep source 100-125Mhz (-20dBM)
- SA: 35KHz Res BW, 40MHz Span, 2.5 GHz center
- Set display to peak hold
- Normalize response to note 3dB point



# 5GT/s jitter challenges

- Jitter measurement more complex!
- Jitter decomposition required

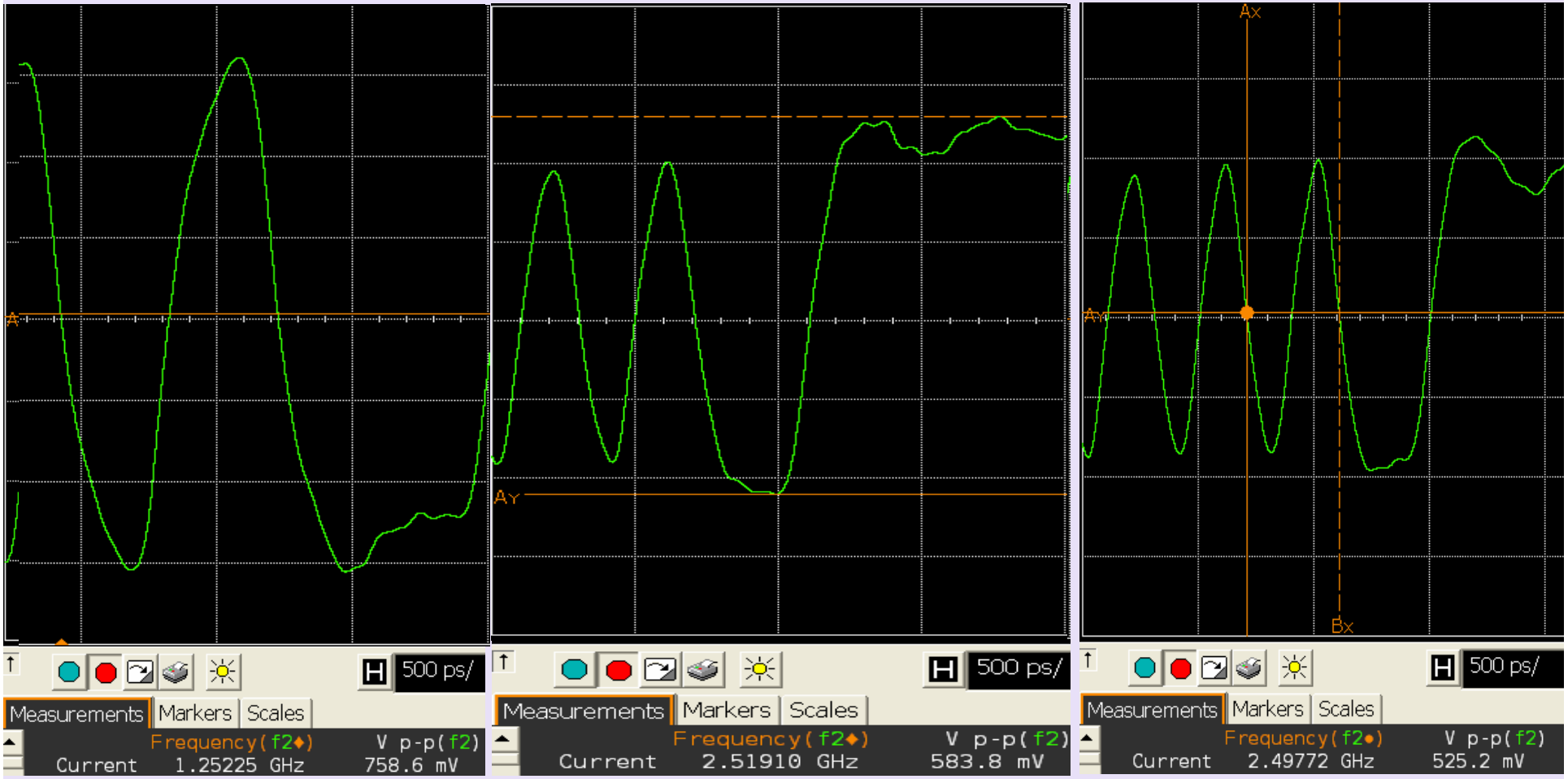
+/- 7.03
For 10-12 BER

$$System\ Tj \equiv \sum Dj + 2Q_{BER}\sqrt{\sum Rj^2} \leq 1.0\,UI$$

- Speed dependant phase jitter filters
  - ✓ 2.5GT/s = 1 pole HPF
  - ✓ 5GT/s = step band pass filter

- Error correction needed to measure TX at pins

# Why New De-emphasis Levels

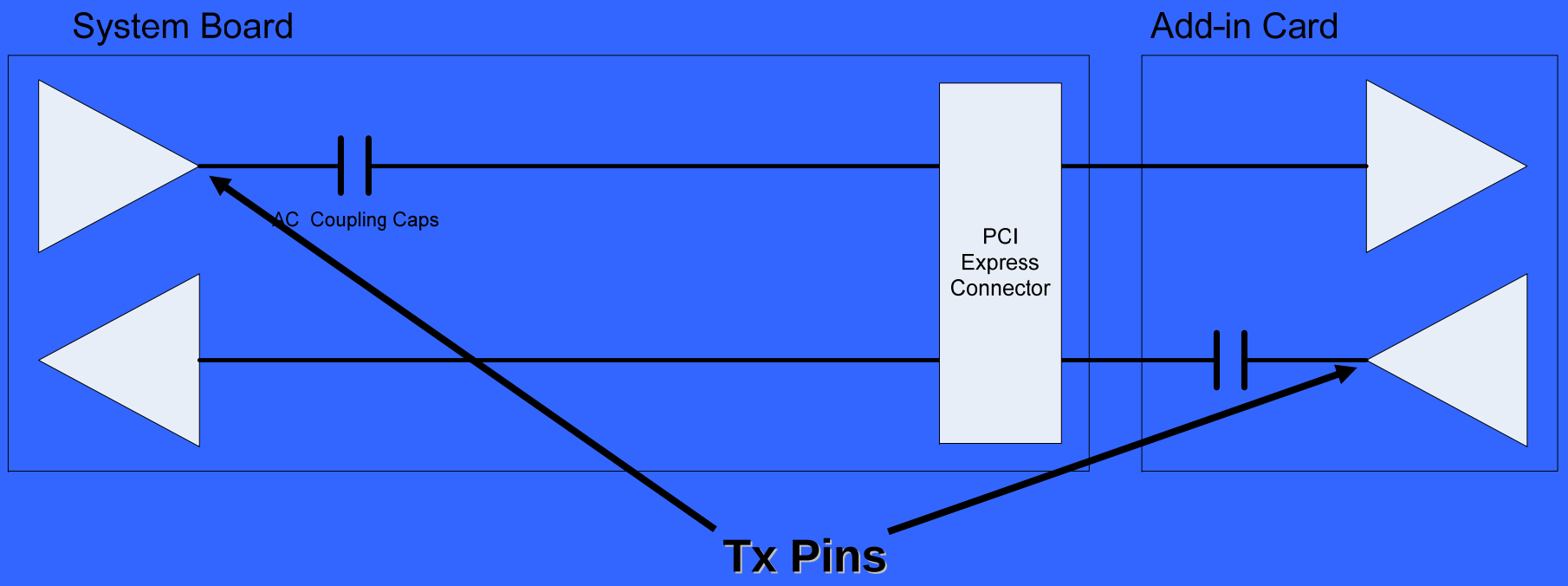



**2.5GT/s -3.5dB**
**Vp-p = 758mV**

**5GT/s -3.5dB**
**Vp-p = 583mV**

**5GT/s -6dB**
**Vp-p = 525mV**

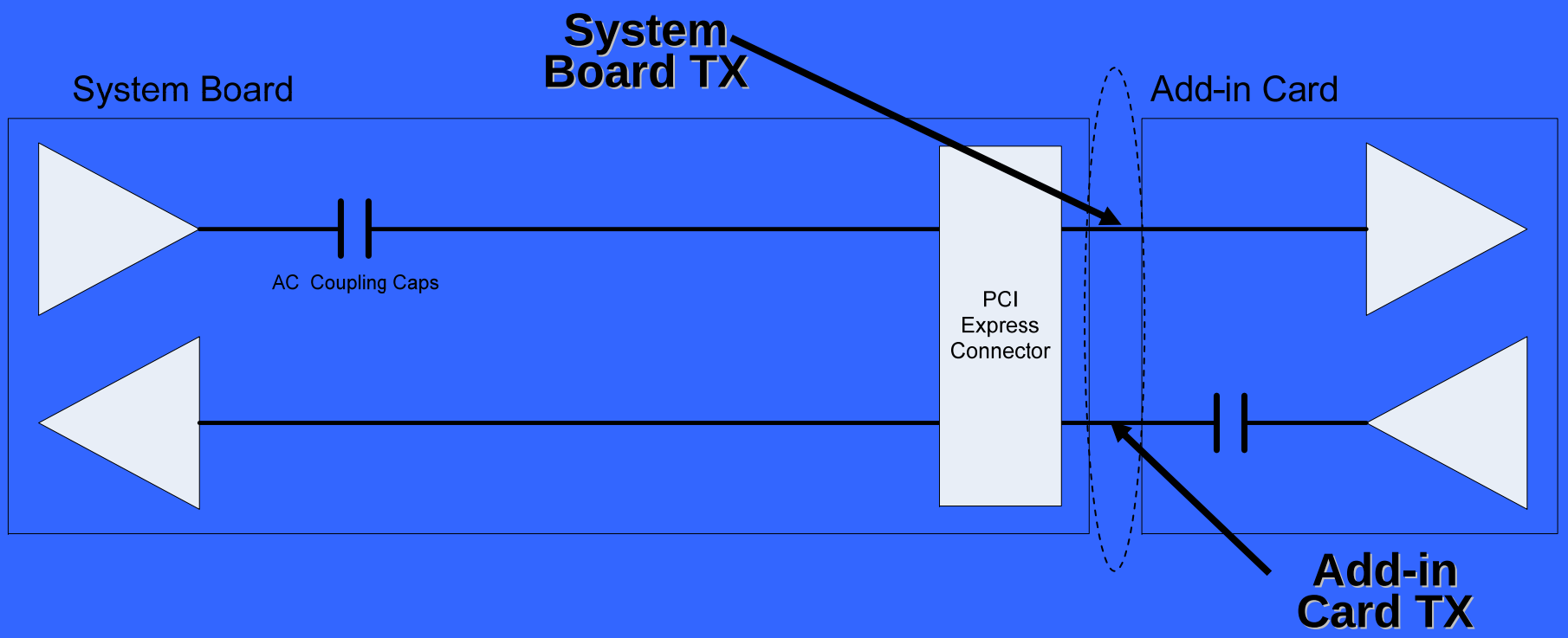
# Transmitter specs at TX Pins




## Same reference location as 1.1

Error correction needed to measure TX at pins

# CEM Spec targets connector




**Clarification of measurement location**
**Compared to 1.1**
**Chip + Interconnect**

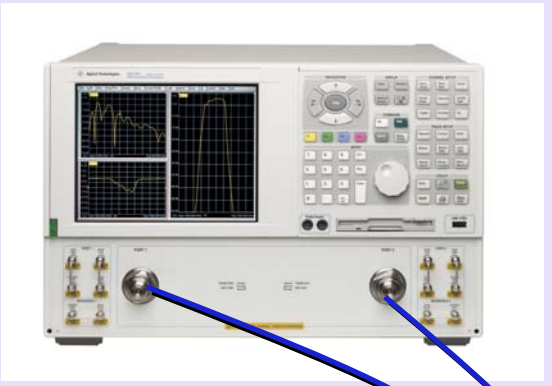
# Error Correction Techniques

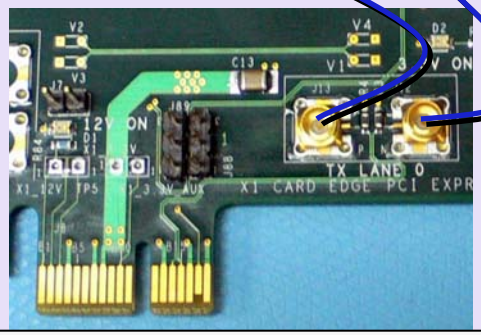
## DSO81304 HPS
Pre-measurement operations

Skew Calibration
Probe Attenuation/offset
Channel Vertical Cal
Channel Trigger Cal

**Calibrating the Scope**

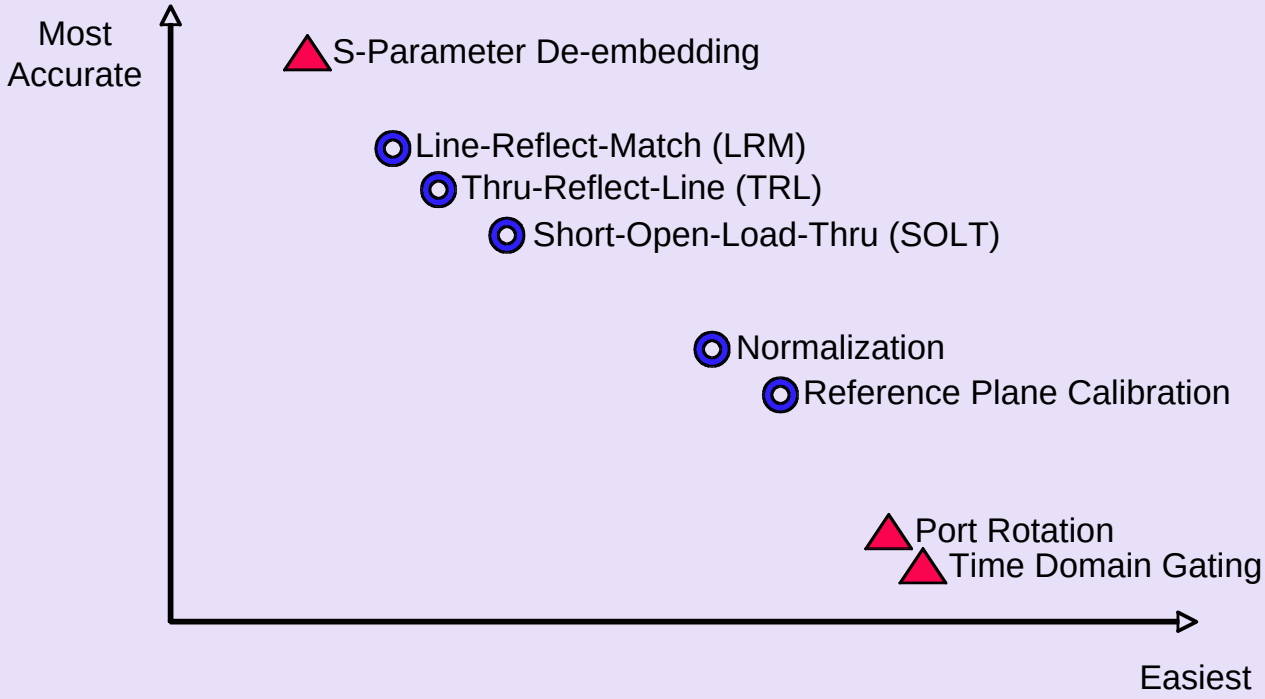
## N5230A PNA-L
Post-measurement operations






**De-embedding the CLB/CBB**

# Fixture Error Correction Techniques




= Pre-measurement error correction

= Post-measurement error correction

# De-embedding

- New Transmitter base specification requirement

"Measurements at 5.0 GT/s must de-embed the test fixture"

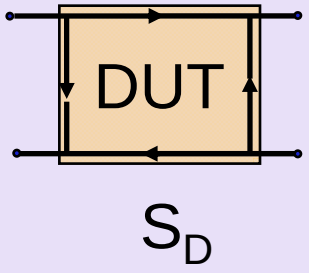
"It is also acceptable to use a common test fixture and de-embed it for measurements at both 2.5 and 5.0 GT/s."

- What does it mean to de-embed?

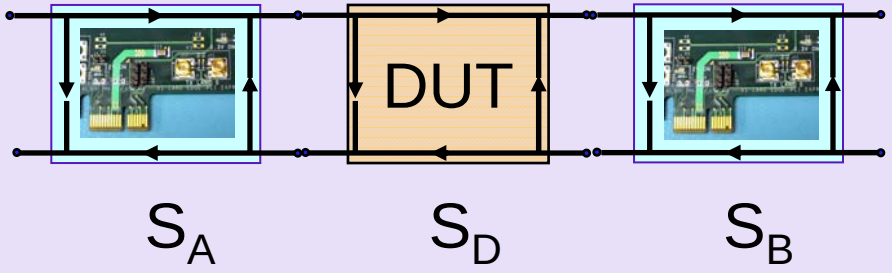
"Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins."

# What is De-Embedding

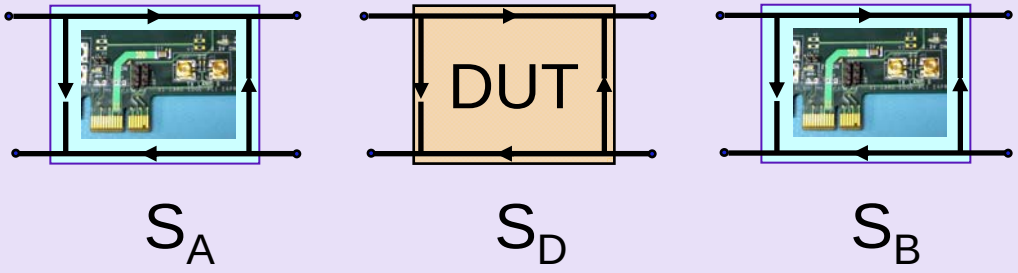
**What we want**: DUT performance




**What we measure**: composite measurement of DUT and fixtures

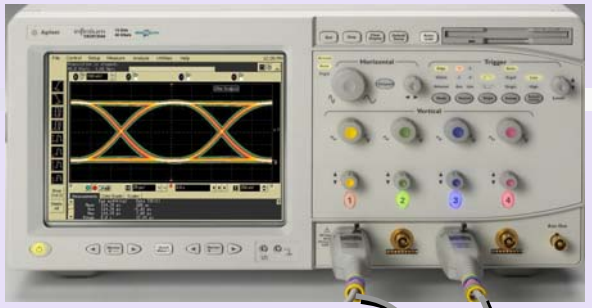



With the separate fixtures' S-Parameters, we can de-embed the DUT alone from the composite measurements

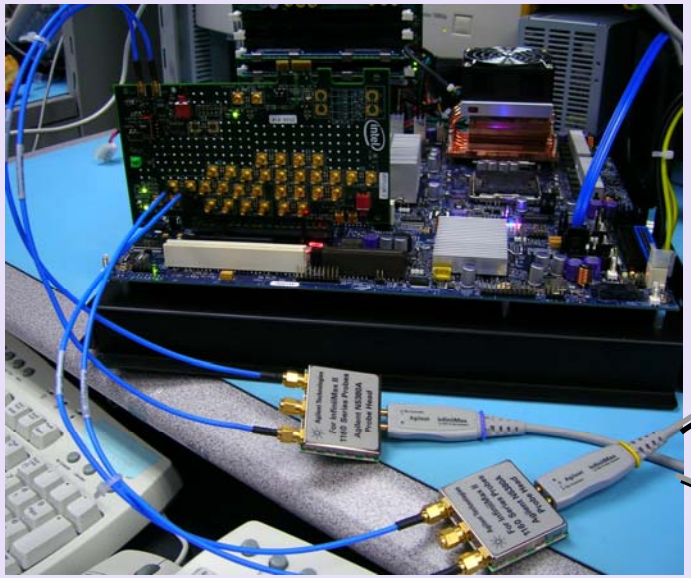



**Agilent is working on application notes for de-embed of fixtures**

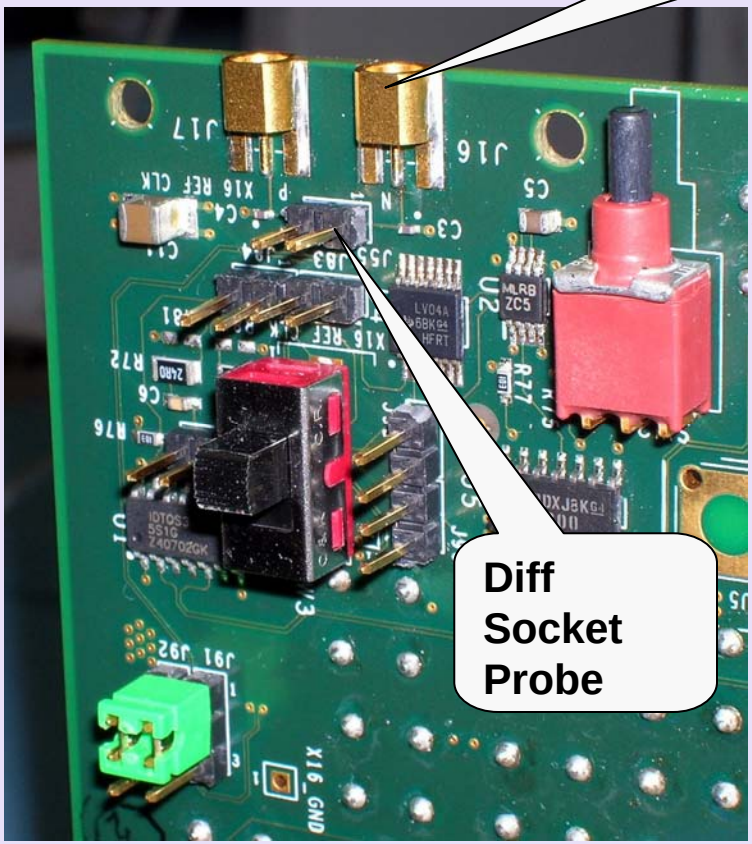
# SQ Test Tool Requirements – System Board

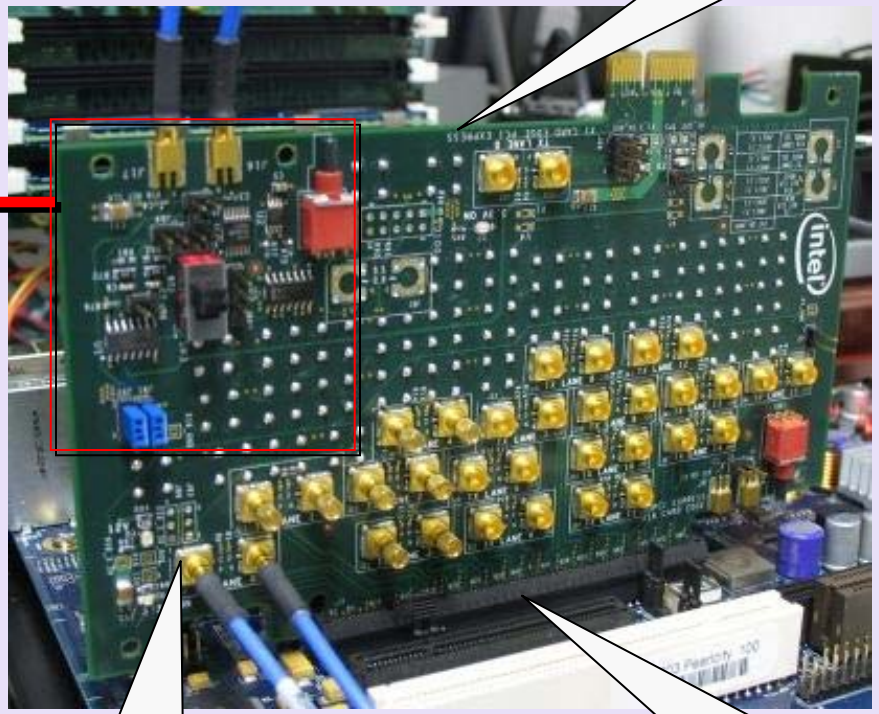


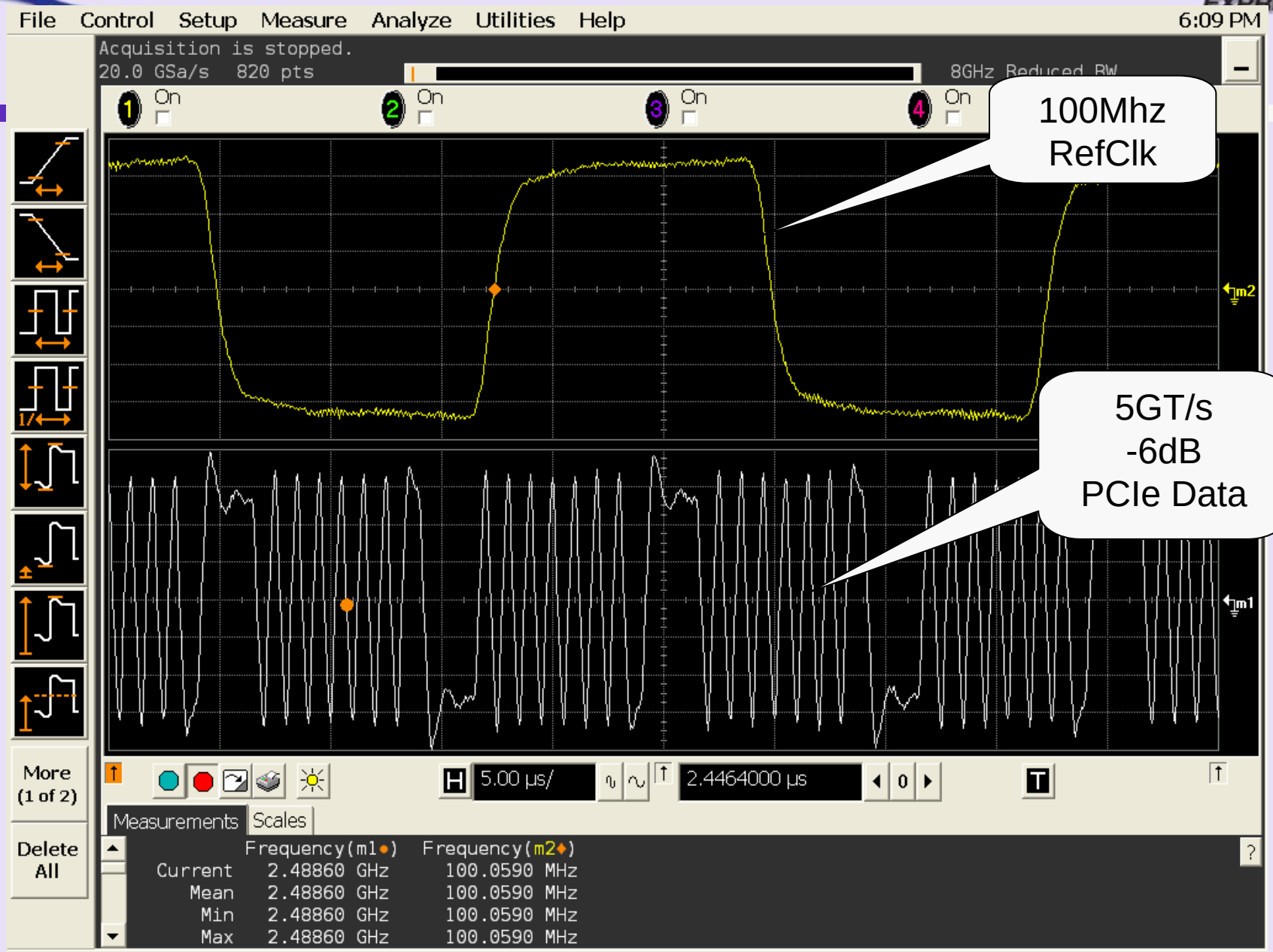
- Use of CLB 2.0
- SMP to SMA adapter, phase matched SMA cables
- Terminate all lanes except the lane under test
- Measure transmitted clock and data waveforms simultaneously with high speed oscilloscope
- Use compliance pattern
- 1M UI of data
- Sample rate of 40GS/s (25ps)
- Compute:
  - eye diagram,
  - Rj, Dj, Tj@10^-12 BER,
  - average data rate,
  - rise/fall time,
  - mode toggle
- Measure all lanes of all 5GT/s capable slots



# System 2 port measurement

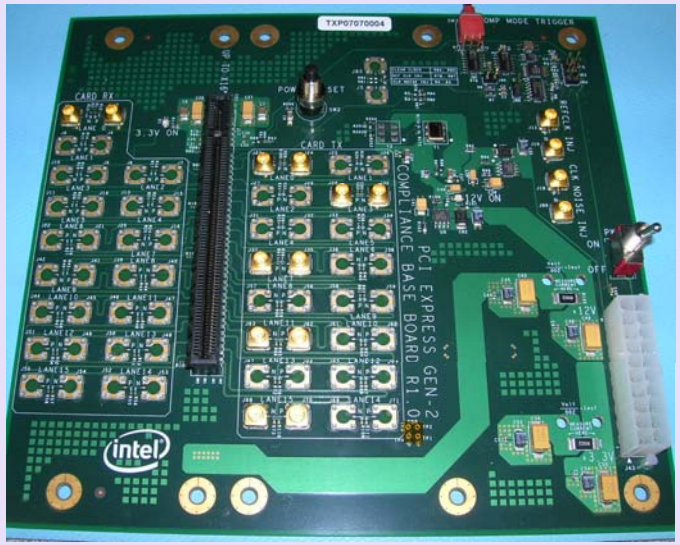




# Test Tool Requirements – Add In Card (AIC)

- Use of CBB 2.0
- SMP for all lanes, phase matched SMA cables
- Terminate all lanes except the lane under test
- Measure transmitted waveform with high speed oscilloscope
- Use compliance pattern
- 1M UI of data
- Sample rate of no more than 25 ps
  - ✓ 40GS/s or greater
- Compute:
  - eye diagram,
  - Rj, Dj, Tj@10^-12 BER,
  - average data rate,
  - rise/fall time,
  - mode toggle
- Measure all lanes



# Agilent N5393A PCI Express Compliance Application

Key Benefits:

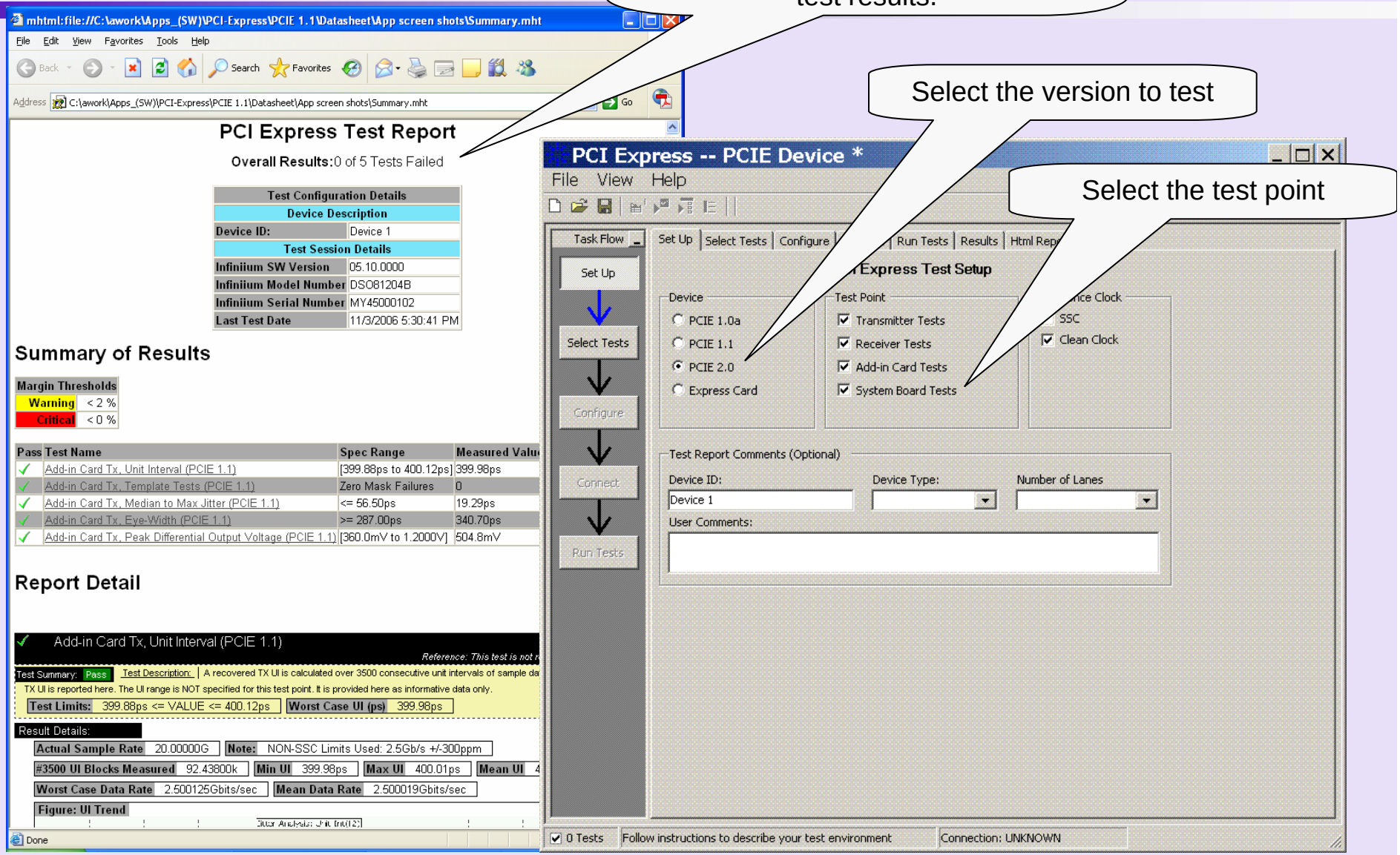
- 1M UI meets compliance requirements
- Batch run capability for greater testing coverage or quick spot checking
- Optimized scope setup for each measurement ensures the highest accuracy of each test performed
- Results trace back directly to the specification and SIGTEST algorithms

# Test Results with the N5393A

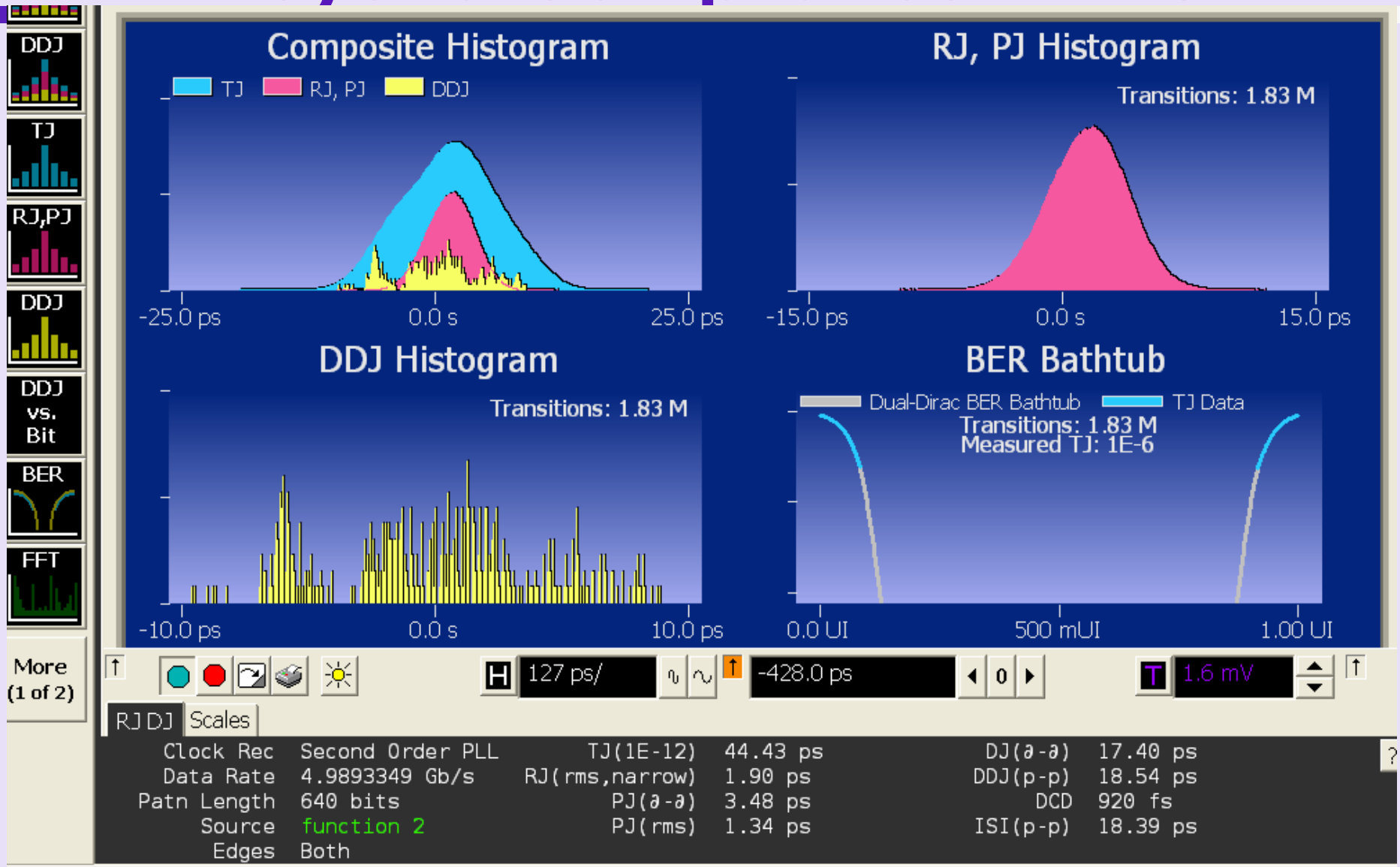
HTML based automatic report generator allows you to easily share test results.

Select the version to test

Select the test point



# Beyond Compliance – EZJIT+



# Achieve Success at 5GT/s with Good designs and Standardized Tools

- Tools are making significant progress for PCIe 2.0 AIC and 2 port System compliance tests.
- De-embed fixtures and cabling to fully characterized your design – give the margin back to your DUT
- Easy to use sophisticated tests allow you to expertly execute accurate tests with repeatable results
- Use SigTest tools provide by the PCI-SIG to determine design margins
- Complex Jitter analysis can provide design directions to solving marginal jitter budgets.

Thank you for attending the
PCI-SIG Developers Conference 2007.

For more information please go to
www.pcisig.com


# Mastering Physical Layer Compliance Challenges at 5GT/s

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