PCI Express® Electrical Basics

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Topics

- PCI Express® Electrical Overview
- Target channels for the specification
- Electrical signaling for 2.5GT/s and 5GT/s
- Transition to 8GT/s and rationale
- Electrical enablers for 8GT/s

Electrical Features

- Data rates 2.5GT/s, 5GT/s and 8GT/s*
- 10^{-12} bit error ratio
- AC coupled
- Link widths 1, 2, 4, 8, 16, 32 lanes
- Hot swap capable
- 2.5 and 5GT/s scrambled + 8b10b
- 8GT/s scrambled + 128/130*
- Power management

** Spec in development*

Power Management

- There are four power states defined
  - ✓ L0 – operational
  - ✓ L0s – fast wake-up (<10ns)
    - Tx and Rx disabled, clocks running or fast recovery, short CDR relock
  - ✓ L1 – medium wake-up (<10us)
    - Tx and Rx disabled, clocks off, normal CDR and symbol lock, FIFO initialization
  - ✓ L2 – longest wake-up (<1ms)
    - Mostly powered down, power-on recovery, full link training, speed negotiation etc

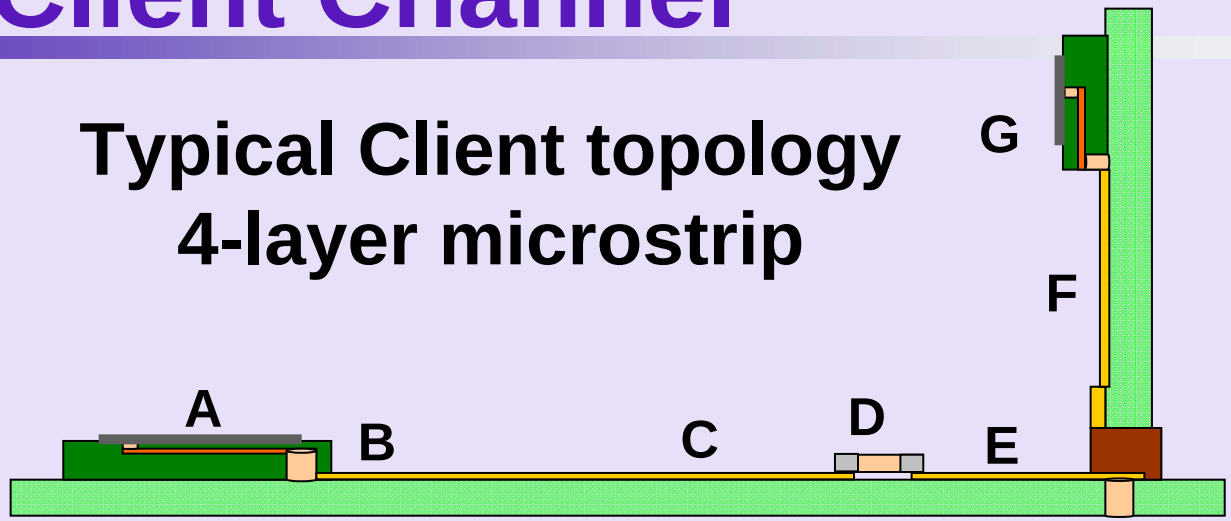
Target Channels

PCI Express Channels

- No formal channel spec
  - ✓ Channel budget implied
  - ✓ Card Electromechanical (CEM) spec sets limits and measurement points
- Two worst case models assumed
  - ✓ Client CEM
    - Short to medium length (3-12”), reflection and crosstalk dominated
  - ✓ Server CEM
    - Medium to long (20”) loss dominated

Client Channel

Typical Client topology
4-layer microstrip

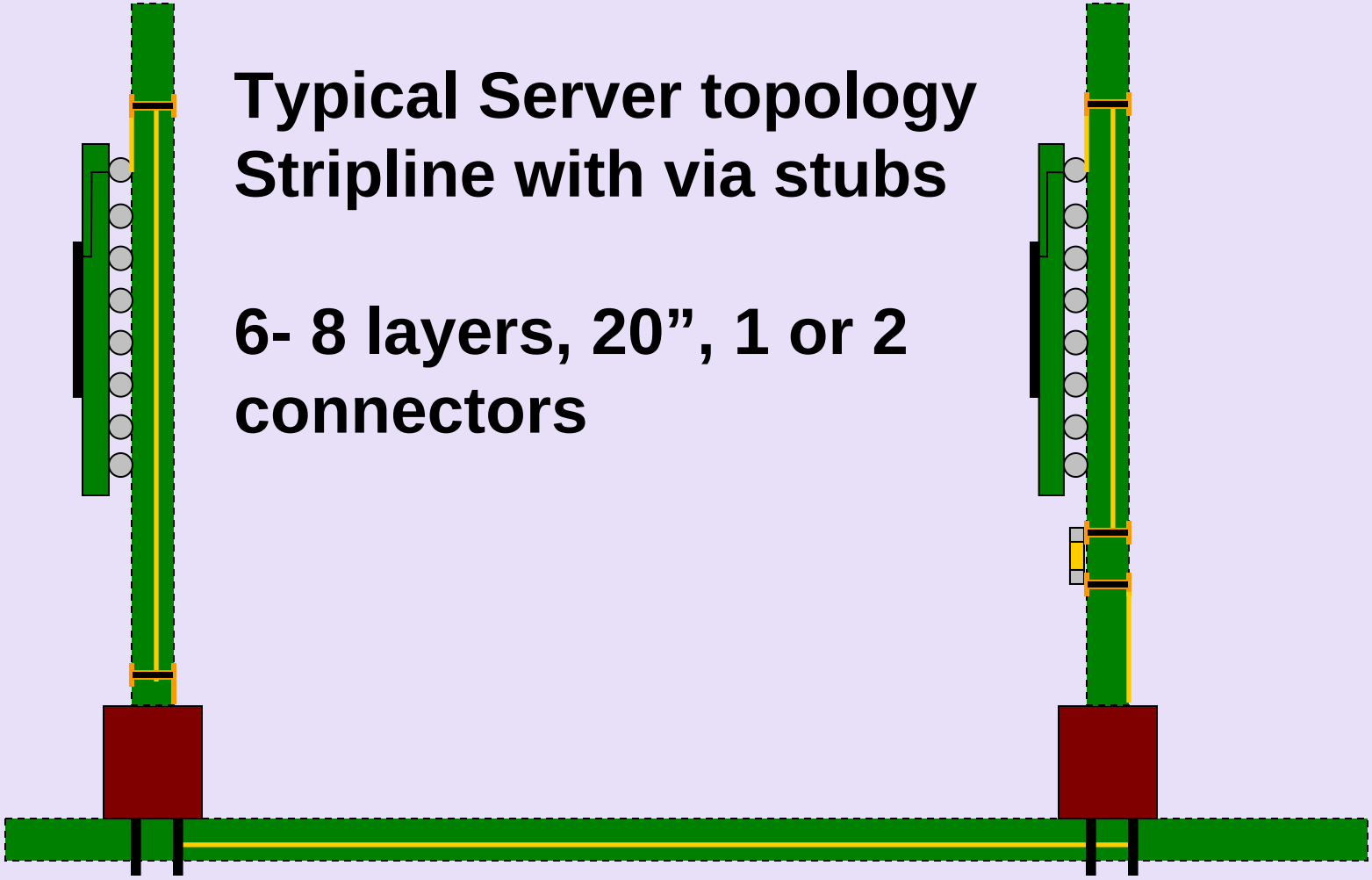


Seg	Description
A	RC PKG (transmitter)
B	RC break-out ~1”
C	MB Main 3-7”
D	MB coupling cap
E	Add in card break in 3”
F	EP break-out
G	EP PKG (receiver)

Server Channel

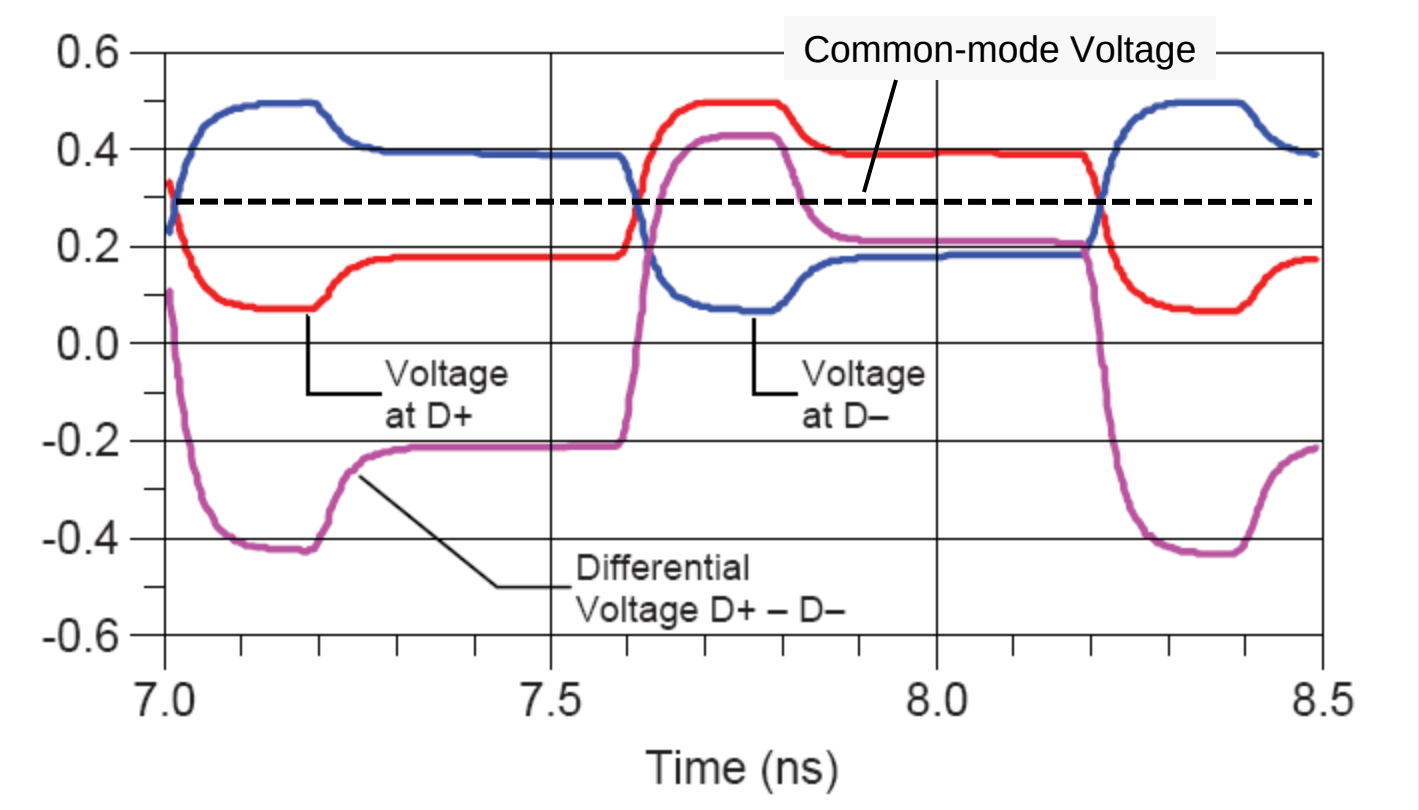
Typical Server topology
Stripline with via stubs

6- 8 layers, 20”, 1 or 2 connectors

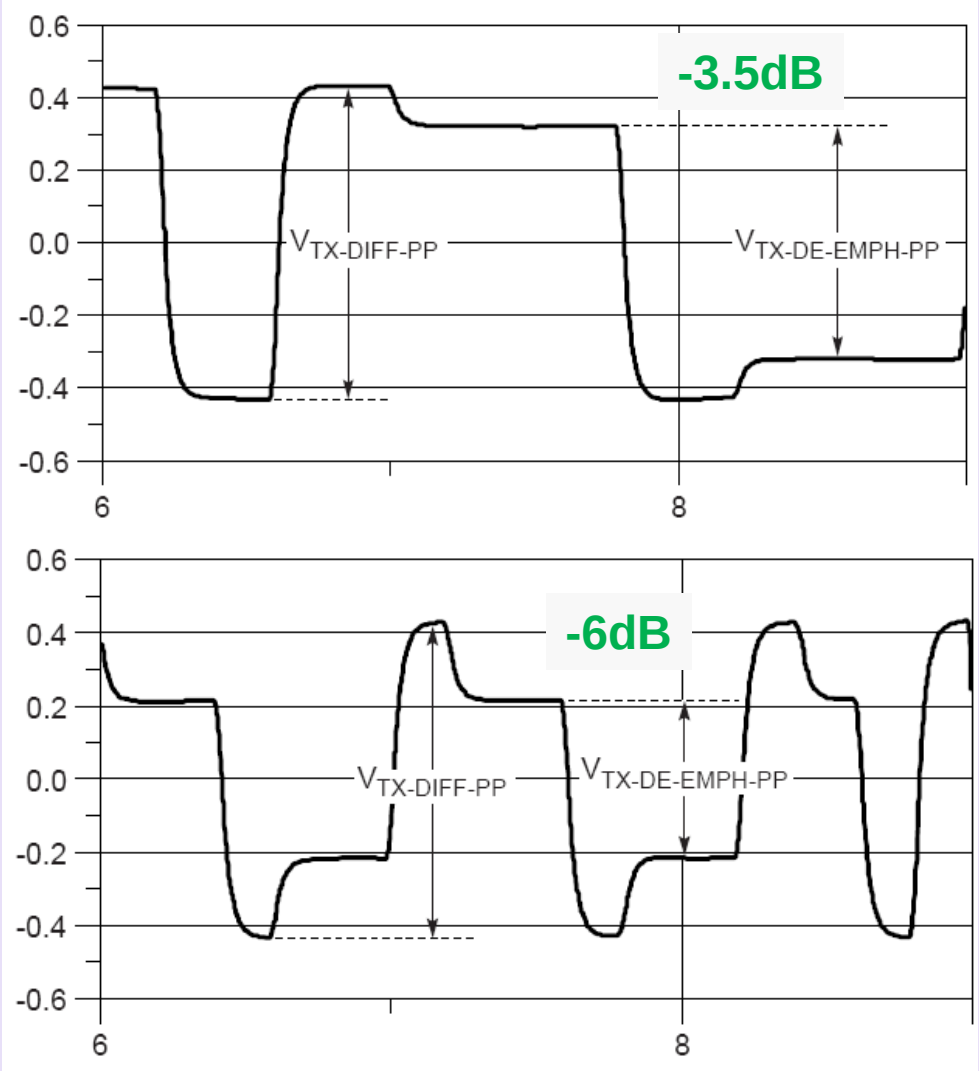


Electrical signaling for 2.5GT/s and 5GT/s

Voltage Definitions



De-emphasis



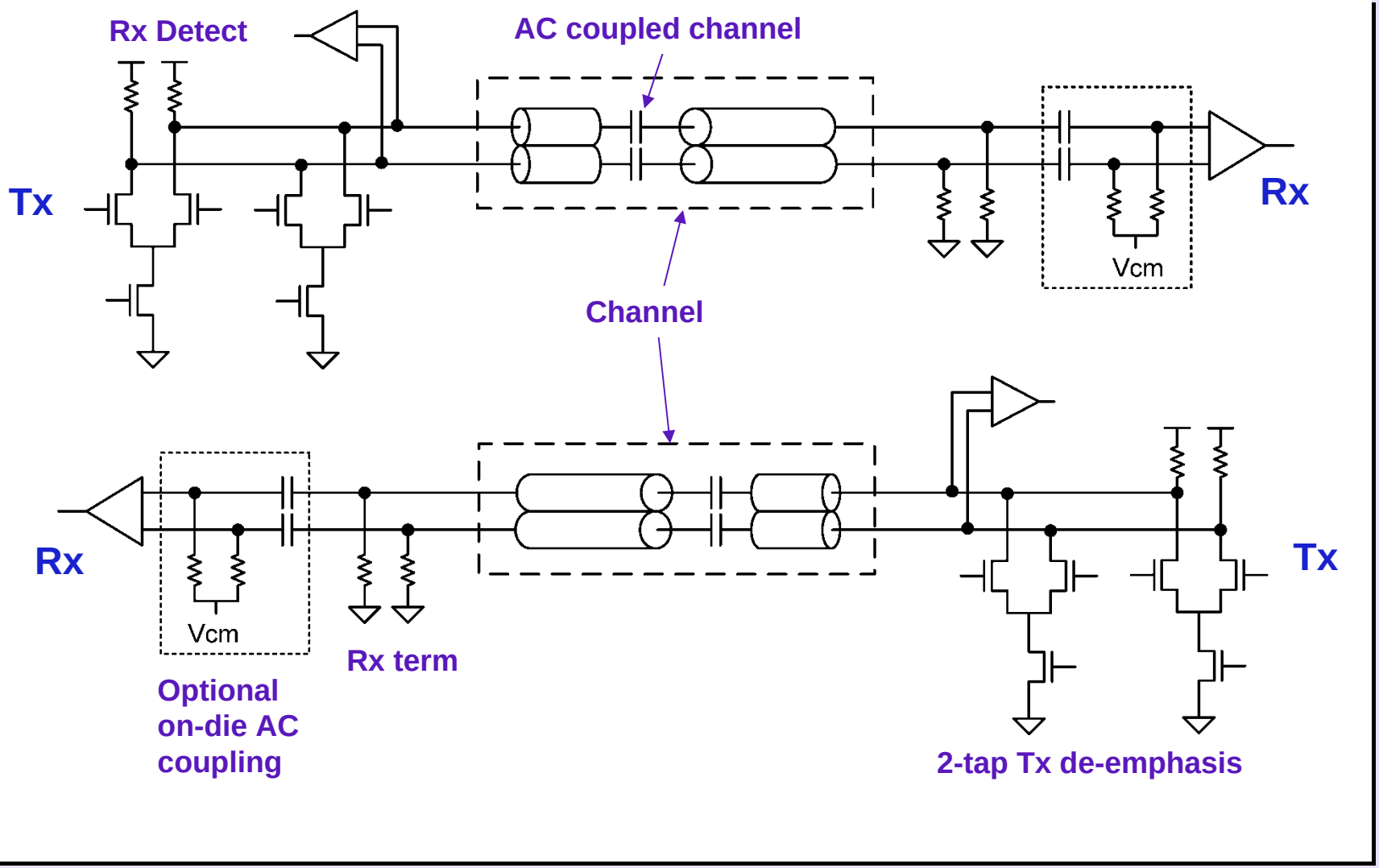
The transmitter uses de-emphasis to equalize the HF loss of the channel

Approximates the inverse of the channels step response

Two settings:

- -3.5dB for 2.5GT/s and 5GT/s
- -6dB for 5GT/s

Transceiver and Channel



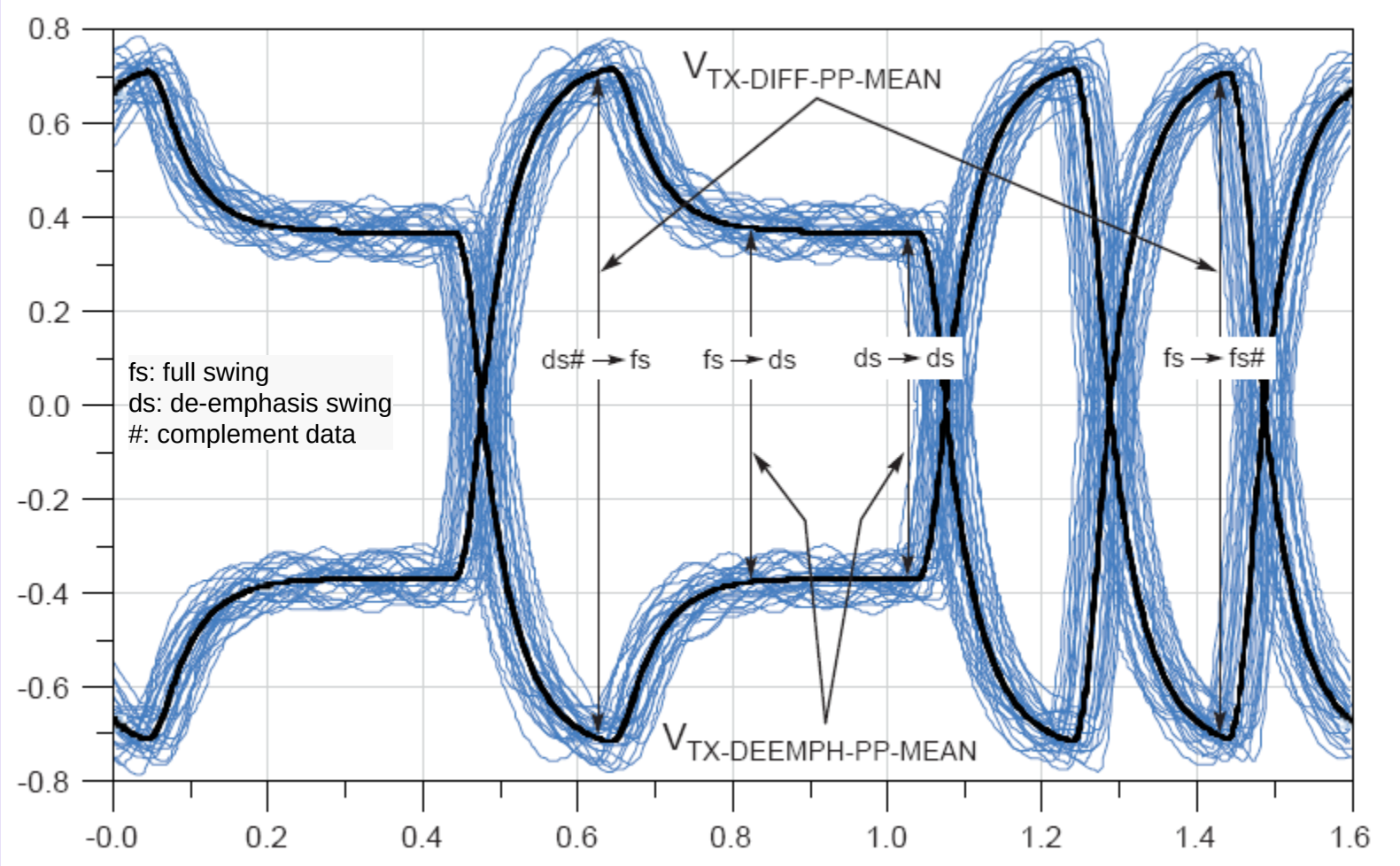
Transmitter 2.5 and 5GT/s

- Differential ~100ohm transmitter
  - ✓ FS: 800-1200mV, HS: 400-800mV
  - ✓ 0.75UI eye opening
- Two tap FFE
  - ✓ FS: -3.5dB and -6dB, HS: 0dB
- AC coupled channel
  - ✓ 75-200nF series capacitor
- Return Loss
  - ✓ SDD11 -10dB 2.5GT/s, -8dB 5GT/s
  - ✓ SCC11 -6dB

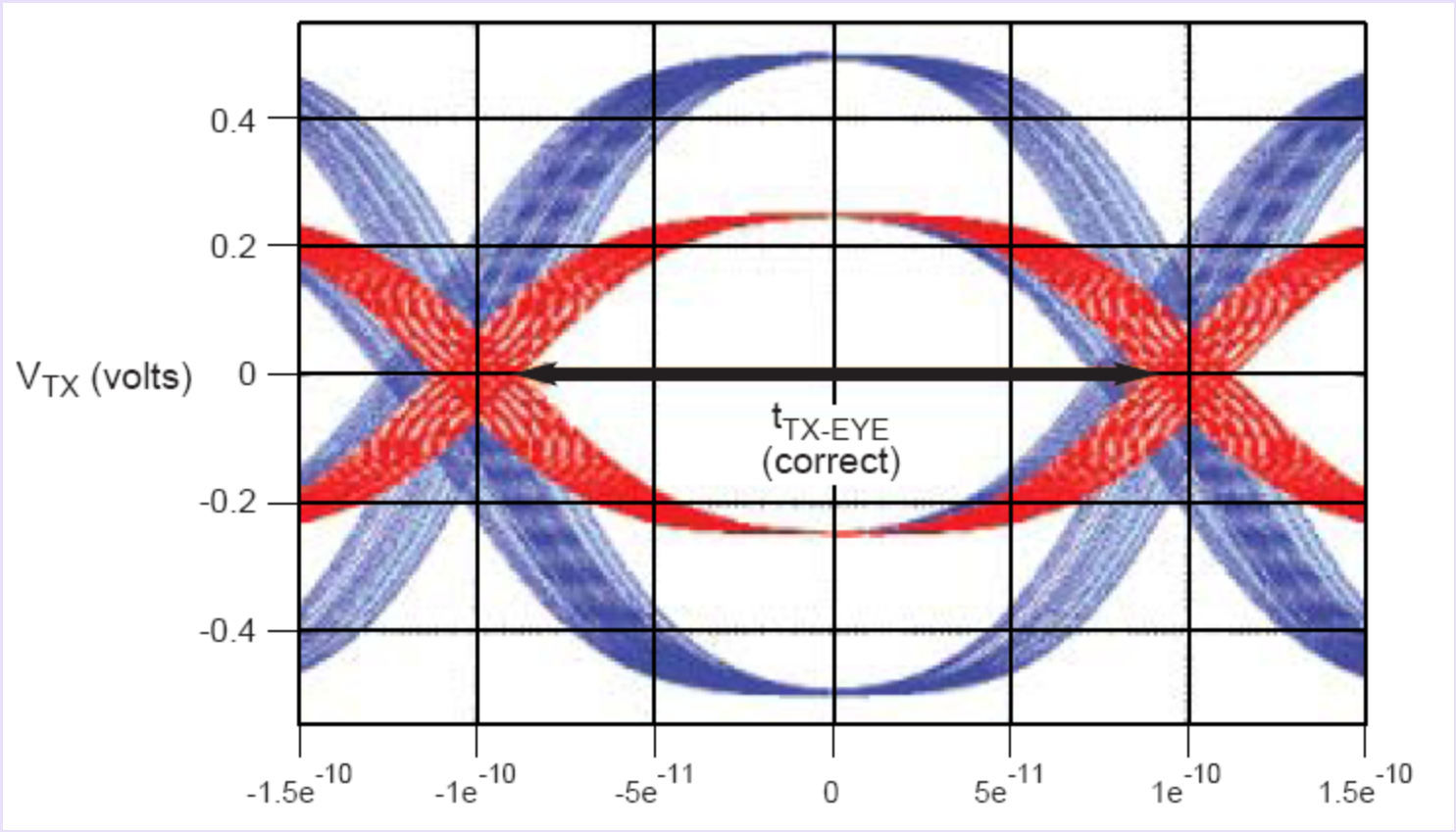
Transmitter cont.

- Receiver Detect
  - ✓ Tx pulses common-mode and measures RC charge time of coupling caps
  - ✓ Rx enables input termination to indicate presence for training
- Electrical Idle
  - ✓ Low power, zero-differential, Tx common-mode maintained
  - ✓ Used in L0s, L1 and L2
- Beacon (optional)
  - ✓ EP breaks Electrical Idle and signals to RC complex it needs to send traffic

Averaged Eye Diagram



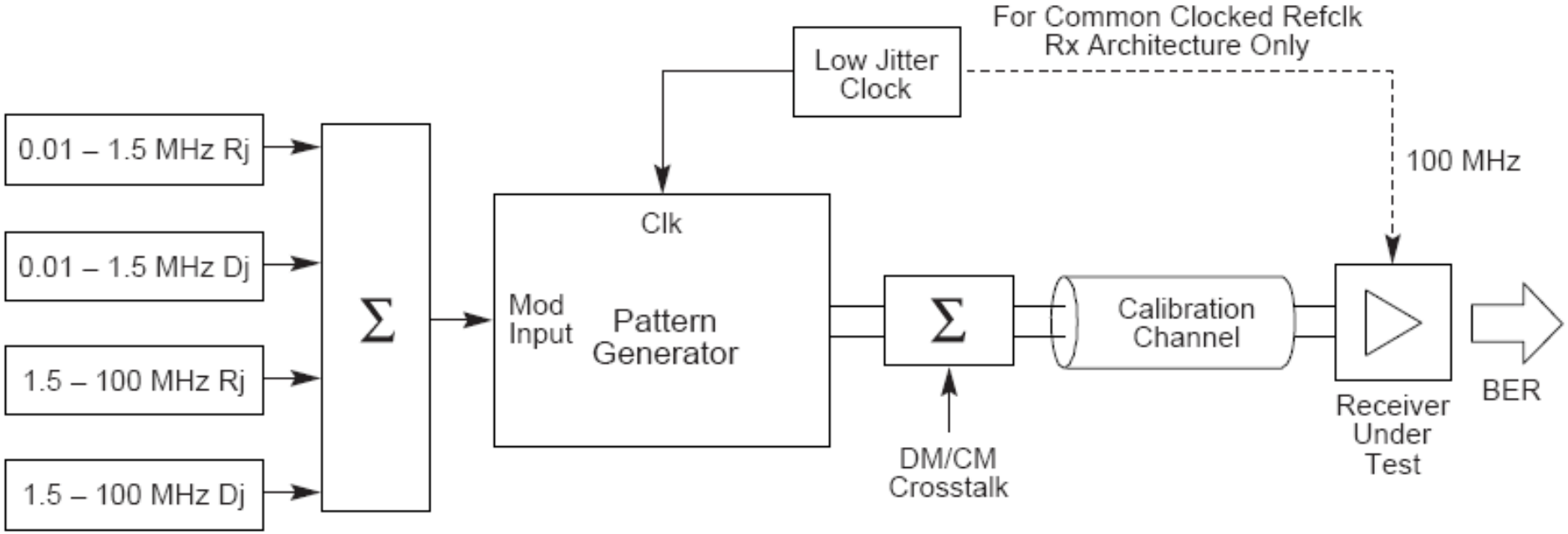
Removing De-emphasis Jitter



Receiver 2.5 and 5GT/s

- Open Eye standard, validated at device pin, package included in device budget
  - ✓ Eye height 175/120mV 2.5/5GT/s
  - ✓ Eye width 0.4/0.32UI 2.5/5GT/s
  - ✓ AC common-mode 300mV pk-pk
  - ✓ 100ohm differential termination
    - 0v common-mode for detect
  - ✓ SDD11 -10dB 2.5GT/s, -8dB 5GT/s
  - ✓ SCC11 -6dB

Receiver Compliance Testing

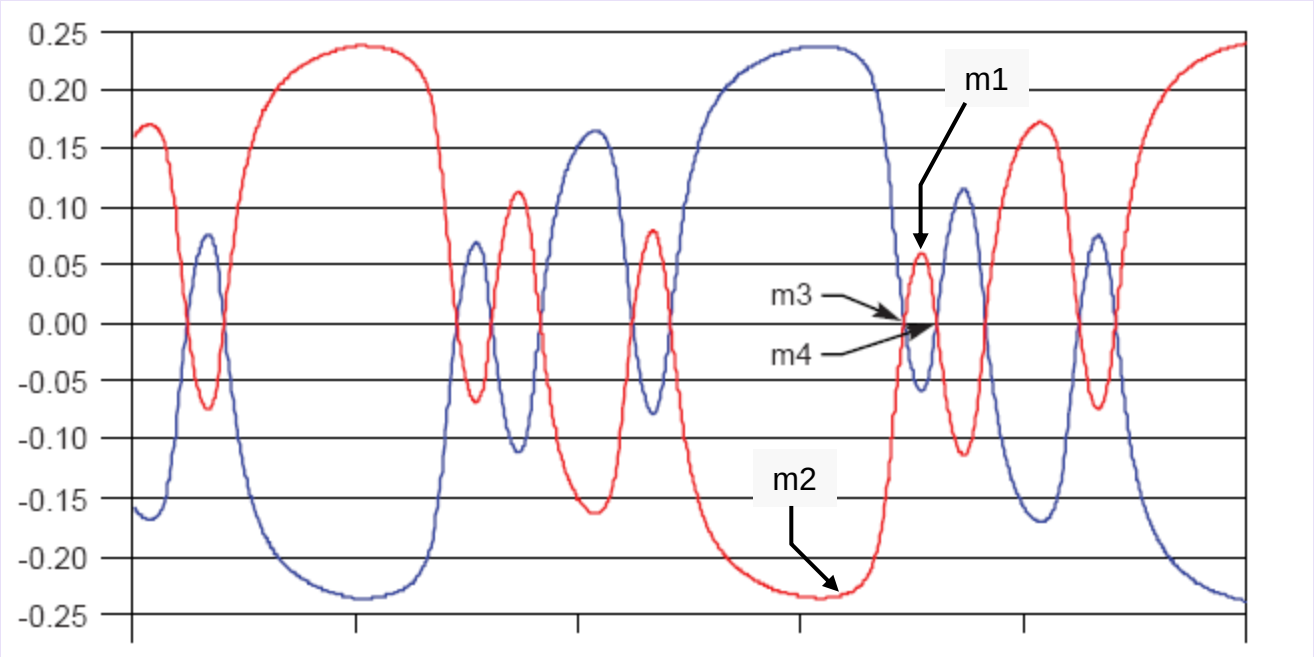


Stressed eye calibrated at pin reference plane

Error rate measured using loopback

Pass BER 10^{-12}

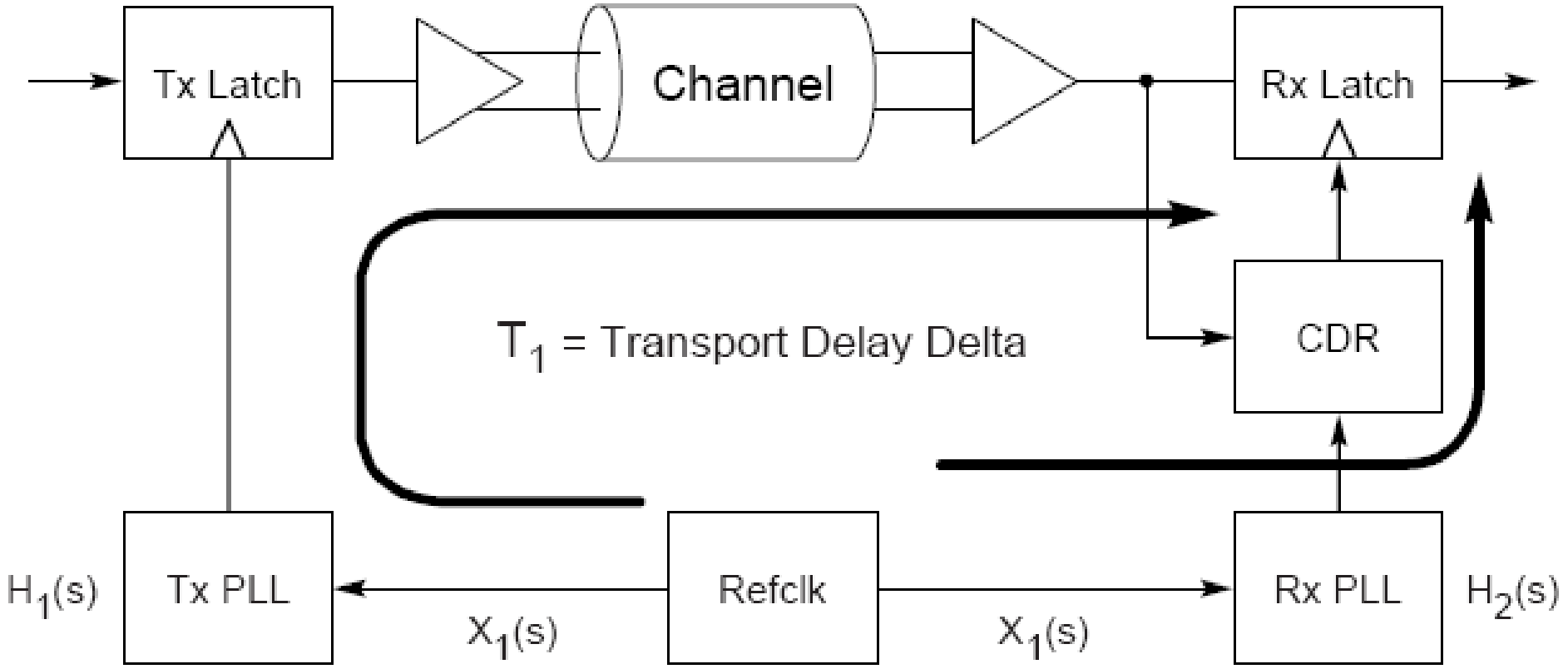
Stressed Eye Calibration



Stressed Rx eye must simultaneously meet:

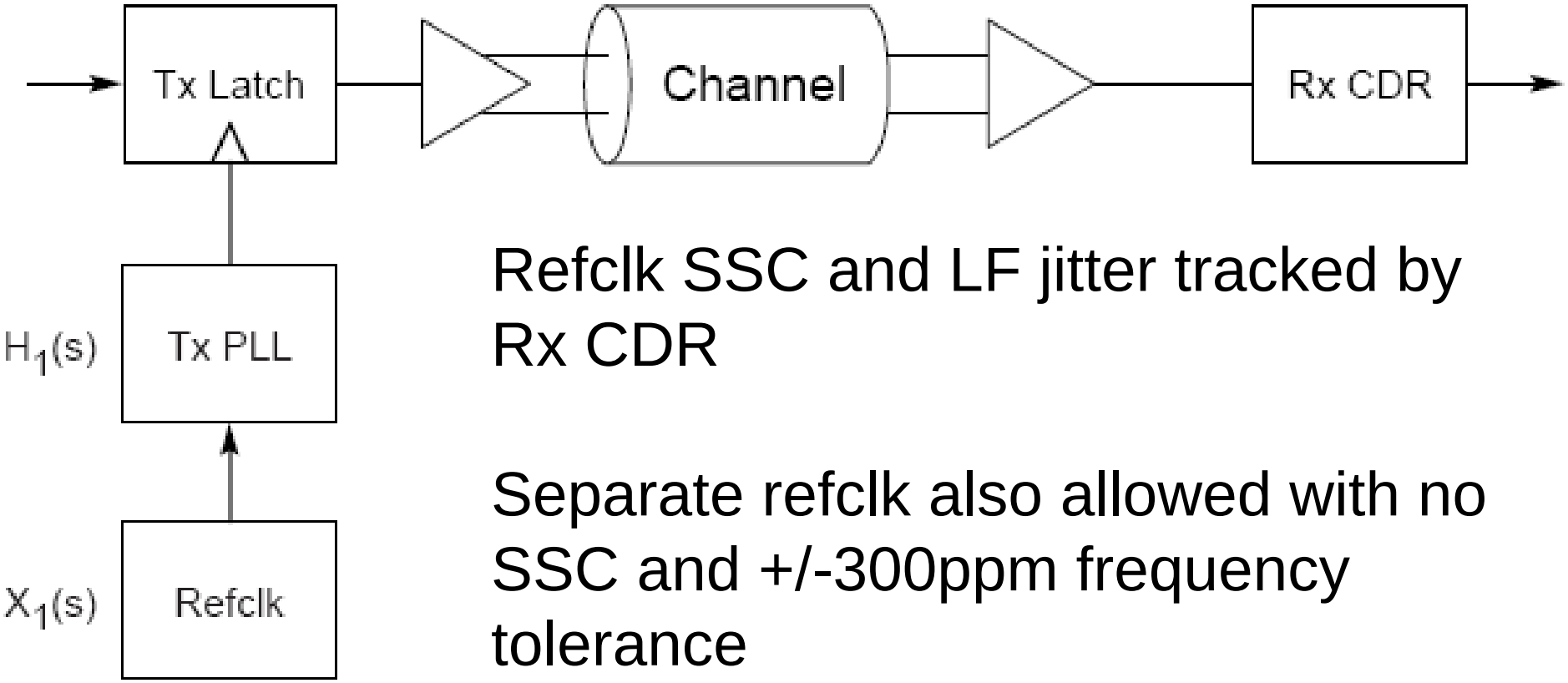
- Eye height (m1 all eye centers)
- Eye width (all crossing times)
- Minimum pulse width (m4-m3)
- Min-max ratio (m2:m1)

Common Reference Clock



Refclk SSC and LF jitter common-mode to Tx and Rx

Data Clocked Receiver



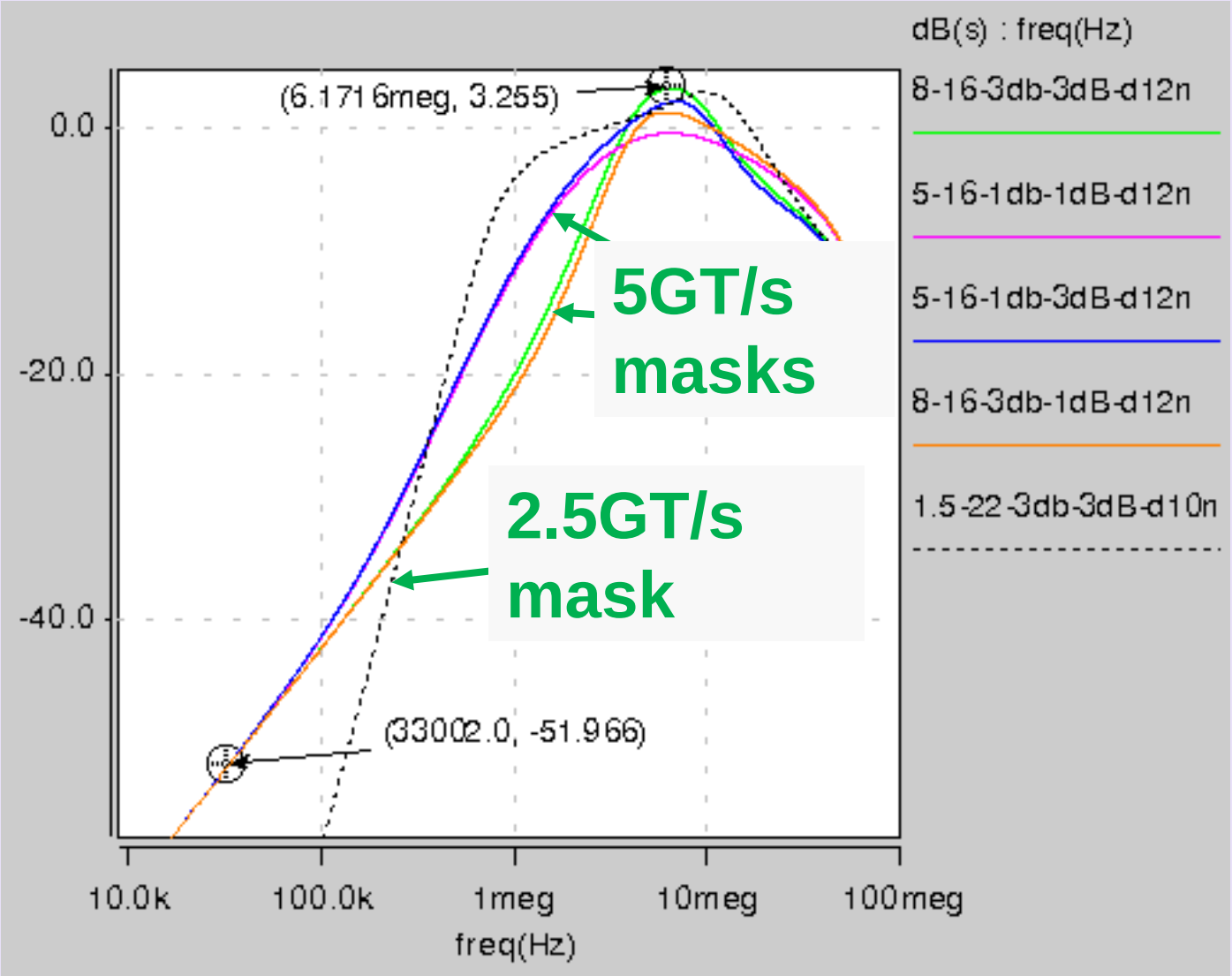
Refclk SSC and LF jitter tracked by Rx CDR

Separate refclk also allowed with no SSC and +/-300ppm frequency tolerance

Reference Clock Specification

- Bounds jitter for common reference clock architecture
  - ✓ Data clocked architecture must operate with this jitter definition
- Multiplying PLL Tx/Rx bandwidth specified
  - ✓ 2.5GT/s 1.5-22MHz 3dB peaking
  - ✓ 5GT/s 5-16MHz 1-3dB peaking
  - ✓ 2.5GT/s CDR bandwidth >1.5MHz
- PLL difference function and transport delay defines reference clock masks

Reference Clock Jitter Masks



Proposed 8GT/s specifications

This following provides a snapshot of the work in progress in the PCI Express Electrical Working Group. This specification work is not finalized and has not been ratified by the PCI SIG membership.

Doubling from 5GT/s

- Major goal is to make PCIe® 3.0 evolutionary
  - ✓ Support existing usage models
  - ✓ Preserve Common Reference Clock and Data Clocked modes
  - ✓ Re-use of 5GT/s reference clock generators
  - ✓ Re-use of silicon PHY architectures
- Evaluated channels at 10GT/s and 8GT/s
  - ✓ 10GT/s allows 8b10b coding to be preserved

8GT/s Wins

- Shown that a non-linear increase in difficulty to reach 10GT/s
  - ✓ Increased channel improvement cost
  - ✓ Increased power in silicon
  - ✓ Increased difficulty for eco-system
- Concluded the cost of changing encoding acceptable
  - ✓ Work started on defining a new scrambled encoding scheme
  - ✓ Efficiency to be 20% better than 8b10b

New Encoding Scheme

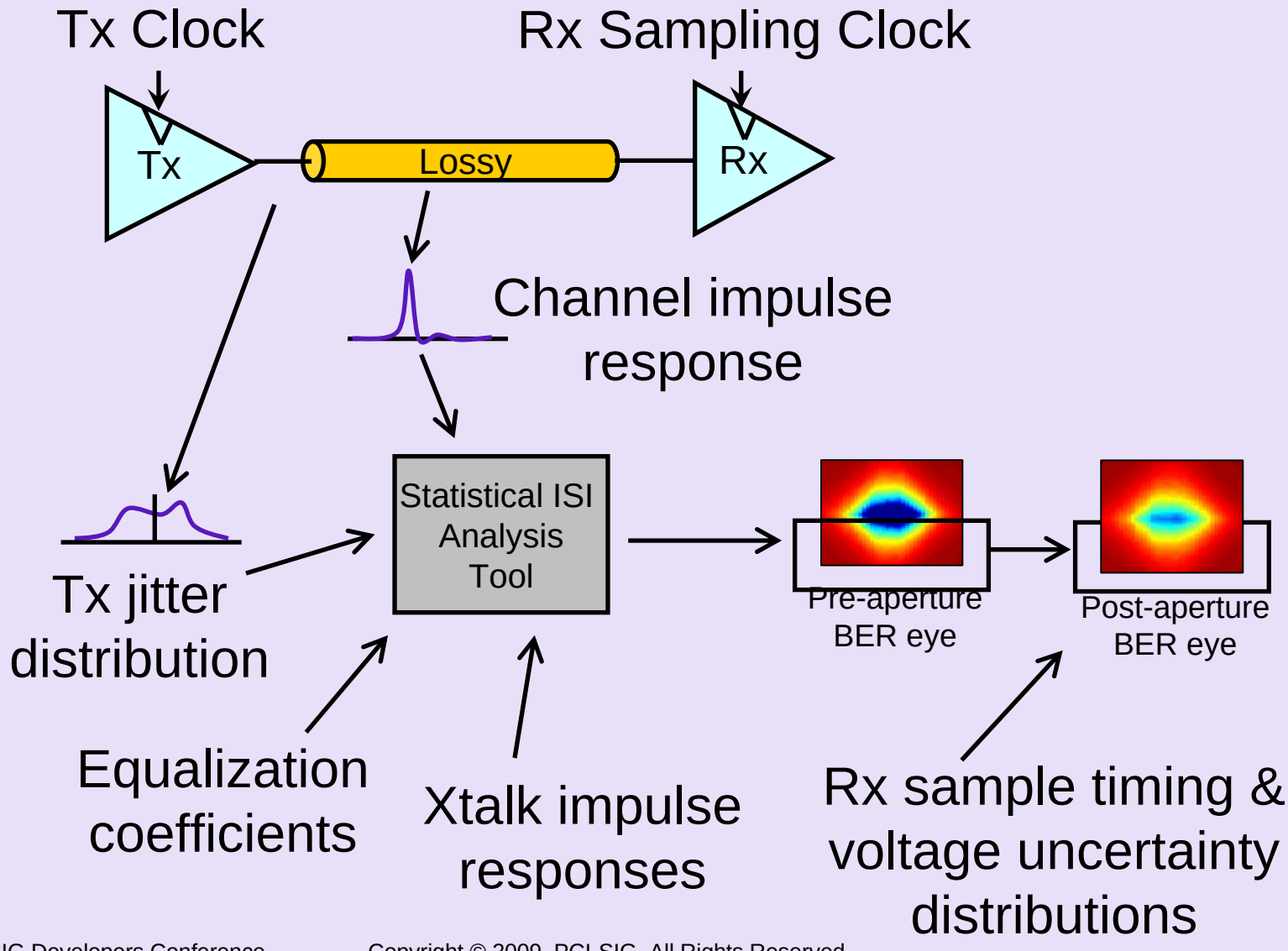
- 2 levels of encapsulation
  - ✓ 128/130 code on individual lanes
    - 130 bit Block used for Block lock
    - 2 bit header distinguishes payload
  - ✓ Physical layer packetization identifies packet boundaries
    - Link Level (TLP and DLLP) across lanes
    - Lane Level (Ordered Sets or Link Idle)
- Scrambling for 128 bit payload
  - ✓ Additive EXOR with 23bit LFSR
  - ✓ Electrical Idle Exit resets scrambler

8GT/s Electrical Enablers

8GT/s Enablers

- Use statistical channel analysis
- Reduce reference clock jitter sensitivity
  - ✓ Tx/Rx PLL lower bandwidth
  - ✓ Increase CDR bandwidth
- Mitigate baseline wander and crosstalk
  - ✓ Polynomial choice
  - ✓ LFSR offsets between adjacent lanes
- Receiver equalization required
- Introduce channel compliance
  - ✓ Channel simulation with behavioral Tx/Rx

Statistical System Analysis



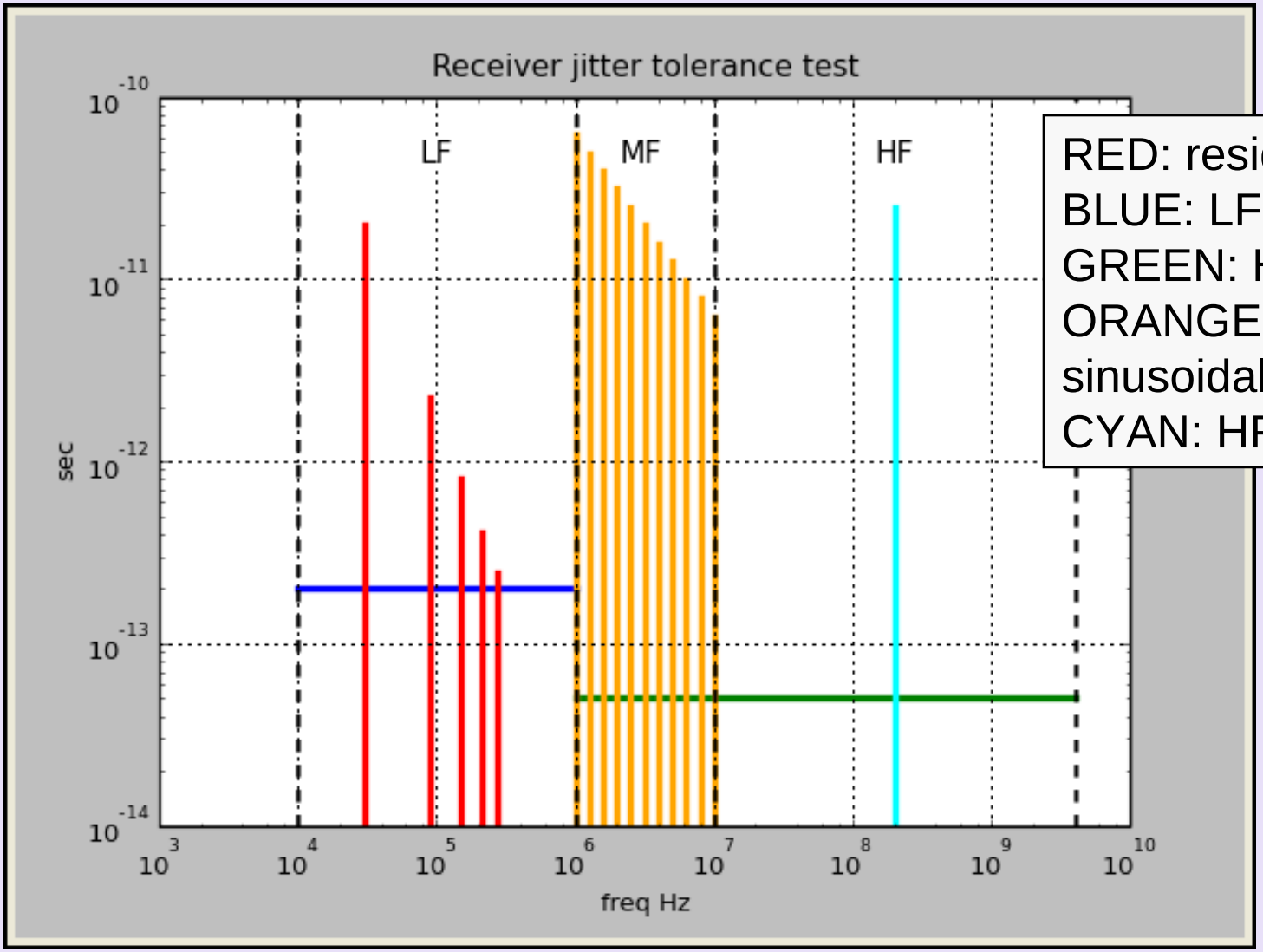
Reference Clock

- Reduce sensitivity to reference clock jitter
  - ✓ Tx and Rx PLL
    - Matched and lower bandwidth
  - ✓ Increase CDR bandwidth 10MHz
    - 8GT/s Rx tolerance tests CDR phase tracking
    - 2.5GT/s assumed a minimal 1.5MHz bandwidth
  - ✓ Bang-bang digital CDR implementations can meet this requirement
    - Expectation is that existing Rx CDR's can be modified to meet specification

Reference Clock Filtering

- New PLL difference function as defined for 2.5GT/s with new parameters:
  - ✓ 2-4MHz PLL BW 1dB peaking
  - ✓ 10MHz high pass for CDR
  - ✓ 12ns transport delay
  - ✓ <1ps RMS HF jitter
- Requires additional post-processing of reference clock measurement
  - ✓ Expect existing 5GT/s ref clocks will pass

Receiver Tolerance Testing

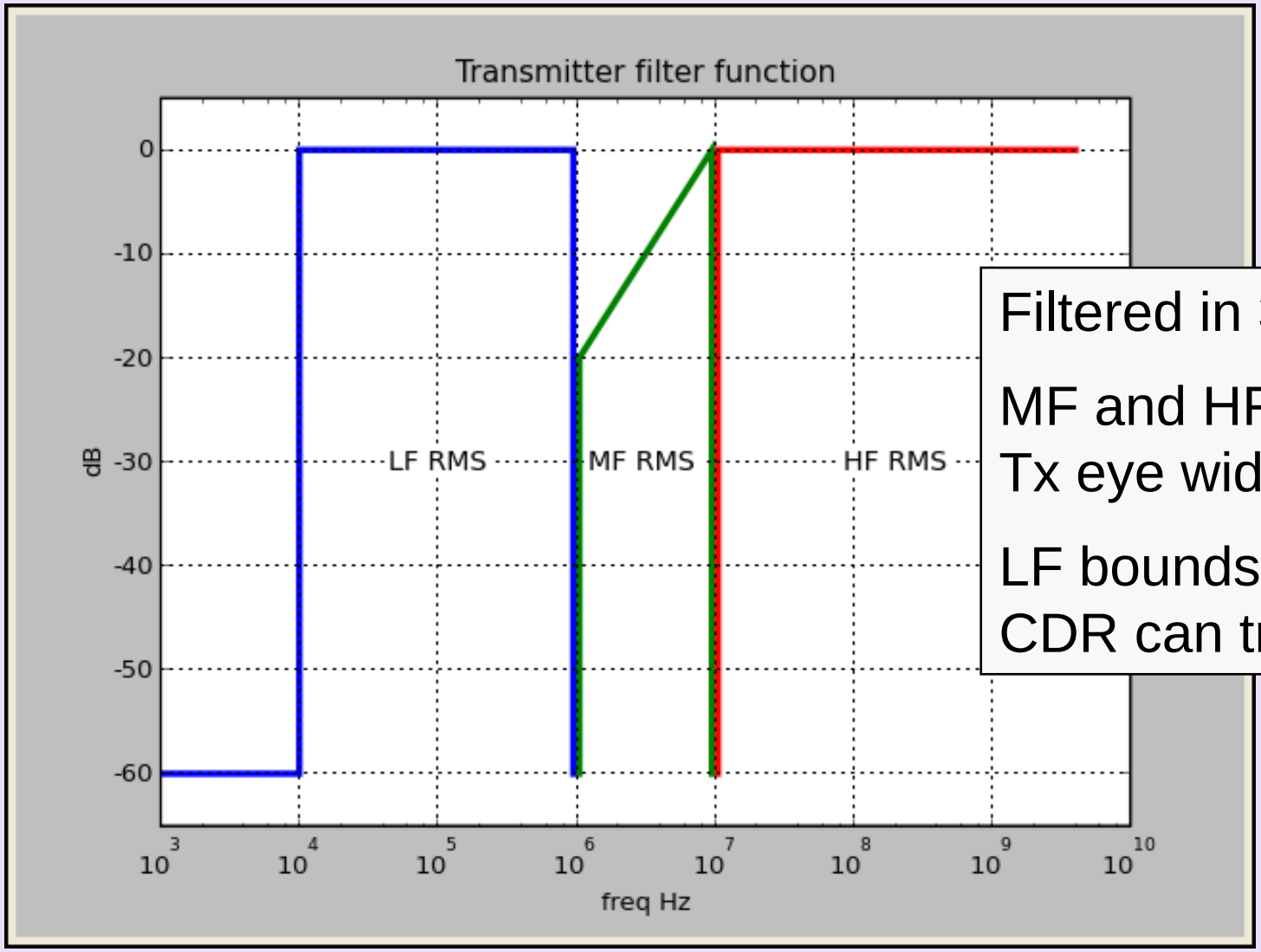


RED: residual SSC
BLUE: LF RMS
GREEN: HF RMS
ORANGE: MF swept sinusoidal
CYAN: HF DJ

Transmitter Reference Plane

- Reference plane remains at DUT pin
  - ✓ Same as 2.5 and 5GT/s
  - ✓ Most convenient manufacturing boundary
  - ✓ Package losses are part of Tx performance
- At 8GT/s die pad, package route and package pin interactions are more significant
  - ✓ Makes fixture de-embedding inaccurate
  - ✓ Measuring Tx equalization is difficult

Transmitter Jitter Filtering



Filtered in 3 bands

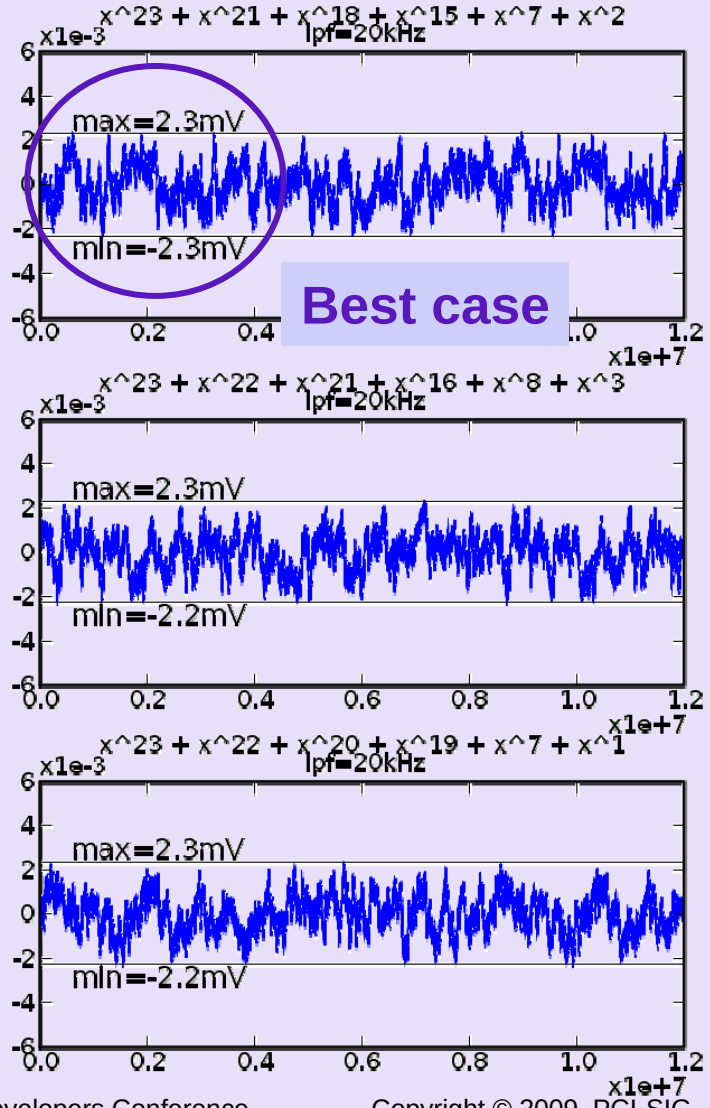
MF and HF determine Tx eye width

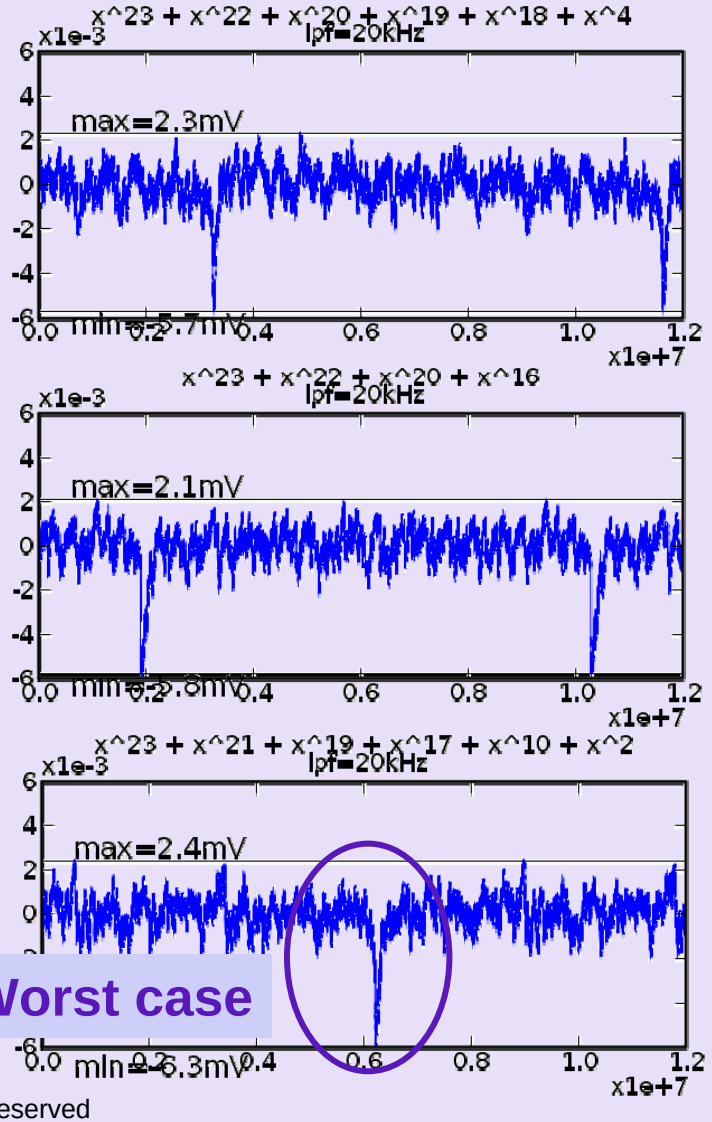
LF bounds jitter that CDR can track

Baseline Wander from PRBS

- PRBS provides sufficient transition density but does not preserve DC balance
  - ✓ Creates a slow changing differential offset that reduces eye height
- Different polynomials have different peak offsets
  - ✓ Need to find the best polynomial for AC coupling time constant
- Random data improves bad PRBS sequences
  - ✓ Worst case is free-running scrambler

Three Best and Worst Results



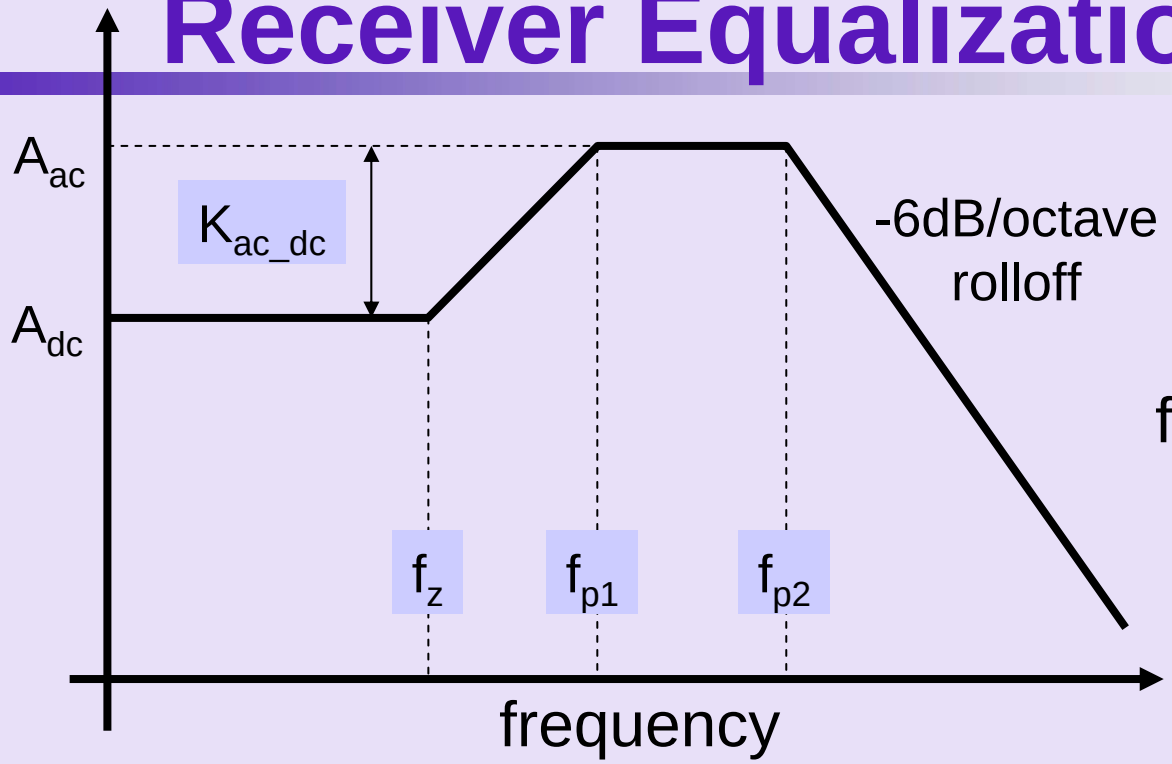


Lane to Lane Crosstalk

- Adjacent lanes need an offset to their LFSR generation to avoid all lanes switching together during periods of idle data
- Evaluation of different LFSR offsets schemes found it better to make lane offsets to be dependent on each other
  - ✓ Reduces simultaneous switching

Red: vict+2aggr; pink: vict+1aggr; black: vict only

Receiver Equalization



$$f_{p1} = f_z * K_{ac\_dc}$$

Reference equalizer minimum Rx requirement

- f_{p2} 8GHz for spec (implementation dependent)
- f_{p1} can be fixed ~2GHz
- K_{ac_dc} provides tuning, 6-12dB <=1dB steps

Thank you for attending the PCI-SIG Developers Conference 2009

For more information please go to
www.pcisig.com