PCIe® 3.0 Cards

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Disclaimer

The information in this presentation refers to a specification still in the development process. This presentation reflects the current thinking of the workgroup, but all material is subject to change before the specification is released. The CEM specification 1.0 is awaiting completion of 12 mechanical ECNs planned for integration in the final 1.0 document.

Agenda

- PCIe® 3.0 CEM Goals
- PCIe 3.0 CEM Simulation Methodology
- PCIe 3.0 Rev 1.0 Simulation Results
  - ✓ Motherboard (MB) and Add-in Card (AIC) TX spec limits
- MB TX Preset Selection
- Dual Port MB TX Test Method
- CEM RX Test Methodology
- Power and Thermal Update
- Summary and Conclusions

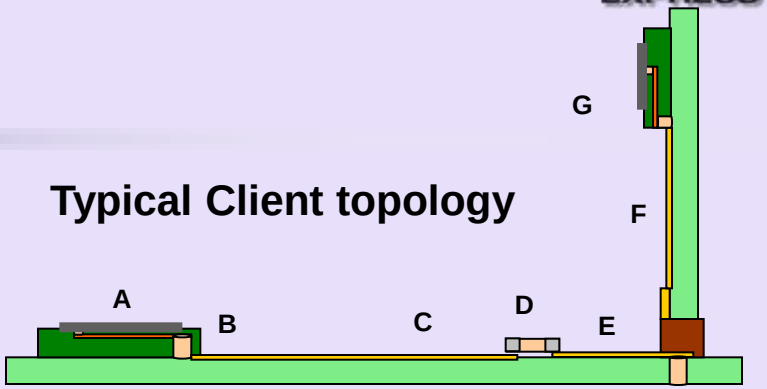
PCI Express 3.0 CEM Goals

- Same channel reach as for PCIe 2.0
  - ✓ Client: 14 inch, one connector
  - ✓ Server: 20 inch, two connectors
- Full backwards interoperability with PCIe 1.x, PCIe 2.0
- No required changes to the connectors, card form factors, or material
- Minimal or no changes to the measurement methodologies from those used in the PCIe 1.x/2.0 specifications
  - ✓ Use eye diagrams (jitter/voltage margin requirements). Minimize additional new requirements.

PCI Express 3.0 Channel Analysis

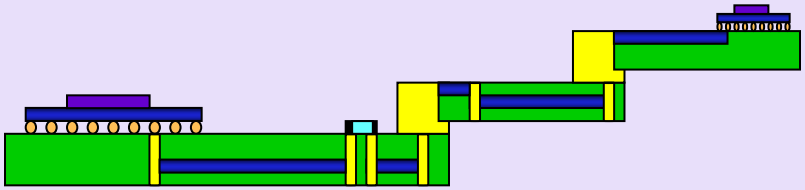
- Client
  - ✓ Motherboard and adapter
  - ✓ 1 PCIe connector
  - ✓ No vias other than connector
  - ✓ Routed as mstrip
  - ✓ Channel length: ~14”
- Server
  - ✓ Motherboard, riser card, and adapter
  - ✓ 2 PCIe connectors
  - ✓ Several vias on motherboard
  - ✓ Routed primarily as stripline
  - ✓ Channel length: ~20”
- Channel analysis includes corner cases

Typical Client topology



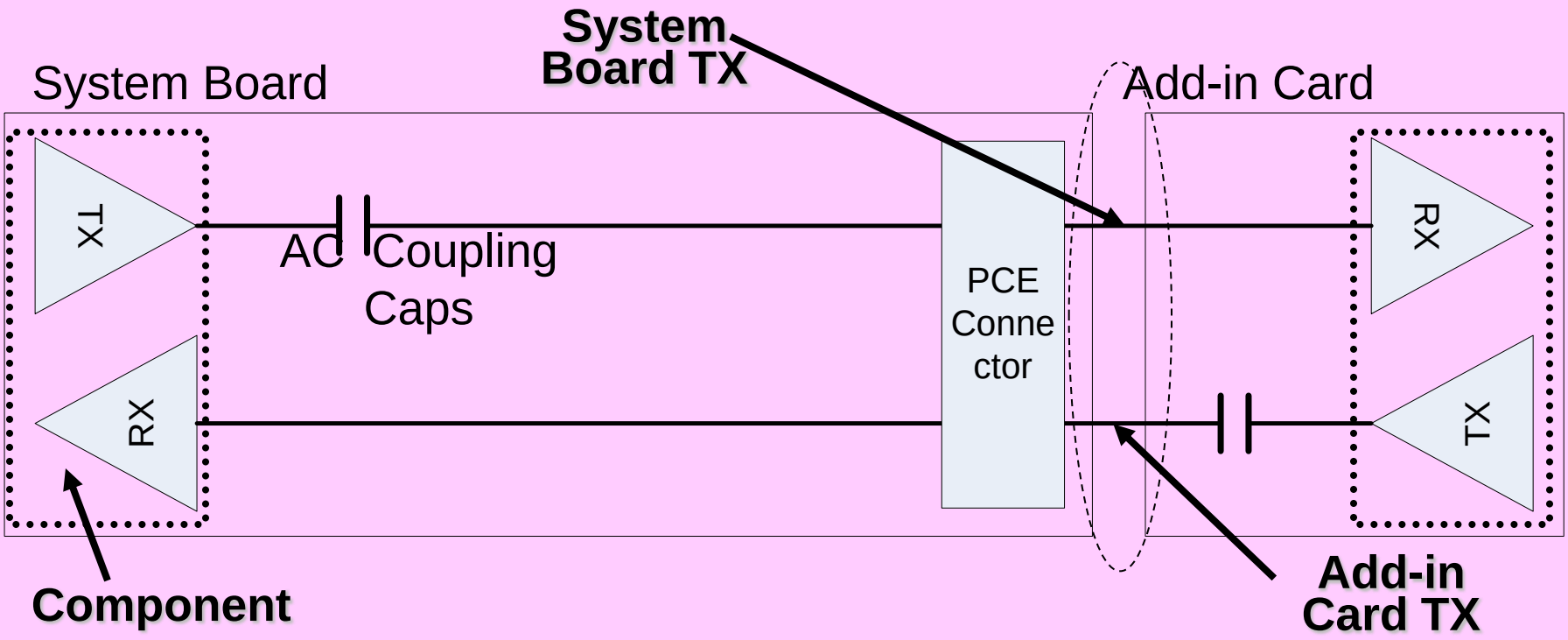
Seg	Description
A	MCH PKG (transmitter)
B	Break Out
C	MB Main 7”
D	MB post cap
E	Add in card main 3”
F	Add in card PKG Break out
G	Add in card PKG (receiver)

2 Connector Server topology



PCIe 3.0 targets support for the same channels and lengths as PCIe 2.0

CEM Spec – TX Path



CEM Spec Defines TX Requirements for Chip + Interconnect

No Separate TX Chip Or Interconnect Only Requirements

.9 CEM Simulation Details

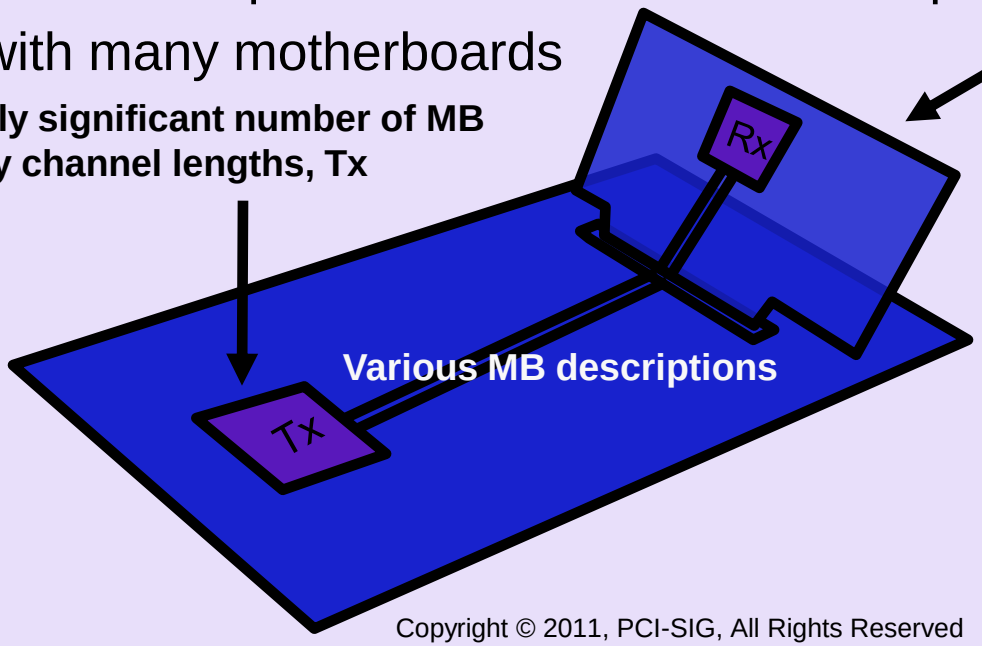
- Channels
  - ✓ Worst case 2 connector 16” server MB
  - ✓ Worst case 1 connecter 10” client MB
  - ✓ 4” microstrip Add-in card
- TX jitter following base spec limits
- Base spec package models for TX and RX packages
- Equalization
  - ✓ Adaptive 2-tap (pre/post) TX LE
  - ✓ Reference Equalizer – 1st order Adaptive RX CTLE + 1 Tap DFE
- Pass/Fail Decision for End To End (ETE) Simulations
  - ✓ Base Spec RX test stressed eye (25 mV and .3 UI)

PCIe 3.0 CEM Simulation Method Step 1: End to End (E2E) Simulations

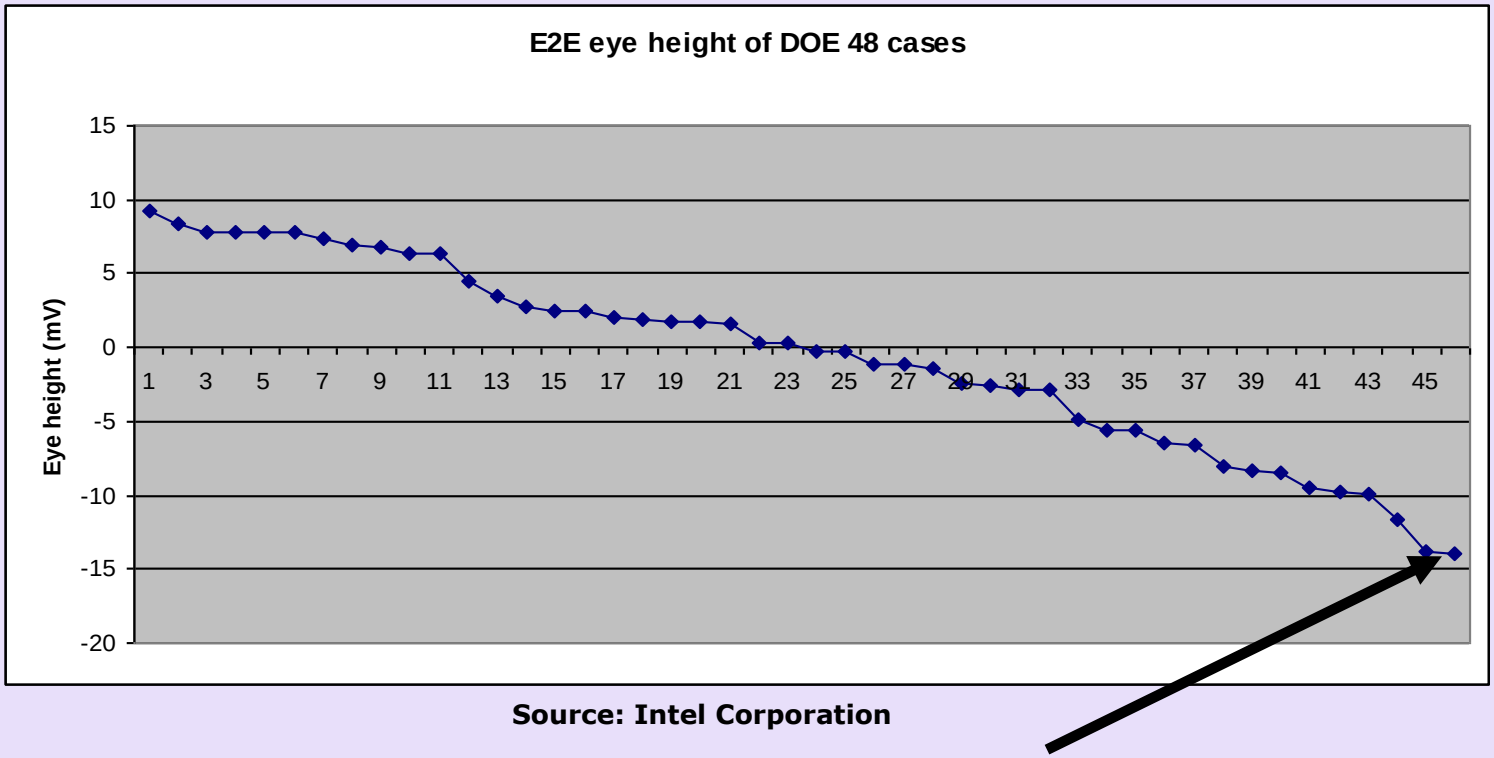
- Perform E2E simulations
  - ✓ Use target 1 connector and 2 connector solutions
  - ✓ Eye height (EH) and eye width (EW) examined after reference equalizer at eye pad
    - CTLE + 1 tap DFE and base spec package structure
    - Pass/fail determined by base spec RX test stressed eye
  - ✓ Statistical tools used for all simulations
- For each set of MB parameters determine worst case eye across expected add-in card solution space
- Repeat with many motherboards

Sweep add-in card parameters over reasonable solution space

Create a statistically significant number of MB descriptions. (Vary channel lengths, Tx params, etc.)



CEM Simulations – Worst Case Eye Height



Source: Intel Corporation

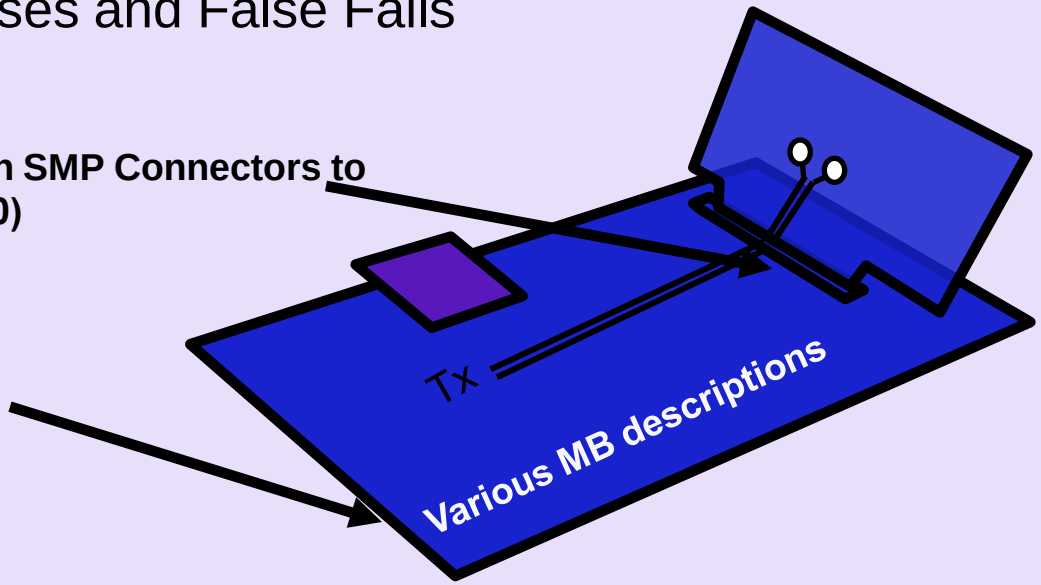
- Worst case Add-in card (AIC) parameters for given MB
- Repeat simulation with different MBs and find worst case for each
- THE ONLY POINT OF INTEREST FOR EACH SET OF MB PARAMETERS IS THE WORST CASE ACROSS ADD-IN CARD SOLUTION SPACE

PCIe 3.0 CEM Simulation Method Step 2: Test Fixture Simulations

- Choose a test fixture
  - 2.0 CLB Test Fixture Used For Initial Investigation
  - CEM spec pathfinding work showed better correlation with worst case E2E results with fixture with package model vs 2.0 CLB
- Repeat previous MB simulations with test fixture
  - Determine an eye mask at compliance Test Point
  - Find correlation between EH and EW at Test Point vs. E2E results
  - Use TX presets only to match expected compliance test
- Optimize number of False Passes and False Fails

Text fixture with SMP Connectors to 'scope (CLB 3.0)

Statistically significant number of MB Descriptions (same as E2E simulations)

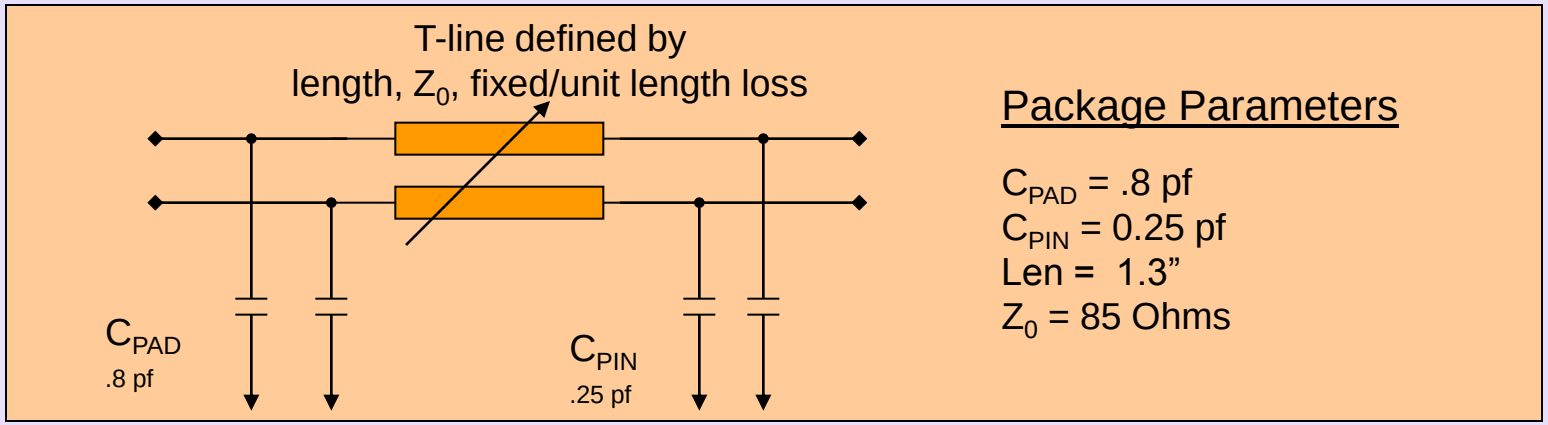


Package Test Fixture Topology

- 4” test fixture

Base Spec RX Package Structure

Source: Intel Corporation

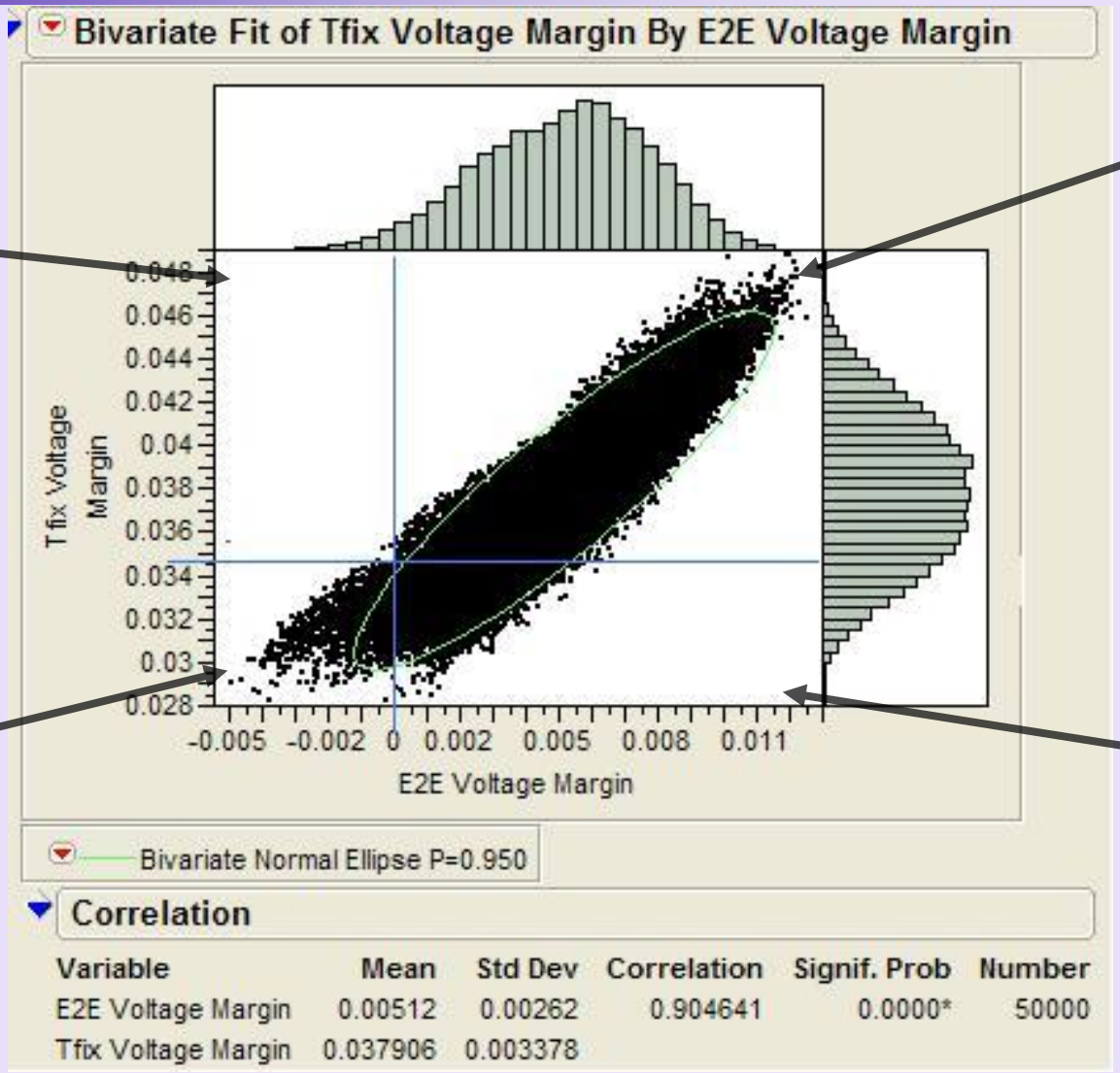


Package Parameters

C_{PAD} = .8 pf
C_{PIN} = 0.25 pf
Len = 1.3”
Z_0 = 85 Ohms

- **CEM spec pathfinding work showed better correlation with worst case E2E results with fixture with package model on test fixture**
- **Parameters shown for current CEM 3.0 CLB fixture proposal**
- **S parameters for fixtures used in CEM simulations are published**

Interpreting Simulation Results



"False Passes"

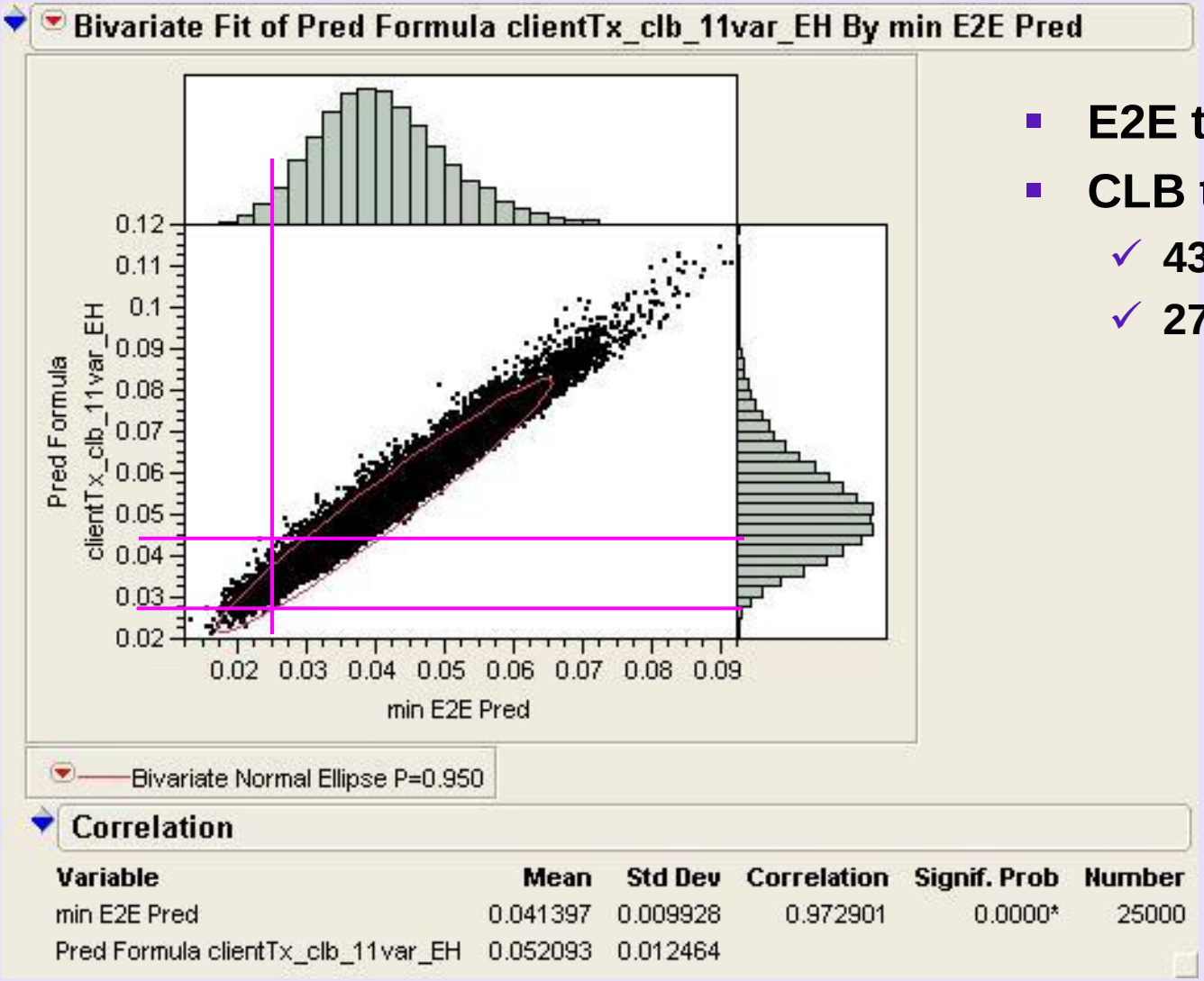
Passing Results

Failing Results

"False Failures"

Source: Intel Corporation

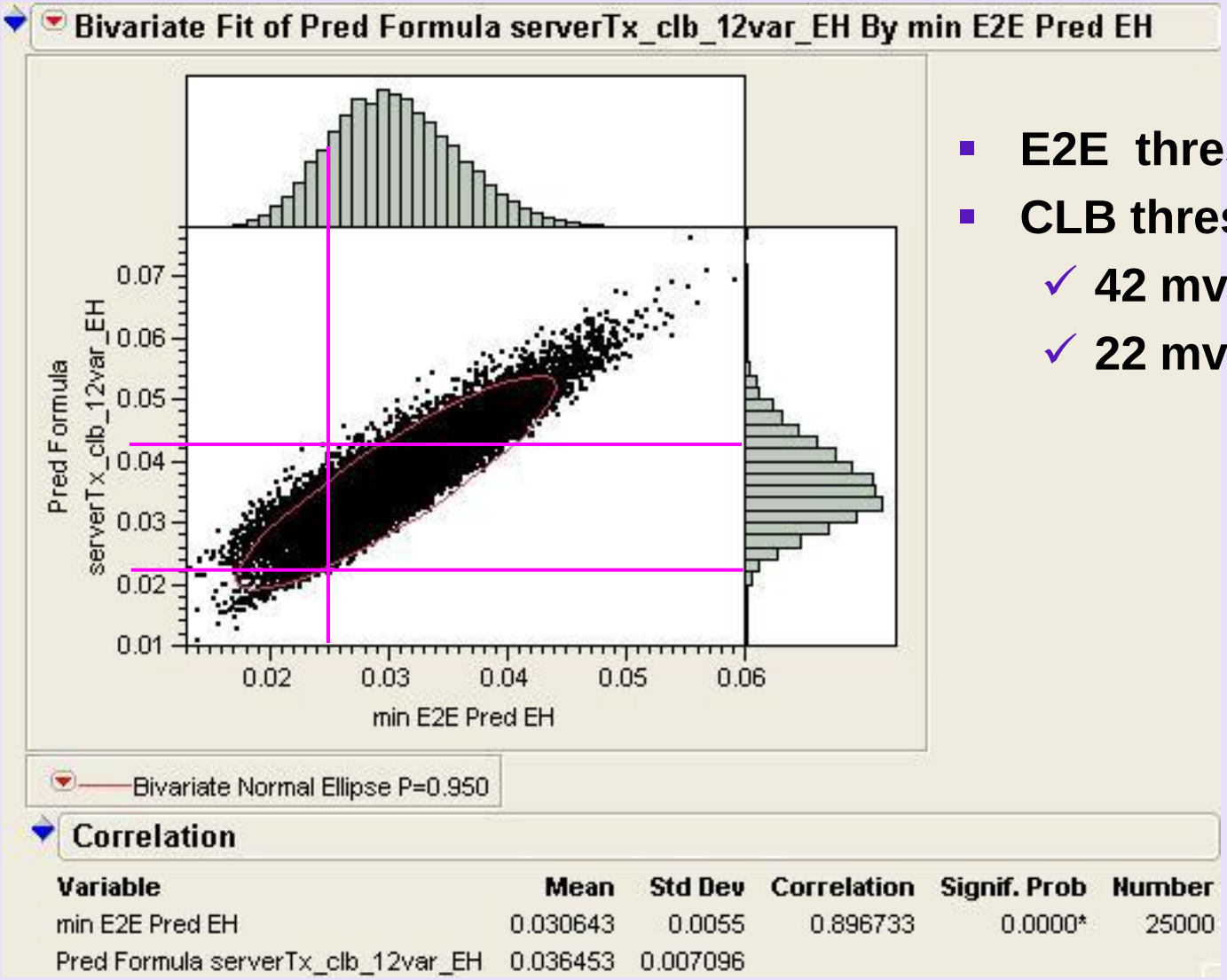
Client Tx E2E to CLB Eye Height Correlation



- **E2E threshold at 25.0mV**
- **CLB threshold range**
  - ✓ **43 mv. No False Passes**
  - ✓ **27 mv. No False Failures**

Source: Intel Corporation

Server Tx E2E to CLB Eye Height Correlation



- E2E threshold at 25mV
- CLB threshold range
  - ✓ 42 mv. No False Passes
  - ✓ 22 mv. No False Failures

Source: Intel Corporation

.9 TX Limits

- Test Channels
  - ✓ MB TX Test Channel
    - 4” 85 ohm trace + reference RX package
  - ✓ AIC TX Test Channel
    - 16” and 2 connectors + reference RX package
- CTLE + 1 Tap DFE reference Equalizer
- BER E-12 Limits (Same for AIC and MB)
  - ✓ 34 mV
  - ✓ .33 UI
- BER E-6 (Same for AIC and MB)
  - ✓ 46 mV
  - ✓ Informative – for simplified lab measurement use

8.0 GT/s TX EQ Presets

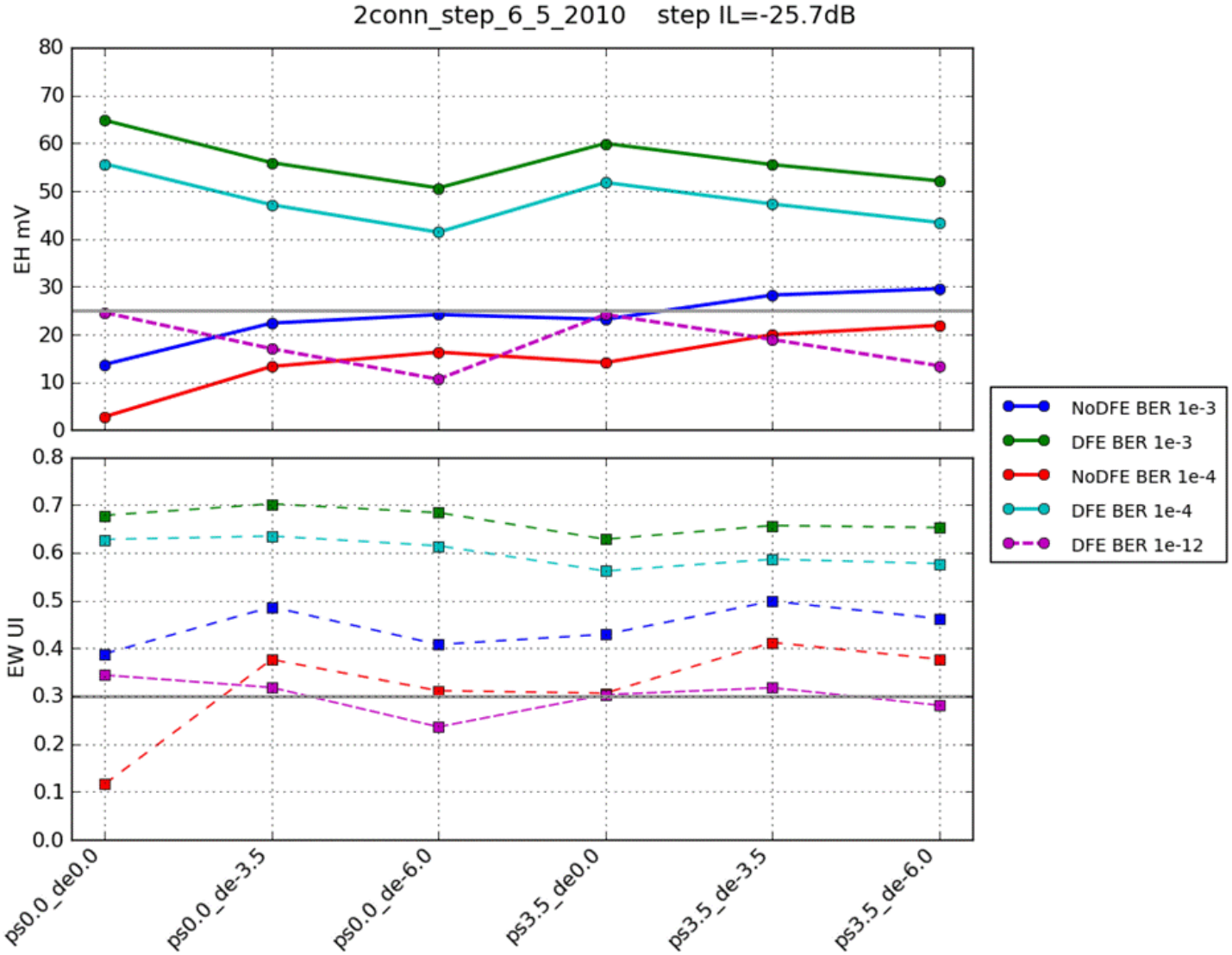
Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

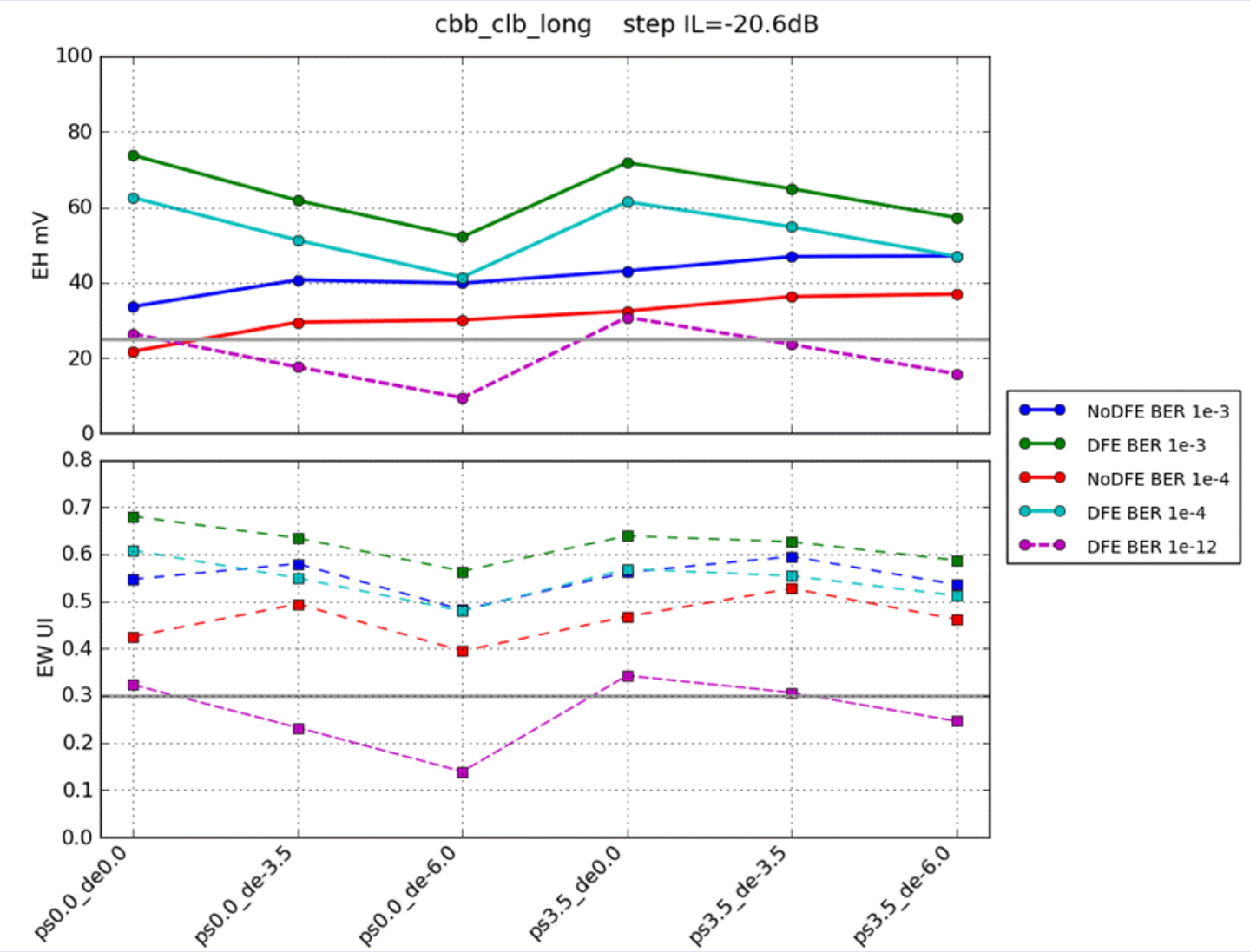
Notes:

1. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the two diagonal lines in Figure 4-45. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

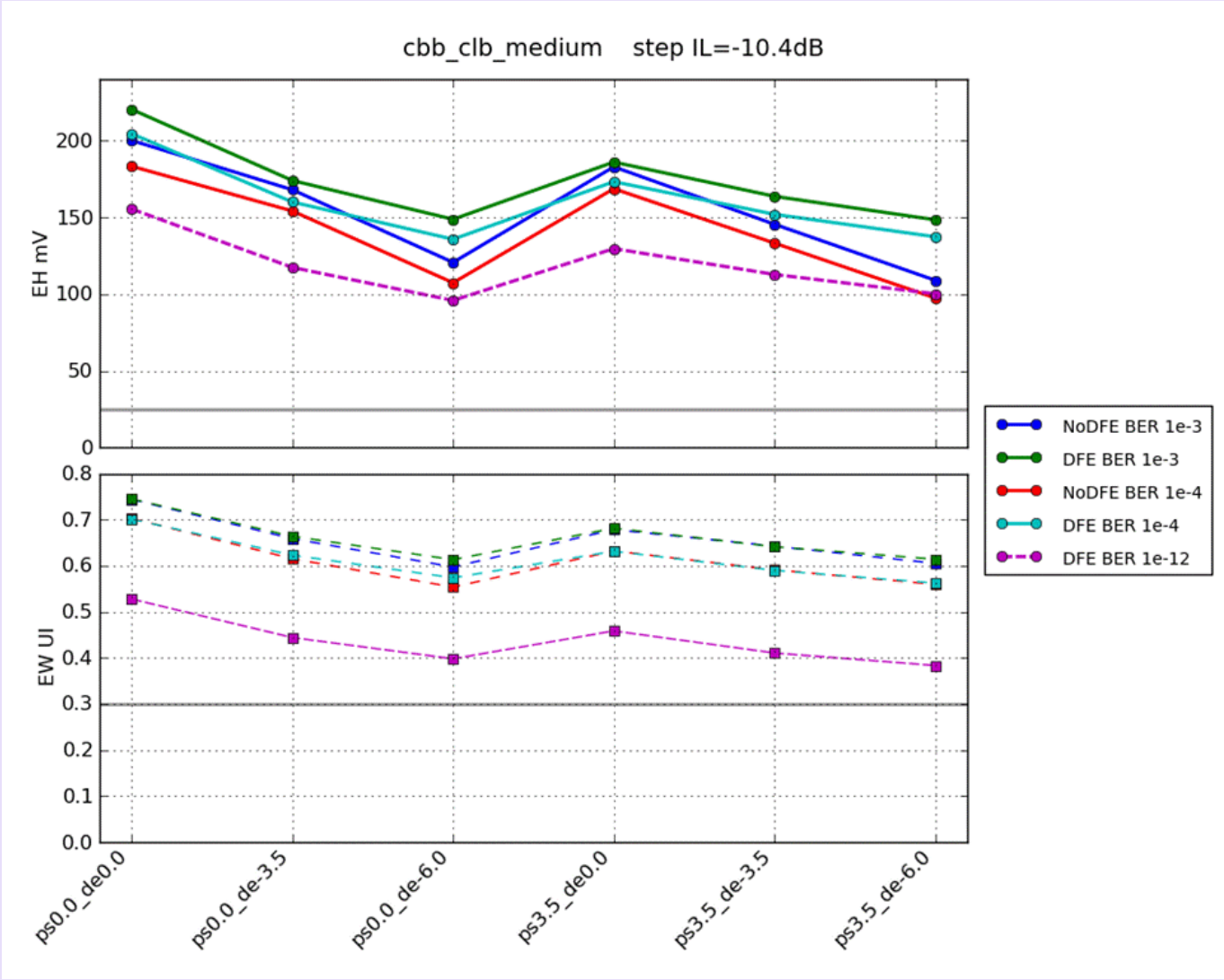
Seasim Simulation Results – Published Worst Case Server



Seasim Simulation Results 3.0 CLB/CBB Compliance Channel



Seasim Simulation Results 2.0 CLB/CBB Compliance Channel



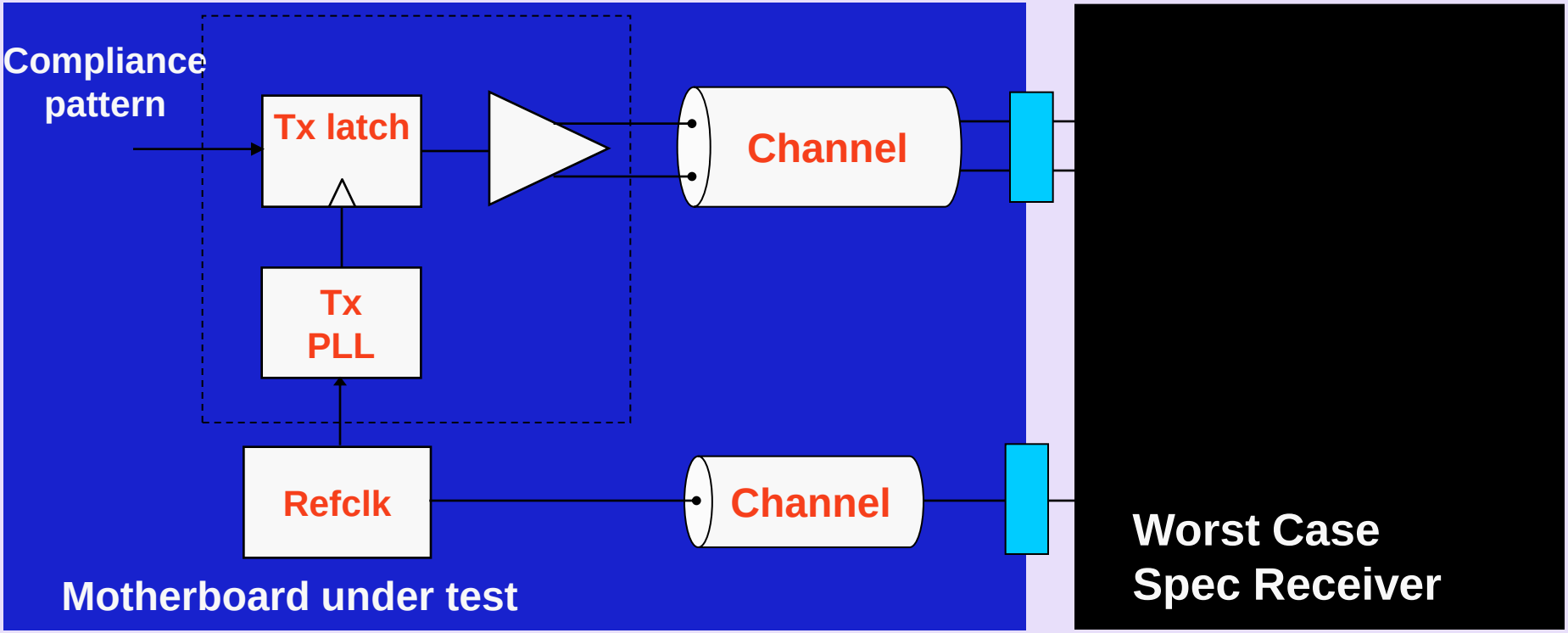
CEM TX Preset Selection

- CEM Specification
  - ✓ MB shall pick preset from following set
    - P1, P7, P8
  - ✓ MB shall use P7 or P8 if channel insertion loss is more than 12 dB at 4 Ghz
    - Measured through compliance pattern and CLB (64 ones and zeroes)
- CEM Compliance

✓ MB TX
- ✓ Measure channel loss with CLB and compliance patterns (64 ones/zeros)
- ✓ If > 12 dB then preset must be P7 or P8
- ✓ Else – preset must be P1, P7, P8

✓ Add-in Card RX
- ✓ Long channel (3.0 CLB/CBB)
  - Test for E-4 BER with P7 and P8
- ✓ Medium channel (2.0 CLB/CBB)
  - Test for E-4 BER with P1, P7, P8

Dual Port Concept

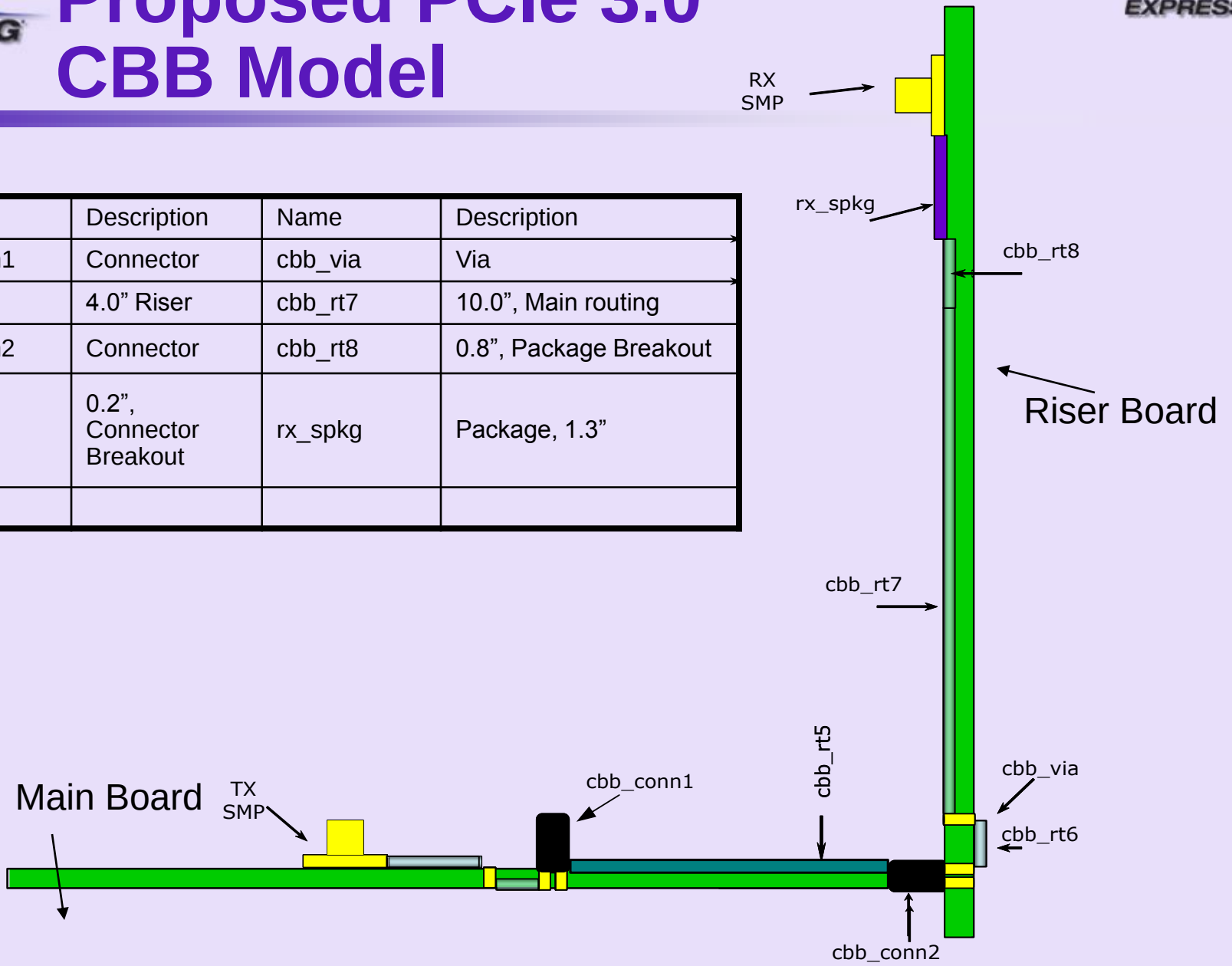


- How Does System Look With A Worst Case Spec Receiver?
  - ✓ Assume Common Clock Receiver
  - ✓ Assume worst case legal receiver PLL and add-in card delay
- Can test with/without SSC

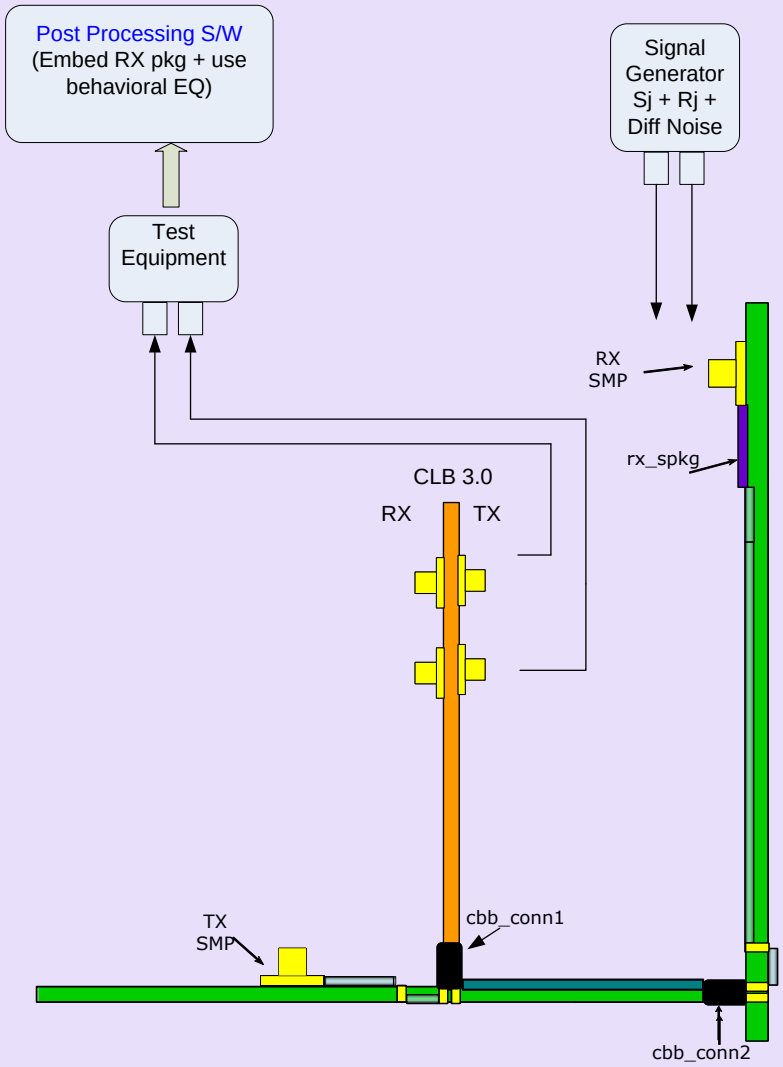
.9 Spec – Use dual port to remove any issue testing with real clock or SSC

Proposed PCIe 3.0 CBB Model

Name	Description	Name	Description
cbb_conn1	Connector	cbb_via	Via
cbb_rt5	4.0” Riser	cbb_rt7	10.0”, Main routing
cbb_conn2	Connector	cbb_rt8	0.8”, Package Breakout
cbb_rt6	0.2”, Connector Breakout	rx_spkg	Package, 1.3”

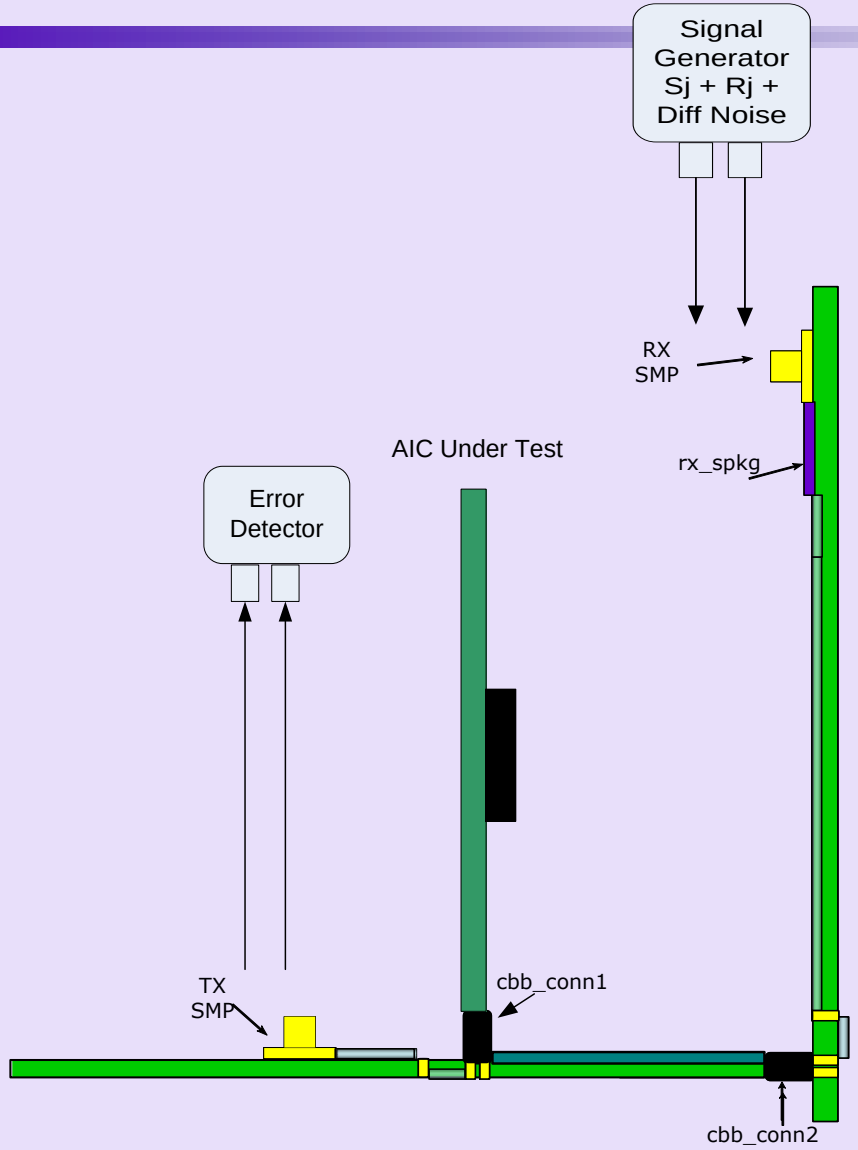


Proposed AIC RX Long Channel Test Calibration



- Calibration performed with optimal TX EQ for reference equalizer
- Calibration performed to MB TX EQ limits
  - ✓ Differential noise and Rj adjusted to match eye
  - ✓ 1.0 spec clarifies Rj value is just nominal starting value
- No AC common mode
  - ✓ CEM test simplification
- Separate short channel test with PCIe 2.0 CLB/CBB

Proposed AIC RX Long Channel Test



- Add-in card can request alternate TX EQ setting
  - ✓ Signal generator switches without recalibration
- If test setup (single lane in loopback) does not produce worst case crosstalk – must compensate
- Test performed with direct path to loopback

Link Equalization Feedback

- Standard RX test does not test the ability of the AIC to request TX EQ adjustments for the link partner if necessary for the receiver to achieve E-12
- Separate testing required to validate that receiver will work at E-12 if initial TX EQ choice is poor – using requests for the link partner to change TX EQ settings if necessary
- Test set-up and detailed methodology outside the scope of CEM specification

CEM 3.0 PCB Requirements

- PCB impedance 70-100 ohms
  - ✓ Tighter requirement likely for high loss (long channel) motherboards
- Limited vias and discontinuities
- PCB routing rotations to mitigate fibre weave impact
  - ✓ May only be necessary for longer/lossier channels

Power and Thermal Update

- Power management can be a challenge
  - ✓ Slot power limit messages not always used/followed
  - ✓ More high power options for add-in cards (150W, 300W)
- 75 Watt ECN
  - ✓ Allows all width add-in cards to consume up to 75W if allowed by the slot power limit message
- Power Budgeting Capability
  - ✓ Workgroup currently reviewing proposal to make capability required for any add-in card capable of consuming more power than default slot power maximum
- Thermal Guidelines
  - ✓ Workgroup discussing publishing additional thermal guidelines for systems and add-in cards when more than 75W is consumed

Mechanical Updates

- A variety of mechanical ECNs are posted for member review
  - ✓ Each will be reviewed separately through standard ECN review process
  - ✓ Plan is to include ECNs in final 3.0 draft
- ECNs are updates clarifications to general mechanical specifications and not specific to 8 GT/s
  - ✓ Reduce size of secondary side north edge trace free area
  - ✓ Clarify area north of edge finger as restricted height
  - ✓ Decouple card power class and slot width
  - ✓ Standardize 225/300 W north edge keepout for all cards
  - ✓ Formalize 1.5 kg mass limit for all cards
  - ✓ More . . . watch PCI-SIG website for ECN member review

Workgroup Accepted Mechanical ECN Change

Current ECN	Proposed Alternative
	

Member feedback during ECN review to relax consolidated North Edge Keep out

Allows a little more flexibility for base CEM (low power) add-in cards to meet ECN

Workgroup accepted. Revised ECNs posted for review soon.

Summary/Conclusions

- PCIe 3.0 CEM electrical requirements can be specified as a simple eye diagram measured with a standard test fixture without significant impact to target solution space
  - ✓ Eye mask differentiates end to end passing and failing cases well
- Power budgeting capability requirements under review
- Receiver Test Methodology
  - ✓ Separate tests for receiver capability and use of link equalization (if needed)
  - ✓ Long and short channel tests for Add-in Cards
- Same channel reach as for PCIe 2.0
  - ✓ Client: 14 inch, one connector
  - ✓ Server: 20 inch, two connectors
- For latest PCIe 3.0 specifications, visit www.pcisig.com
  - ✓ 1.0 CEM 3.0 with integrated mechanical ECN/errata available soon
  - ✓ .9 includes 150W and 300 W graphics specification content
- Several Mechanical ECN/Errata available for review now

Thank you for attending the PCIe Technology Seminar.

For more information please go to www.pcisig.com