PCIe® 2.0 Cards and Slots

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AMD

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Agenda

- 225/300 Watt High Power CEM Spec
  - ✓ Overview
  - ✓ System Volumetric
  - ✓ Connectors
  - ✓ Power Delivery
  - ✓ Card Keepout and Structure
  - ✓ Thermal and Acoustics
- CEM 3.0 Updates
  - ✓ Expected Changes
  - ✓ Connector Performance
  - ✓ Supported Topologies
  - ✓ Simulation Methodology
  - ✓ Key Tasks
- Summary

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225/300 Watt High Power CEM Spec 1.0

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High Power CEM Specification

- Support 225 W / 300 W high power requirements for add-in cards and systems
  - ✓ The 150W spec is no longer sufficient
- Standardize new power delivery connector and power-up sequencing scheme
- Define system boundary conditions for 225W/300W cards
  - ✓ Mechanical, thermal and acoustic
- Focus on the ATX form factor
- 1.0 spec released March 27th, 2008
  - ✓ http://www.pcisig.com/members/downloads/specifications/pciexpress/PCIe_225_300W_r1.0_27Mar08.pdf

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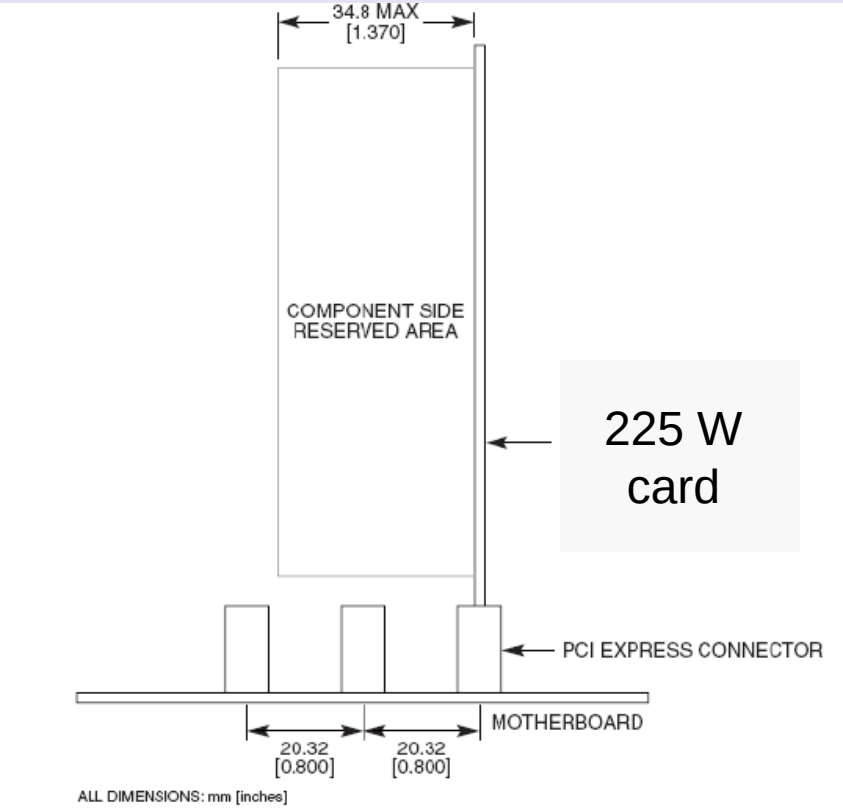
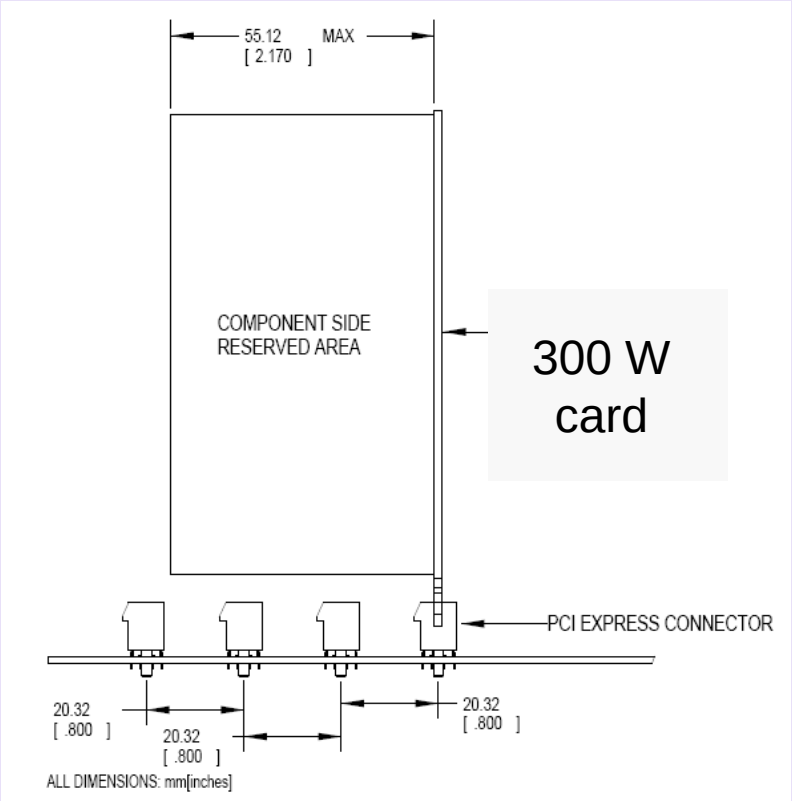
System Volumetric





(150W-225W] cards can occupy two slots

(225W-300W] cards may occupy three slots

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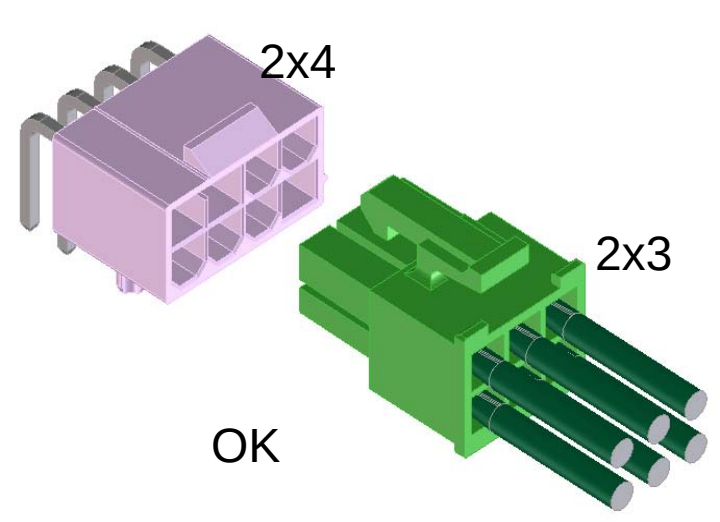
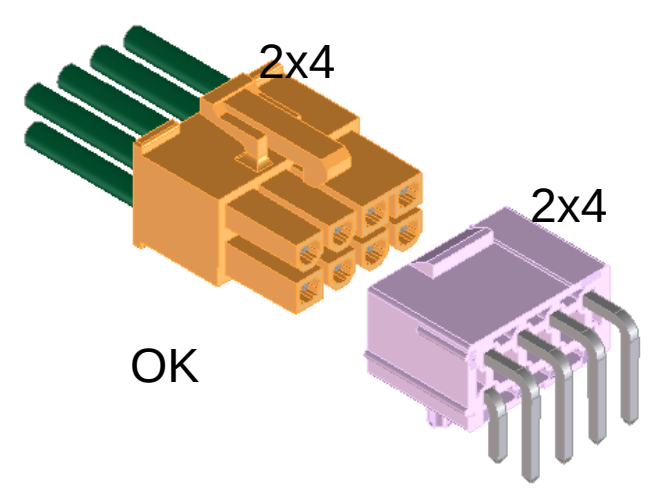
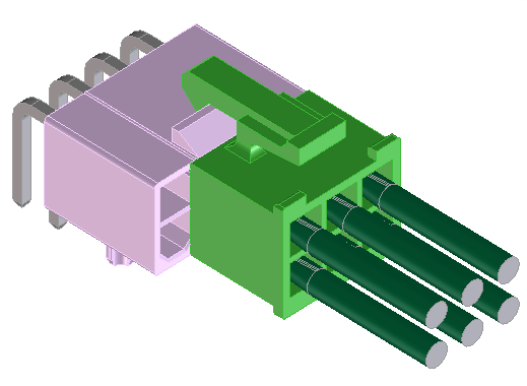
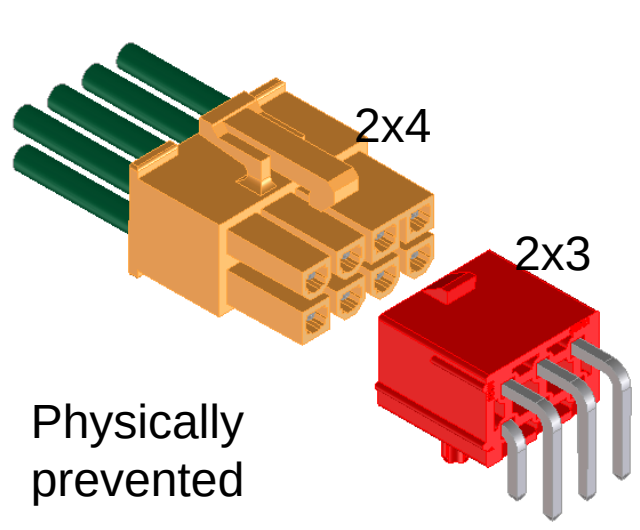
2x4 Connector

- Besides the 2x3 connector defined in the 150W Graphics Spec 1.0, a new 2x4 connector is defined for delivering power to the 225/300W cards









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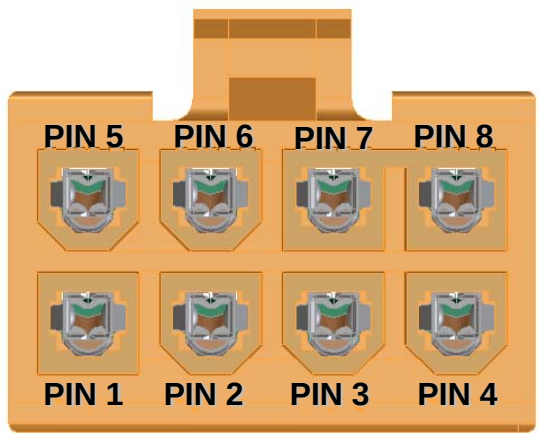
2x4 Connector Pinout



Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Sense1
5	Ground
6	Sense0
7	Ground
8	Ground

Sense1	Sense0	Comment
Ground	Ground	A 2x4 auxiliary power connector is plugged into the card. Card can draw up to 150W from the auxiliary power connector
Ground	Open	Reserved
Open	Ground	A 2x3 auxiliary power connector is plugged into the card. Card can only draw up to 75W from the auxiliary power connector
Open	Open	No auxiliary power connector is plugged in

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Delivering Power to Cards

- A 300W add-in card can receive power by the following methods:
  - ✓ 75W from x16 PCIe® connector plus 150W from a 2x4 connector plus 75W from a 2x3 connector.
  - ✓ 75W from x16 PCIe connector plus 75W from a first 2x3 connector, plus 75W from a second 2x3 connector, plus 75W from a third 2x3 connector.
    - – Note that this is not the preferred approach.
- A 225W add-in card can receive power by one of the following methods:
  - ✓ 75W from x16 PCIe connector plus 150W from a 2x4 connector.
  - ✓ 75W from x16 PCIe connector plus 75W from a 2x4 connector plus 75W from a 2x3 connector.
  - ✓ 75W from x16 connector plus 75W from a first 2x3 connector plus 75W from a second 2x3 connector.

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Additional Power Delivery Requirements

- The +12V delivered from the standard x16 edge connector and the additional +12V(s) delivered via the dedicated 2x3 and/or 2x4 auxiliary power connector(s) must be treated as coming from independent separate system power supply rails.
- The different +12V input potentials from different connectors must not be electrically shorted at any point on a PCI Express® 225W/300W add-in card.
- The power pins of a single 2x3 or 2x4 auxiliary power connector can be shorted together.
- No specific power sequencing between the slot, 2x3 and 2x4 connector power can be assumed. A PCI Express 225W/300W add-in card must handle all possible combinations.

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Power-up Sequencing

- At system power up, the permitted initial power draw depends on the auxiliary power connector configurations on the card and how many sense pins are detected
- After system reset is released and the PCI Express link is up, the card will receive the Slot_Power_Limit message.
  - ✓ If the Slot_Power_Limit is bigger than or equal to the permitted initial power draw, the card can then draw power up to the Slot_Power_Limit in any order from the PCI Express edge connector, the 2x3 connector (if exists) and the 2x4 connector (if exists), subject to and limited to the individual power ratings of the respective connectors.
  - ✓ If the Slot_Power_Limit is smaller than the permitted initial power draw, the card can ignore the Slot_Power_Limit message and continue draw the same amount of power as permitted at system power up time.

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Permitted Initial Power-300W

2x4 Sense0 Detected?	2x4 Sense1 Detected?	2x3 Sense Detected?	Power draw permitted at system power up
N	N	N	25W available from PCI Express edge connector
N	N	Y	Total of 75W is available: 25W available from PCI Express edge connector 50W available from 2x3 connector
Y	N	N	Total of 75W is available: 25W available from PCI Express edge connector 50W available from 2x4 connector
Y	N	Y	Total of 125W is available: 25W available from PCI Express edge connector 50W available from 2x3 connector 50W available from 2x4 connector
Y	Y	N	Total of 125W is available: 25W available from PCI Express edge connector 100W available from 2x4 connector
Y	Y	Y	Total of 175W is available: 25W available from PCI Express edge connector 100W available from 2x4 connector 50W available from 2x3 connector

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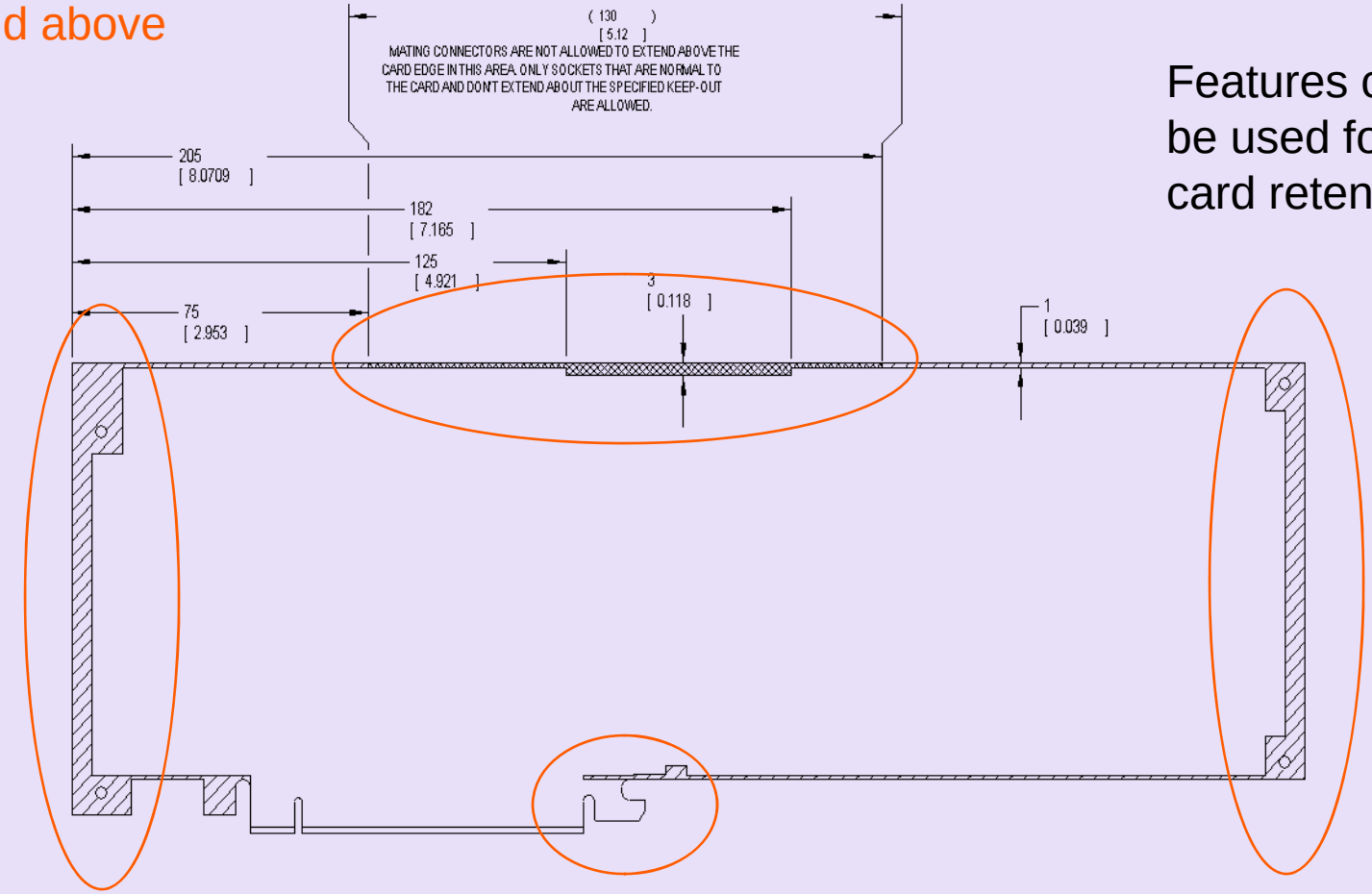
Card Keepout

Mated connectors are not allowed to extend above



Features can be used for card retention

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Other Mechanical Requirements

- Card total mass: <= 1.5 Kg
- All cards, including partial-length cards, shall have means of being extended to a full-length add-in card retainer as shown in CEM 2.0 Figure 6-6
- All cards, including partial-length cards, shall have means of being stiffened along their entire length from the rear bracket to the front card retainer

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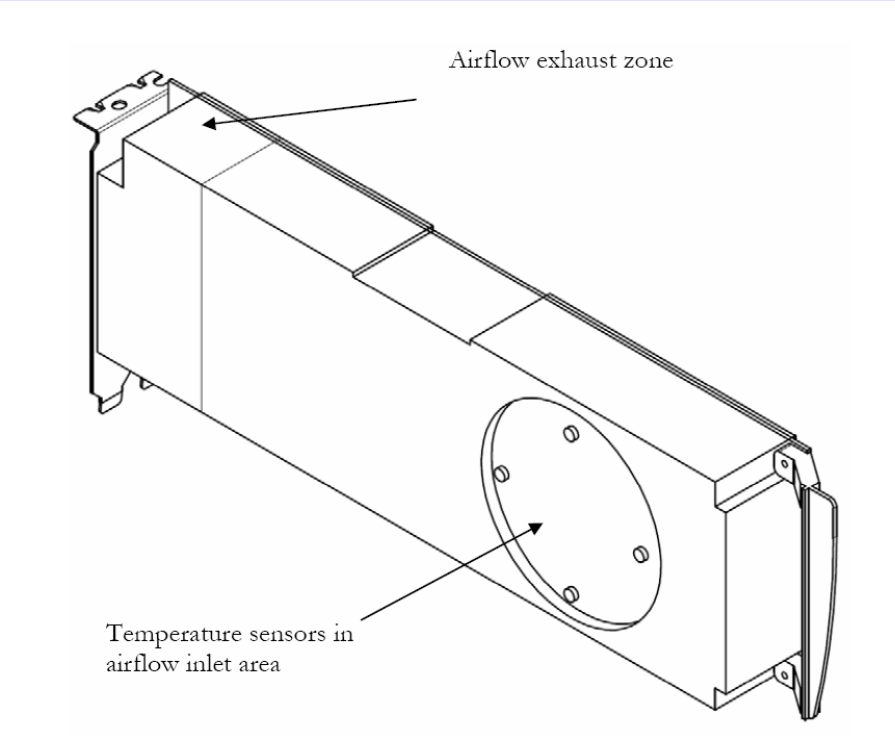
Thermal Boundary Condition

- Card inlet temperature:
  - ✓ 45°C for (150W- 225W] and (225W-300W] cards
  - ✓ In comparison, the 150W spec has an inlet of 55°C



- Inlet temp is the averaged temp at the card fan inlet
- Airflow exhaust should be within 2” of the rear bracket to avoid recirculation

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Thermal Measurements

- Open bench test done with fixtures in thermal chamber- adjust chamber temperature such that the card inlet temp is 45C

Characterization is performed under the "idle" and "full power" states:

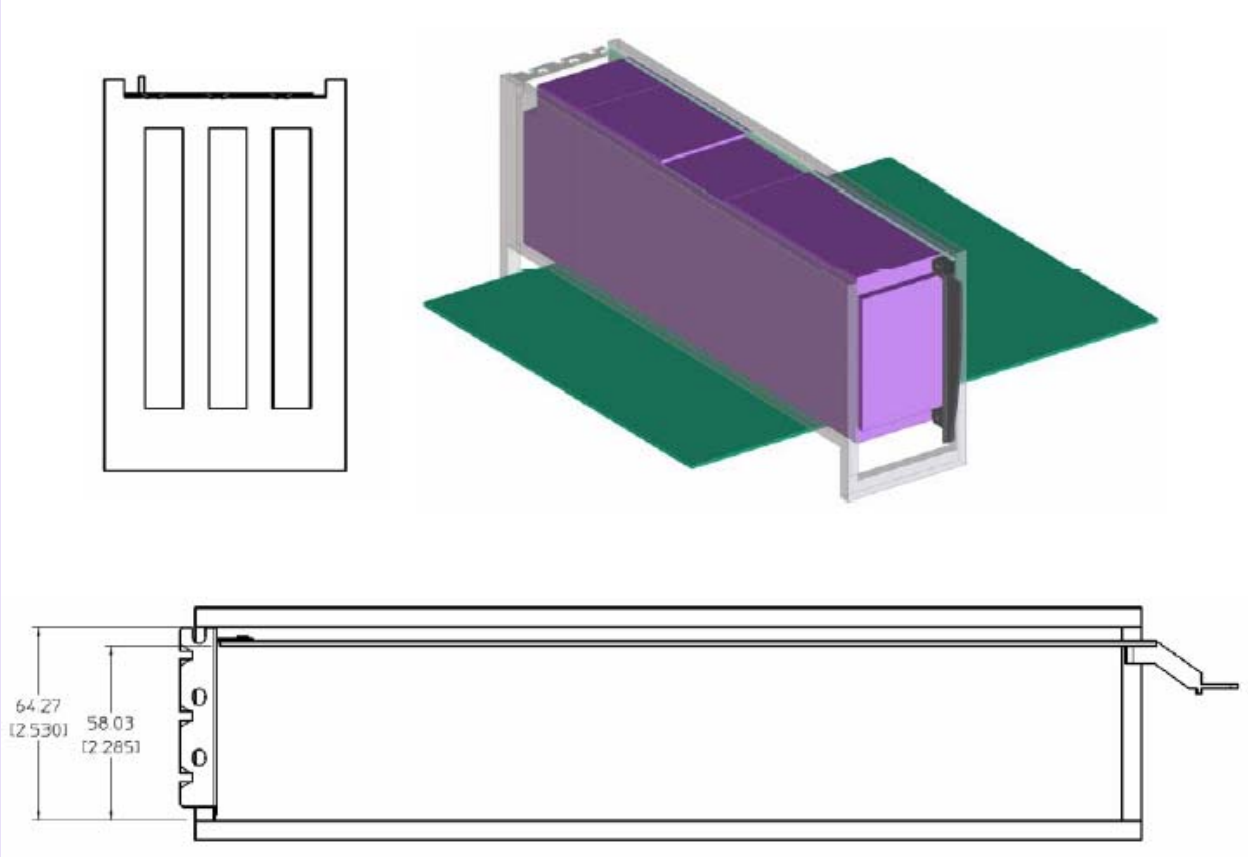
•Critical component temperatures

•Critical temperature limits

•Inlet temperature

•Exhaust temperature

•Fan speed



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Acoustic Management

- No acoustic requirement is specified
  - ✓ Market segments driven
- But metrology is specified for card vendors to report card acoustics
  - ✓ Consistent results
- Acoustic guidelines also provided

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Acoustic Measurement

- Measurement and test setup should be as defined in ISO 3744, Acoustics – Determination of Sound Power Levels of Noise Sources Using Sound Pressure – Engineering Method in an Essentially Free Field Over a Reflecting Plane.
- Place the card in the acoustic chamber by itself, in free air, without the system board or any other system components. The card under test should be suspended by some type of “bungee cords” to avoid any fixturing effect on acoustics.
- It is not necessary to fully power or operate the card. Instead, it is necessary to operate only the fan.
- Measure and/or calculate the following acoustic emissions at both the “idle” and “full power” fan speeds:
  - ✓ Sound pressure, *LPA*
  - ✓ Sound power, *LWA*
  - ✓ 1/3-octave acoustic spectral content

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Acoustic Guidelines

- The acoustic emissions should not include any prominent tones.
- Certain frequencies are more objectionable to humans than others.
- The card's fan(s) should be dynamically controlled to minimize noise over the complete range of expected operational and environmental conditions.
- The card's fan(s) should be controlled such that there are no abrupt changes or noticeable oscillations in acoustic levels or quality.
- The chassis should be designed so as to minimize coupling of vibrations and acoustic noise from the card to the chassis.
- The card should be designed so as to minimize coupling of vibrations from the card's fan to the card.

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PART II

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PCI Express 3.0 CEM Goals

- Backwards compatibility
- No required changes to the connectors, card form factors, or material.
- Minimal changes to the measurement methodologies from those used in the PCIe 1.x/2.0 specifications.
  - ✓ Use eye diagrams (jitter/voltage margin requirements). Minimize additional new requirements.
- *High Volume Manufacturing (HVM) statistical study used to validate if this achievable for 8GT/s*

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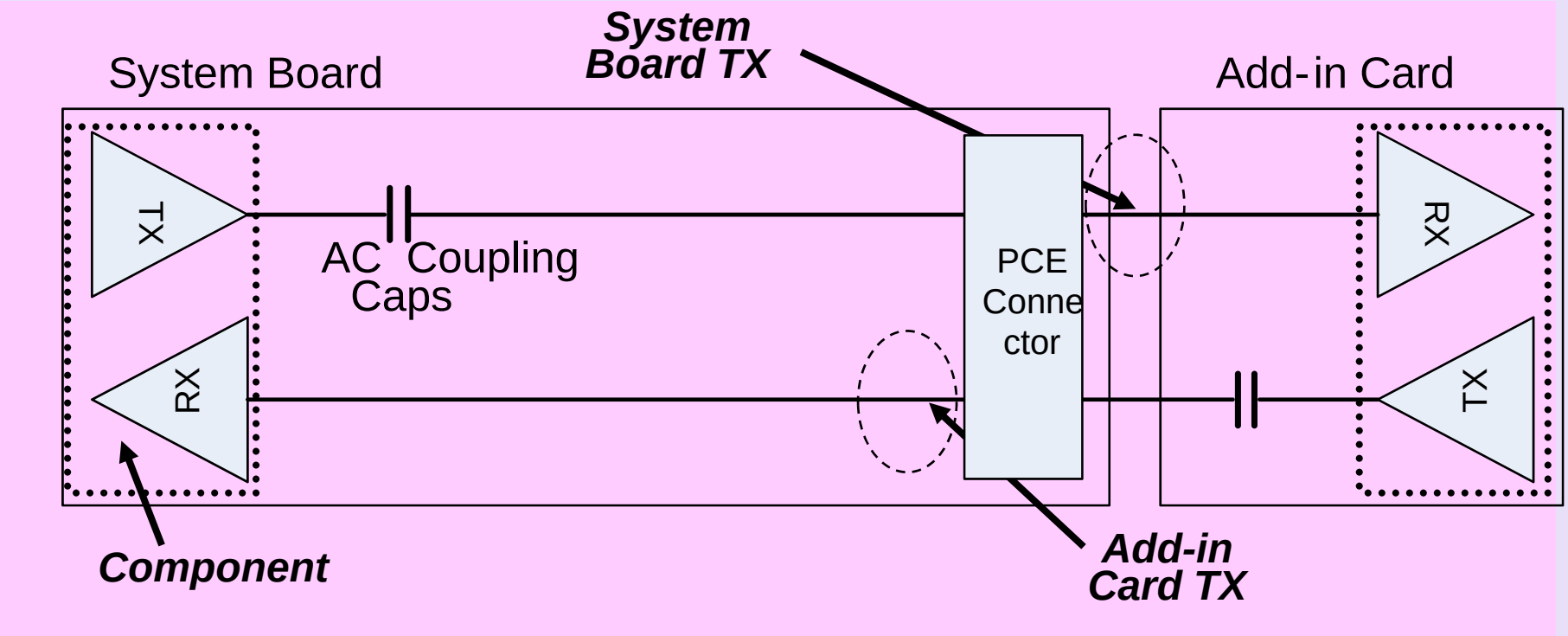
2.5-5GT/s CEM Spec – TX Path



CEM Spec Defines TX Requirements for Chip + Interconnect

No Separate TX Chip Or Interconnect Only Requirements.

Rx tolerance testing for 8GT/s under consideration

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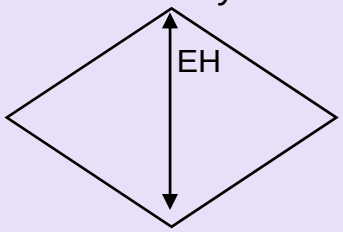
PCIe 3.0 CEM Methodology: End-End Simulation

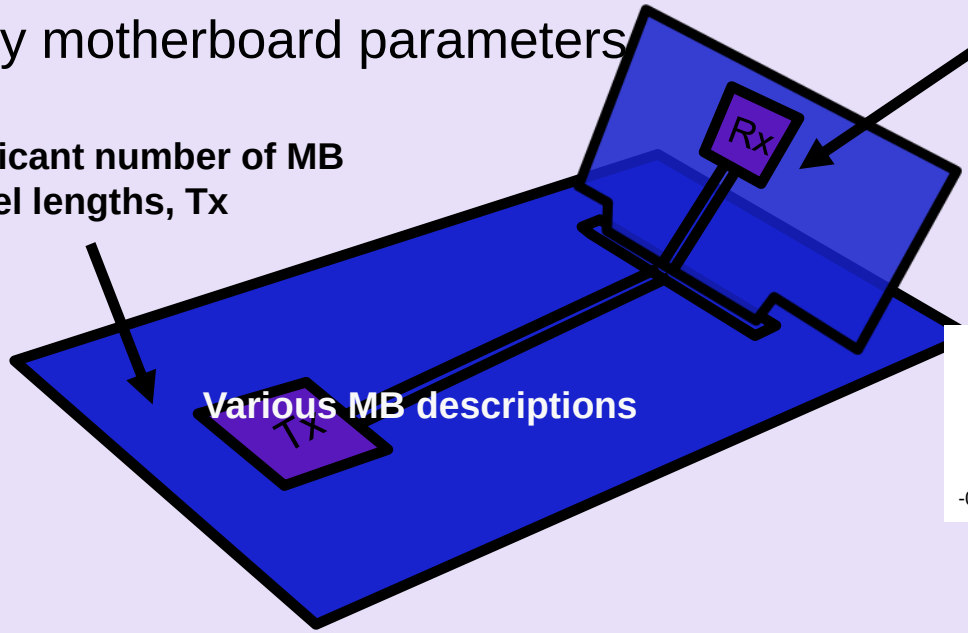
- Perform End-to-End (E2E) simulations
  - ✓ Use target 1 connector and 2 connector solutions
  - ✓ Eye height (EH) and eye width (EW) examined after first order CTLE at die pad
  - ✓ Statistical tools used for all simulations
- Fix motherboard (MB) parameters and determine pass/fail conditions across expected add-in card solution space
- Repeat with many motherboard parameters

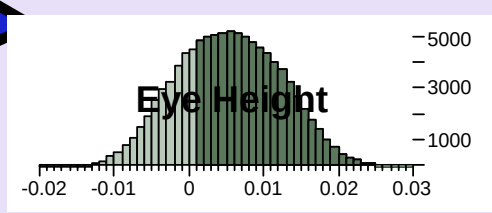
Sweep add-in card parameters over reasonable solution space

Pass/Fail Eye Mask



Create a statistically significant number of MB descriptions. (Vary channel lengths, Tx params, etc.)





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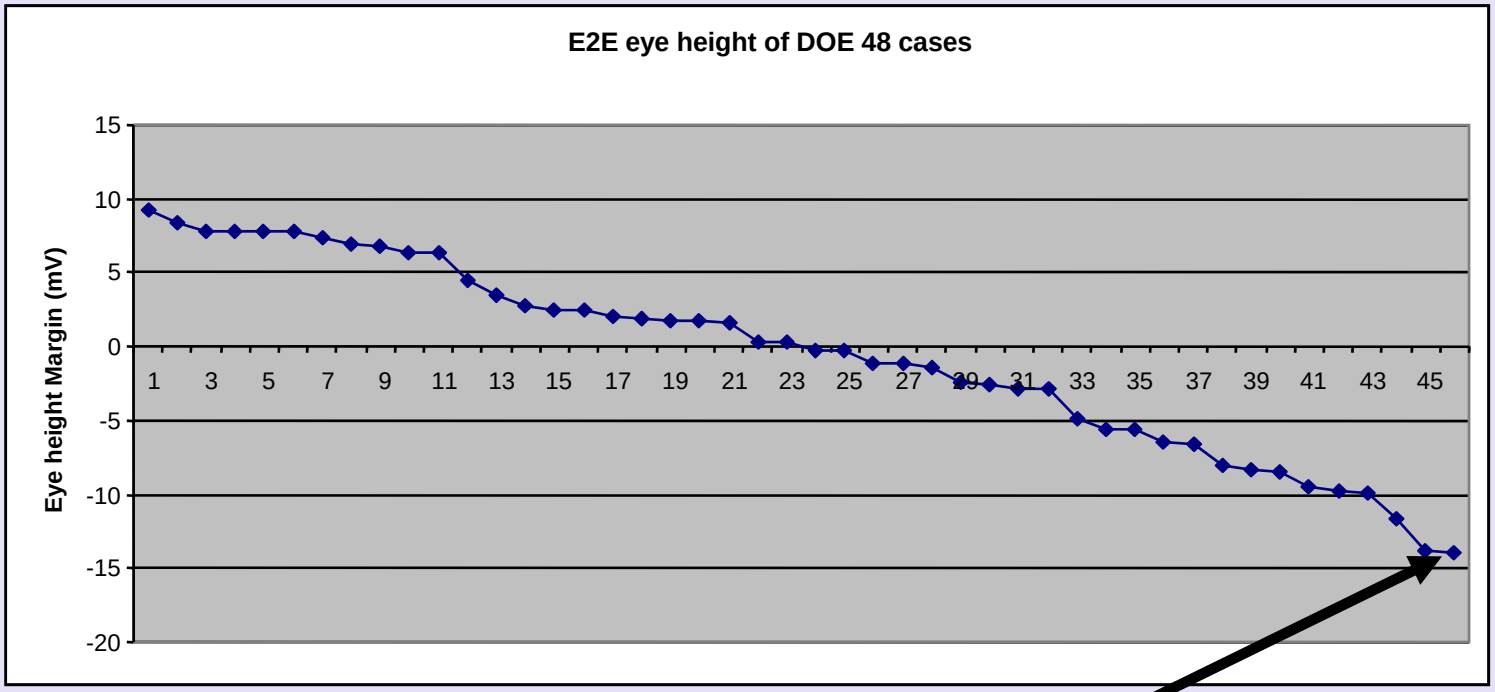
CEM Simulations – Worst Case Eye Height Margin



Source: Intel Corporation

- Worst case Add-in card (AIC) parameters for given motherboard (MB)
- Repeat simulation with different motherboards and find worst case for each
- THE ONLY POINT OF INTEREST FOR EACH SET OF MB PARAMETERS IS THE AIC PARAMETERS THAT GIVES WORST CASE

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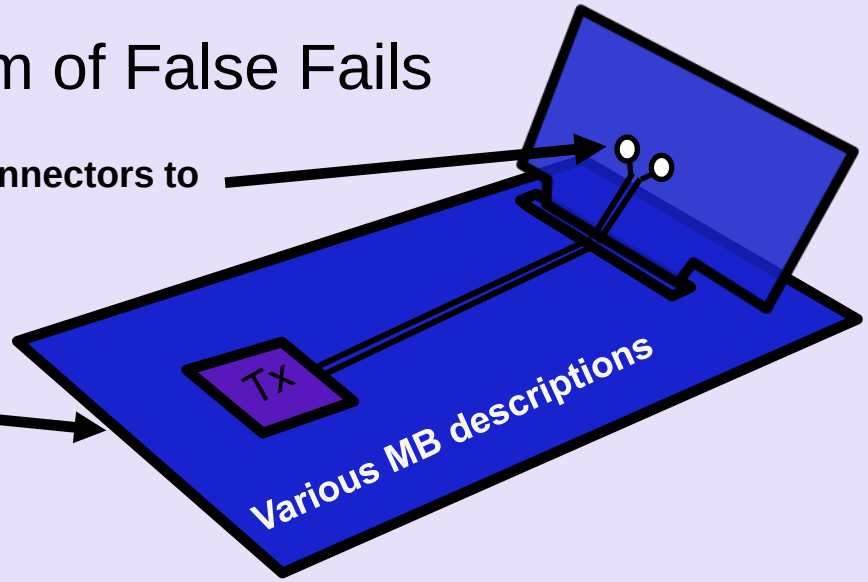
PCIe 3.0 Simulation Methodology Test Fixture Simulations

- Choose a test fixture
  - 2.0 CLB Test Fixture Used For Initial Investigation
  - No receiver equalization applied (eye is open)
- Repeat previous MB simulations with test fixture
  - Determine an eye mask at compliance Test Point
  - Find correlation between EH (and EW) at Test Point vs. end to end results
- No False Passes and a minimum of False Fails

Text fixture with SMP Connectors to 'scope (CLB 3.0)

Statistically significant number of MB Descriptions (same as E2E simulations)



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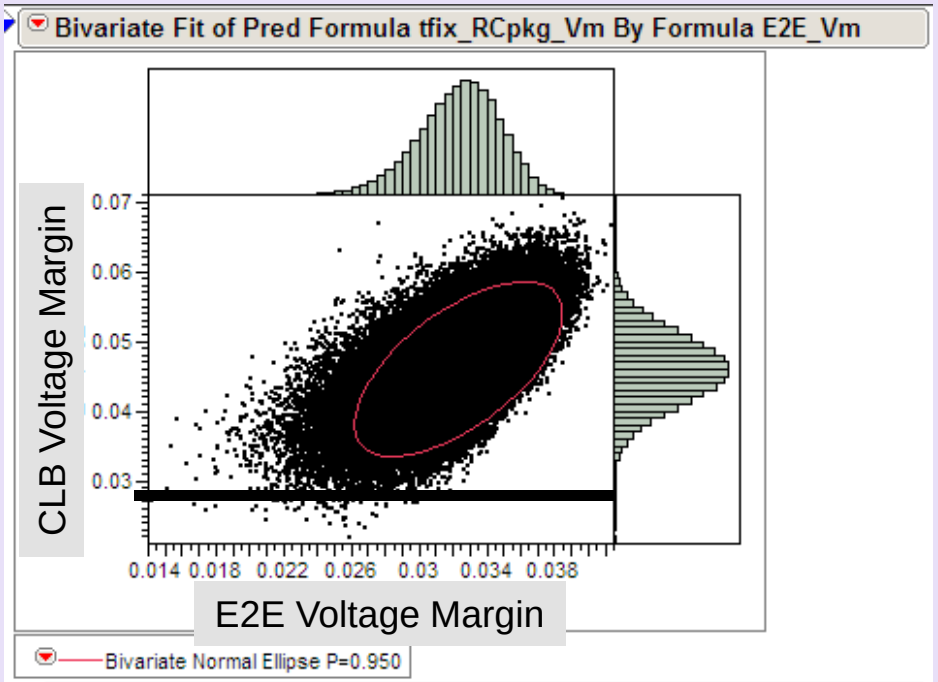
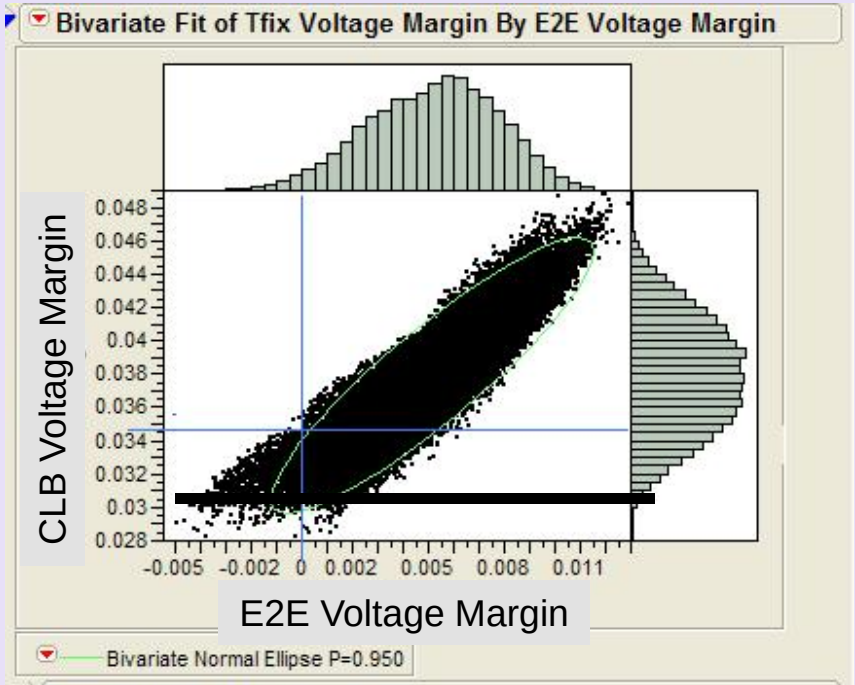
Package Model Test Fixture Performance With Product Design Targets



Correlation

Variable	Mean	Std Dev	Correlation	Signif. Prob	Number
Formula E2E_Vm	0.032314	0.002507	0.628765	0.0000*	250000
Pred Formula tfix_RCpkg_Vm	0.04603	0.005148			



Correlation

Variable	Mean	Std Dev	Correlation	Signif. Prob	Number
E2E Voltage Margin	0.00512	0.00262	0.904641	0.0000*	50000
Tfix Voltage Margin	0.037906	0.003378			

Client motherboard up to 11”

2 Connector Server up to 16”

Good correlation for lossy server channels, reflective client channels shows number of outliers

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Summary

- Using current CEM compliance methodology for 8GT/s looks feasible
  - ✓ More study required to better capture margin for client reflective channels
  - ✓ Tuning of layout on CBB and CLB to introduce a synthetic package model being considered
- Feasibility of CEM compliance Rx tolerance testing for 8GT/s being considered
  - ✓ Desire to validate Rx equalizer, CDR tracking bandwidth and input sensitivity

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