



SIGTM



Highlights of PCI-X Electrical Specification

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About This Presentation

- Goal is to introduce the main challenges facing the I/O buffer designer and the system H/W engineer when transitioning from Mode 1 to Mode 2 design/operation
 - ✓ Mode 1, Common Clock (CC) operation at 133MHz
 - ✓ Mode 2, PCI-X 266 = data rate of 266MHz (also called DDR operation)
 - ✓ Mode 2, PCI-X 533 = data rate of 533MHz (also called QDR operation)
- Provides in-depth look at some important topics of the spec.
- Explains the why and how of certain electrical parameters
- Provides some tips that can save you valuable design time
- Signal Integrity issues

Main Topics

- Transitioning from PCI-X Mode 1 to PCI-X Mode 2
 - ✓ 3.3V vs. 1.5 DC operating voltages
 - ✓ Mode 2 DC and AC spec highlights
 - ✓ Signal waveforms at receiver's pin and pad
- New jitter and timing specifications for PCI-X Mode 1 and Mode 2
 - ✓ Review of new jitter spec
 - ✓ implications on existing designs
 - ✓ Impact of jitter on Common Clock (CC) timing budgets
 - ✓ CC setup timing budget calculations
- I/O buffer design issues
 - ✓ Same buffer needs to operate with $V_{i/o} = 3.3V$ or $1.5V$
 - ✓ Buffer modeling issues for system level simulations
- Add-in card PCB layout considerations
- System board PCB layout considerations
- System level simulations

PCI-X Operating Voltages

- Mode 1: 3.3V, same as before.
- Mode 2: 1.5V, only AD, ECC, Strobe (80 signals).

Table 2-1: Driver and Receiver Categories

Category		Supply Voltage	Output Type	Input Terminator	Signals	Notes
1	Mode 1	3.3V	Totem pole	No	AD, C/BE#, PAR64/ECC[7], REQ64#/ECC[6], ECC[5::2], ACK64#/ECC[1], PAR/ECC[0]	1
	Mode 2	1.5V	Totem pole	Yes		2
2		3.3V	Totem pole	No	FRAME#, IRDY#, DEVSEL#, TRD Y#, STOP#, IDSEL, PERR#, LOCK#, REQ#, GNT#, RST#, CLK	3
3		3.3V	Open drain	No	SERR#, INTx#	4
4		See PCI 2.3	See PCI 2.3	See PCI 2.3	M66EN, PRSNT[1::2]#, TCK, TDI, TDO, TMS, TRST#, SMBCLK, SMBDAT	5
5		See PCI PM 1.1	See PCI PM 1.1	See PCI PM 1.1	PME#	
6		na	na	na	PCIXCAP, MODE2	6

2. In Mode 2, these signals use source-synchronous timing for data phases of source-synchronous transactions

Selecting I/O buffer Electrical Behavior

- Mode 1 or Mode 2 I/O buffer selection
 - ✓ Sensing the magnitude of $V_{i/o}$
 - Change mode of operation while $RST\#$ is asserted
 - If $V_{i/o}$ in 3.3V range select I/O buffers for Mode 1 or conventional PCI
 - If $V_{i/o}$ in 1.5V range select I/O buffers for Mode 2

1.5V Signaling DC Specs

- 5% $V_{I/O}$ tolerance
- 1% V_{ref} tolerance
- Output levels specified relative to $V_{I/O}$
- Input levels specified relative to V_{ref}
- Z_{term}
 - ✓ on-die
 - ✓ $57\Omega \pm 10\%$ in critical range
 - ✓ $57\Omega \pm 20\%$ elsewhere
- V_{term}
 - ✓ on die or off die
 - ✓ 5% tolerance

Table 2-12

Sym	Parameter	Condition	Category 1 PCI-X		Units
			Min	Max	
$V_{I/O}$	I/O Supply Voltage		1.425	1.575	V
V_{ref}	Input Reference Voltage		$0.49V_{I/O}$	$0.51V_{I/O}$	V
V_{ih}	Input High Voltage		$V_{ref} + 0.100$	$V_{I/O} + 0.500$	V
V_{il}	Input Low Voltage		-0.5	$V_{ref} - 0.100$	V
I_{il}	Input Leakage Current	$0 < V_{in} < V_{I/O}$		± 10	μA
V_{oh}	Output High Voltage		$V_{I/O} - 0.2$	$V_{I/O} - 0.1$	V
V_{ol}	Output Low Voltage		0.1	0.2	V
C_{pad}	Input Pad Capacitance			4.0	pF
Z_{term}	Equivalent Input Impedance	$V_{ol}(AC)(max) < V_{in} < V_{oh}(AC)(min)$	51	63	Ω
		$0 < V_{in} < V_{I/O}$	45	68	Ω
V_{term}	Equivalent Input Termination Voltage	Open-circuit voltage at input pin	$0.45V_{I/O}$	$0.55V_{I/O}$	V
Z_{pack}	Device Package Characteristic Impedance		46	63	Ω

✦ $\Delta V_{io} = 1\%$ (DC variations between 2 devices, measured at pins while bus is quiescent) per table 2-41.

Category 1 Driver Specification

AC I/O Buffer Specifications at 266MHz

Tor Output Rise Time min: 300 max: 750*

Tof Output Fall Time min: 300 max: 750*

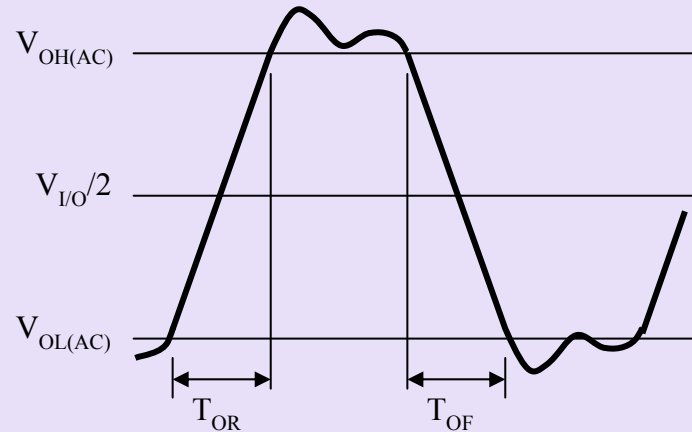
AC I/O Buffer Specifications at 533MHz (goal)

Tor Output Rise Time min: 300 max: 500

Tof Output Fall Time min: 300 max: 500

Voh(AC) Output High Voltage, Switching $V_{I/O}/2 + 0.45 \text{ V}$

Vol(AC) Output Low Voltage, Switching $V_{I/O}/2 - 0.45 \text{ V}$



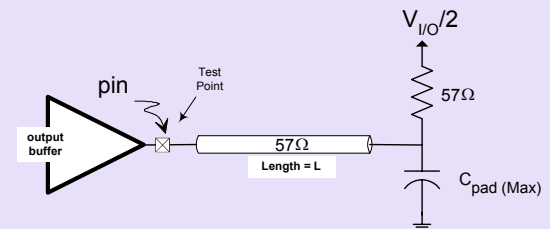
900mv voltage swing

- Tor, Tof are measured at the **device pin** into a test load (57R to $V_{I/O}/2$)
- Output rise/fall times can be slower than the specified max values above at the expense of *Data Valid Before and After Strokes* parameters. See derating table 2-16

DC I/O Buffer Specifications

Voh Output High Voltage min: $V_{I/O}-0.2 = 1.225\text{V}$; max: $V_{I/O}-0.1 = 1.475\text{V}$

Vol Output Low Voltage min: **0.1V**; max: **0.2V**



Note: The length of the transmission line, L, must be selected such that the reflection from the load does not interfere with the measurement at the test point.

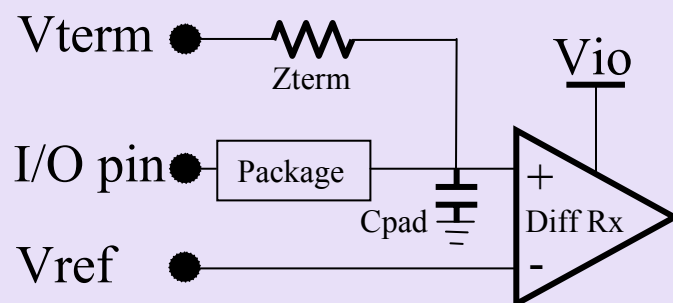
AC Test Load Spec

Receiver DC Specs

- **Zterm**
 - ✓ $57\Omega \pm 10\%$ between $V_{ol}(ac_max)$ and $V_{oh}(ac_min)$
 - ✓ $57\Omega \pm 20\%$ elsewhere
- **Vterm = $V_{I/O}/2 \pm 5\%$**
- **Current through 80 pins: $(V_{term} - V_{ol}(dc_min))/Z_{term} * 80pins$**
 $= (0.75-0.1)/57*80 = 0.65/57*80 = \mathbf{0.9A}$ (nominal values)

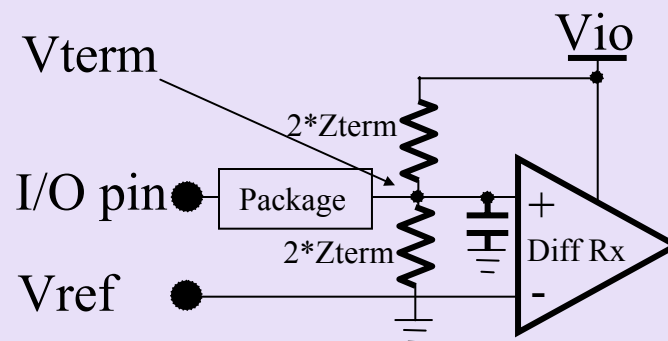
External Vterm

- Less $V_{I/O}$ power pins
- Requires Vterm pins
- Requires external supply
- Slightly less current consumption



Internal Vterm

- More $V_{I/O}$ power pins
- No external Vterm pins
- Simpler board design
 - Same supply voltage pins
- Slightly more current consumption



1.5V Signaling, AC Spec

Table 2-13: 1.5V AC Specification

Symbol	Parameter		Min	Max	Unit	Note
Power Supplies						
VI/O(AC)	I/O Supply Voltage Noise		-75	75	mV	1
Vref(AC)	Input Reference Voltage Noise		-30	30	mV	2
Vterm(AC)	Terminator Voltage Noise	At package pin	-75	75	mV	3
		At die pad	-75	75	mV	4
I/O Voltage Levels						
Vih(AC)	Input High Voltage, Switching	At die pad	Vref + 0.200	VI/O + 0.650	V	
Vil(AC)	Input Low Voltage, Switching	At die pad	-0.650	Vref - 0.200	V	
Voh(AC)	Output High Voltage, Switching		VI/O / 2 + 0.45		V	5
Vol(AC)	Output Low Voltage, Switching		VI/O / 2 - 0.45		V	5
Rise and Fall Times						
Tir	Input Rise Time	At die pad	70	610	ps	6
Tif	Input Fall Time	At die pad	70	610	ps	7
slewirf	Instantaneous Input Rise and Fall Slew Rate	At die pad		5.0	V/ns	16
Tor	Output Rise Time	PCI-X 266	300	See Table 2-16	ps	5, 9
		PCI-X 533	300	500		
Tof	Output Fall Time	PCI-X 266	300	See Table 2-16	ps	5, 10
		PCI-X 533	300	500		
ΔTorf	Output Rise and Fall Matching Deviation	PCI-X 266	See Table 2-16	See Table 2-16	ps	11
		PCI-X 533	-100	100		
sleworf	Instantaneous Output Rise and Fall Slew Rate			4.0	V/ns	8, 17

$V_{I/O(AC)}$ spec limits noise from device *onto* dc supply. Must have sufficient on-die and off-die decoupling

$V_{ih(AC)}, V_{il(AC)} = V_{ref} \pm 200\text{mv}$ at die *pad*

Tight output rise/fall time requires slew rate control

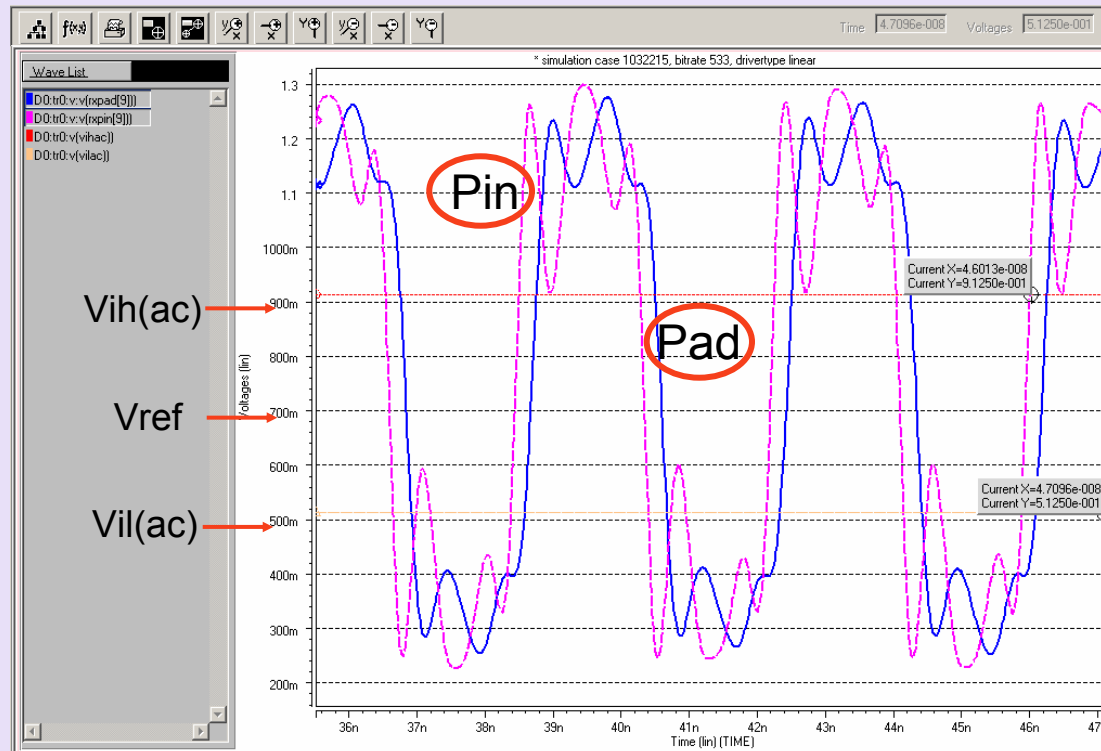
Rise/fall time matching specs required within source-sync group

No current-voltage (IV) tables

Read all table's notes and make sure you understand them

Waveforms at Receiver Pin, Pad

- Spec requires clean (monotonic) waveform at Rx pad
- Waveforms at pin and pad are not the same
- Ringback at pin will not show up at pad
- See Appendix D for detailed discussion (signal integrity issues, measurements at pin)





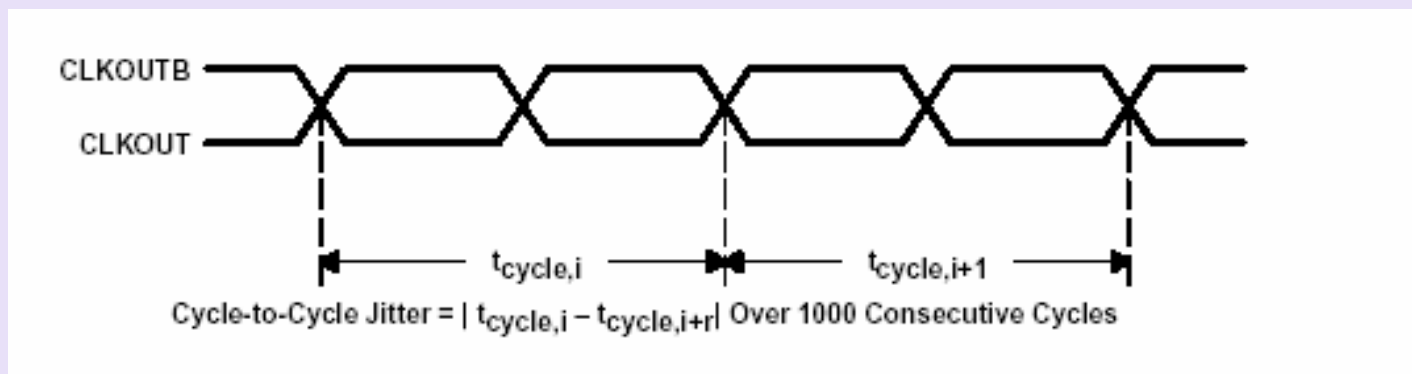
New Jitter Specification for Conventional PCI, PCI-X Mode 1 and Mode 2



Cycle-to-Cycle vs. Peak-to-Peak Jitter

■ **Cycle-to-cycle jitter** = $|T_{\text{cycle},i} - T_{\text{cycle},i+1}|$

✓ JEDEC's JESD65-A definition: *The variation in cycle time of a signal between adjacent cycles, over a random (i.e., not synchronous to the signal) sample of adjacent cycle pairs.*



■ **Peak-to-peak jitter (JEDEC):** *The deviation in cycle time of a signal with respect to the ideal period over a random (i.e., not synchronous to the signal) sample of cycles.*

See appendix C.5 for in-depth discussion about jitter and its impact on device timing

Jitter in Conventional PCI, PCI-X Rev 1.0 Specs

- Previous PCI spec did not adequately address clock jitter
- Only upper clock frequency limit was specified

PCI-X rev 1.0

Table 9-4: Clock Specifications, Mode 1

Sym	Parameter	PCI-X 133		PCI-X 66		Conv. PCI 66 (ref)		Conv. PCI 33 (ref)		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
T _{cyc}	CLK Cycle Time	7.5	20	15	20	15	30	30	∞	ns	1,3,4
T _{high}	CLK High Time	3		6		6		11		ns	4
T _{low}	CLK Low Time	3		6		6		11		ns	4
-	CLK Slew Rate	1.5	4	1.5	4	1.5	4	1	4	V/ns	2,4

Notes:

- For clock frequencies above 33 MHz, the clock frequency may not change beyond the spread-spectrum limits except while RST# is asserted.
- This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 9-5.
- The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
- All PCI-X 133 devices must also be capable of operating in PCI-X 66. All PCI-X devices must be capable of operating in conventional PCI 33 mode and optionally are capable of conventional PCI 66 mode.

Problems:

- ✓ No limit on jitter
 - Is 400ps of jitter acceptable?
- ✓ In order to comply with spec the nom operating frequency has to be lower
- ✓ Any Mode 1 system running at nom 133MHz is in 'technical violation'

Class 1 CC Jitter Spec for PCI-X Mode 1

■ Solution:

- ✓ Acknowledge existing industry practice
- ✓ Define 'Clock jitter class 1' for existing PCI-X rev 1.0 spec
- ✓ All existing Mode 1 systems are compliant with Class 1 clock jitter

New in rev 2.0

Table 2-5: Clock Specifications, Mode 1

		PCI-X 133		PCI-X 66		Conv. PCI 66 (ref)		Conv. PCI 33 (ref)			
Sym	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Clock Jitter Class 1											5
T _{cyc}	CLK Cycle Time	7.5	20	15	20	15	30	30	∞	ns	1,3,4
T _{high}	CLK High Time	3		6		6		11		ns	4
T _{low}	CLK Low Time	3		6		6		11		ns	4

5. Support for this jitter class is required for all Mode 1 devices.

Conventional PCI and Mode 1, Class 2 CC Jitter Spec

- “Jitter class 2” allows for nominal period of the clock to be 30nS, 15nS, 10nS or 7.5nS
 - ✓ Limits period jitter to +/-125ps for Mode 1 (same as Mode 2)

Mode 1

Required →

Optional →

Table 2-5: Clock Specifications, Mode 1

		PCI-X 133		PCI-X 66		Conv. PCI 66 (ref)		Conv. PCI 33 (ref)				
Sym	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes	
Clock Jitter Class 1											5	
T _{cyc}	CLK Cycle Time	7.5	20	15	20	15	30	30	∞	ns	1,3,4	
T _{high}	CLK High Time	3		6		6		11		ns	4	
T _{low}	CLK Low Time	3		6		6		11		ns	4	
Clock Jitter Class 2											6	
T _{cyc}	CLK Cycle Time	Average	7.5	20	15	20	15	30	30	∞	ns	1,4,7
		Absolute minimum	7.375		14.8		14.8		29.7		ns	1,3,4
T _{high}	CLK High Time	2.5		5.5		5.5		10		ns	4	
T _{low}	CLK Low Time	2.5		5.5		5.5		10		ns	4	
<u>T_{jit}</u>	<u>CLK Period Jitter</u>	<u>125</u>	<u>-125</u>	<u>200</u>	<u>-200</u>	<u>200</u>	<u>-200</u>	<u>300</u>	<u>-300</u>	<u>ps</u>	<u>8</u>	

7. Average T_{cyc} is measured over any 1 μs period of time and must include all sources of clock variation.

8. Period jitter is the deviation between any single period of the clock, T_{cyc}, and the average period of the clock, T_{cyc}(average).

Mode 2 CC Jitter Spec

Mode 2

Table 2-6: Clock Specifications, Mode 2

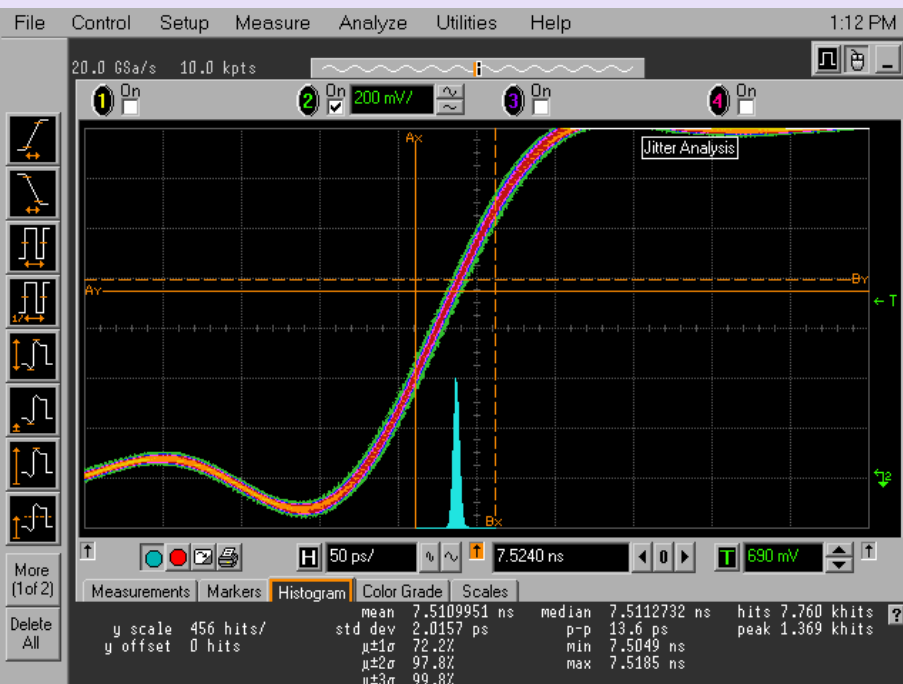
		PCI-X 533		PCI-X 266				
Sym	Parameter	Min	Max	Min	Max	Unit	Notes	
T _{cyc}	CLK Cycle Time	Average	7.5	20	7.5	20	ns	1, 2, 3
		Absolute Minimum	7.375		7.375		ns	1, 2, 4
T _{high}	CLK High Time	3		3		ns	2	
T _{low}	CLK Low Time	3		3		ns	2	
<u>T_{jit}</u>	<u>CLK Period Jitter</u>	<u>125</u>	<u>-125</u>	<u>125</u>	<u>-125</u>	<u>ps</u>	<u>6</u>	
Slew Rate								
-	CLK Slew Rate	1.5	4	1.5	4	V/ns	5	
Spread Spectrum Requirements								
f _{mod}	Modulation Frequency	30	33	30	33	kHz		
f _{spread}	Frequency Spread	-1	0	-1	0	%		

Notes:

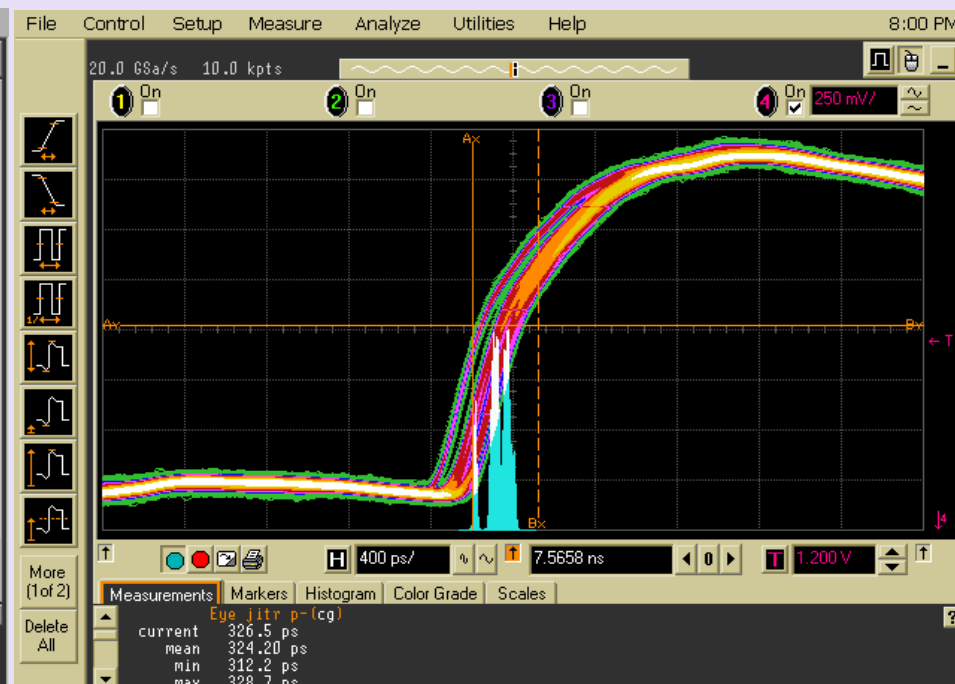
1. The clock frequency must not change beyond the spread-spectrum and jitter limits except while RST# is asserted.
2. All PCI-X 533 and 266 (Mode 2) devices must also be capable of operating in PCI-X 133 and 66 (Mode 1). All PCI-X devices (Mode 1 and Mode 2) must be capable of operating in conventional PCI 33 mode and optionally are capable of conventional PCI 66 mode.
3. Average T_{cyc} is measured over any 1 μs period of time and must include all sources of clock variation.
4. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
5. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 2-5.
6. Period jitter is the deviation between any single period of the clock, T_{cyc}, and the average period of the clock, T_{cyc}(average).

**Down
spread**

CC Jitter Measurements



Jitter measurement of a clock signal coming out of a signal generator.
Peak-to-peak jitter = 13.6ps



Jitter measurement of an off the shelf PCI/PCI-X clock driver device
Peak-to-peak jitter = 326.5ps (not suitable for Mode 2)

CC Timing Budget

- Timing budget calculations are typically done by system vendors to determine max and min trace length on system board.
- Setup time budget calculation limits max trace length – main concern
- Hold time budget determine min trace length.
- Add-in card trace length limits same as before, backward compatibility
 - See Slide 30
- PCI-X 1.0 setup time budget example for Mode 1 ($T_{val} = 3.8\text{ns}$)
calculated $T_{prop} = 2.0\text{ns}$, approx. 12". After subtracting add-in card trace length the max system board trace length = 8.5".
- Same system board trace length of 8.5" was used for mode 2 timing budget calculations
- Same T_{prop} in both cases, with system board max length = 8.5".

Mode 1 System, Setup Time Budget Example

Table 2-31: Setup Time Budget, Mode 1 Operation

Parameter	PCI-X 133 MHz	PCI-X 100 MHz	PCI-X 66 MHz	Conv PCI 66 MHz (ref)	Conv PCI 33 MHz (ref)	Units	Notes
Clock Jitter Class 1							
$T_{val}(\text{parity } 1)(\text{max})$ (ref)	3.8	3.8	3.8	6	11	ns	1
$T_{prop}(\text{max})$	2.0	4.5	9.0	5	10	ns	
$T_{crosstalk}(\text{max})$	0.2	0.2	0.2	-	-	ns	2
$T_{skew}(\text{max})$	0.3	0.3	0.3	1	2	ns	2
$T_{su}(\text{min})$ (ref)	1.2	1.2	1.7	3	7	ns	
$T_{cyc}(\text{min})$ (ref)	7.5	10.0	15.0	15	30	ns	-
Clock Jitter Class 2							
$T_{val}(\text{parity } 2)(\text{max})$ (ref)	<u>3.7</u>	<u>3.7</u>	<u>3.7</u>	<u>6</u>	<u>11</u>	<u>ns</u>	<u>1</u>
$T_{prop}(\text{max})$	<u>2.0</u>	<u>4.5</u>	<u>8.925</u>	<u>5</u>	<u>10</u>	<u>ns</u>	
$T_{crosstalk}(\text{max})$	<u>0.2</u>	<u>0.2</u>	<u>0.2</u>	<u>-</u>	<u>-</u>	<u>ns</u>	<u>2</u>
$T_{skew}(\text{max})$	<u>0.275</u>	<u>0.275</u>	<u>0.275</u>	<u>0.8</u>	<u>1.7</u>	<u>ns</u>	<u>2</u>
$T_{su}(\text{min})$ (ref)	<u>1.2</u>	<u>1.2</u>	<u>1.7</u>	<u>3</u>	<u>7</u>	<u>ns</u>	
$T_{cyc}(\text{absolute min})$ (ref)	<u>7.375</u>	<u>9.875</u>	<u>14.8</u>	<u>14.8</u>	<u>29.7</u>	<u>ns</u>	

Note: $T_{crosstalk}(\text{max})$ and $T_{skew}(\text{max})$ used to be lumped together in PCI-X 1.0 spec as 0.5ns

- No changes to “class 1 jitter”
- T_{prop} same in both cases, with system board max length = 8.5”.
- “Class 2 jitter” requires tighter spec to meet $T_{cyc} = 7.375\text{ns}$
 - ✓ T_{val} is smaller by 100ps
 - ✓ $T_{crosstalk}(\text{max})$ allocates 200ps for CC crosstalk
 - ✓ T_{skew} is smaller by 25ps

Mode 2 System, CC Setup Time Budget

Common-Clock Setup Time Budget, Mode 2 Operation

	CLK Frequency						
	1.5V Signaling			3.3V Signaling			
Parameter	133 MHz	100 MHz	66 MHz	133 MHz	100 MHz	66 MHz	Units
T _{val} (max) (ref)	<u>3.5</u>	<u>3.5</u>	<u>3.5</u>	<u>3.5</u>	<u>3.5</u>	<u>3.5</u>	ns
T _{prop} (max)	2.2	4.7	<u>9.125</u>	2.2	4.7	<u>9.125</u>	ns
T _{crosstalk} (max)	0.2	0.2	0.2	0.2	0.2	0.2	ns
T _{skew} (max) (ref)	<u>0.275</u>	<u>0.275</u>	<u>0.275</u>	<u>0.275</u>	<u>0.275</u>	<u>0.275</u>	ns
T _{su} (min) (ref)	1.2	1.2	1.7	1.2	1.2	1.7	ns
T _{cyc} (<u>absolute min</u>) (ref)	<u>7.375</u>	<u>9.875</u>	<u>14.8</u>	<u>7.375</u>	<u>9.875</u>	<u>14.8</u>	ns

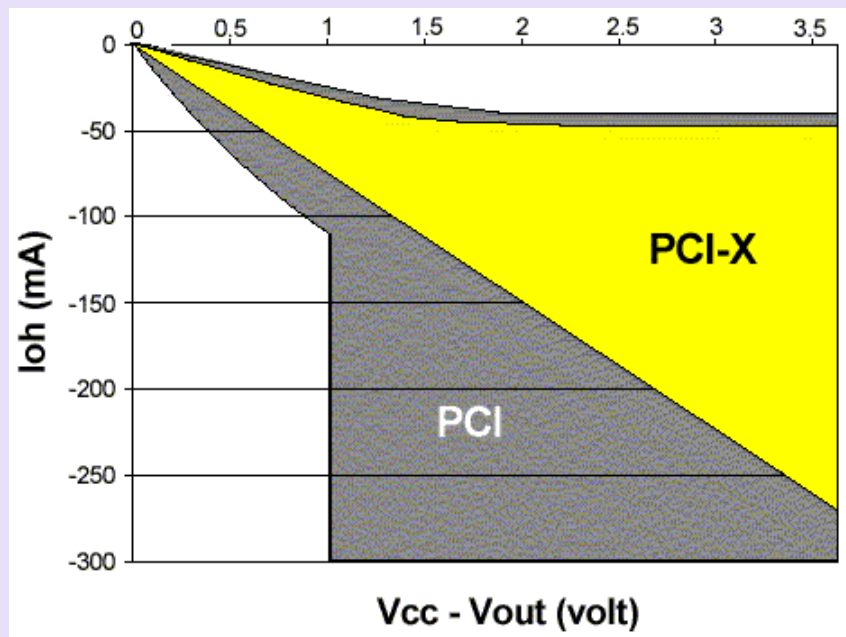
- T_{val} is now **3.5ns**
- $T_{prop} =$ **2.2ns**, longer by 200ps
 - ✓ Measurement conditions (load at output) are **not** the same as in Mode 1
- $T_{crosstalk(max)}$ allocates 200ps for crosstalk
 - ✓ Permitted spacing between signals, per layout spacing guidelines, will cause crosstalk which will affect propagation delay time
- Max system board trace length same as before, 8.5"
- Provisions for 200ps extra delay due to crosstalk
- Clock to clock skew of 275ps



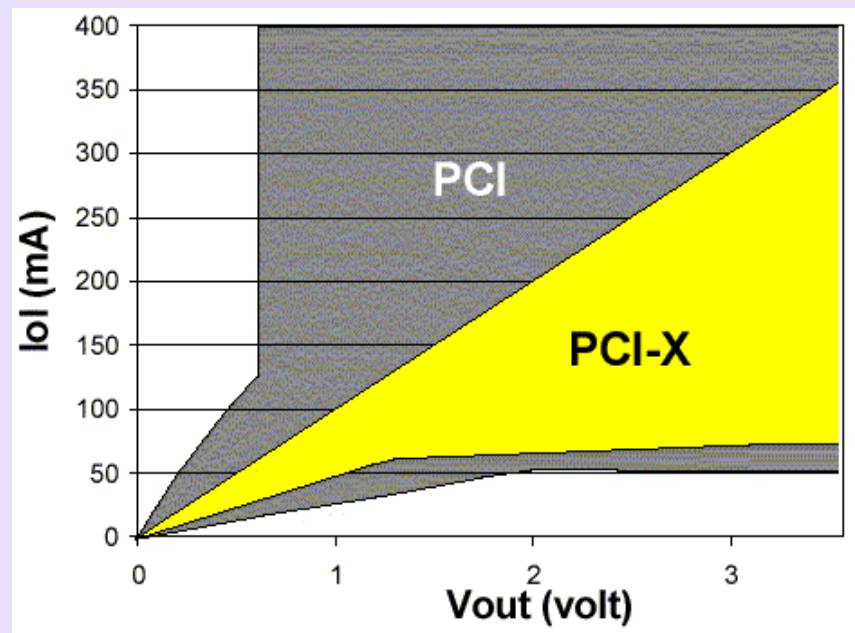
I/O Buffer Design Issues



Mode 1, 3.3V Signaling, Current-Voltage Curves



PCI-X Pull-Up Output Buffer I/V Curves



PCI-X Pull-Down Output Buffer I/V Curves

- PCI-X 3.3V driver range is a subset of allowable range for 3.3V conventional PCI

Fast corner : Process: FF; Temp: 0C; Voltage: 3.6V

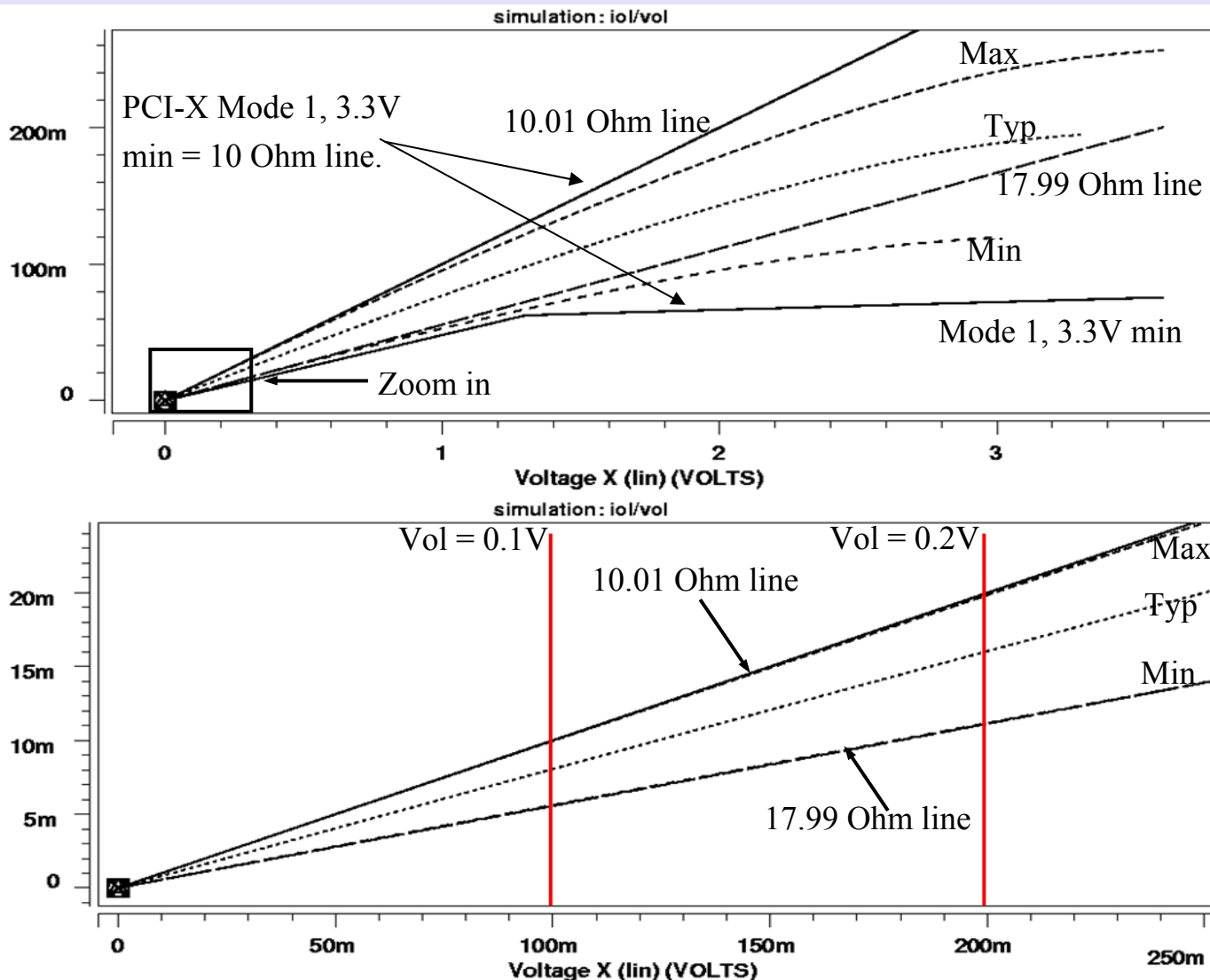
Typ corner : Process: TT; Temp: 27C; Voltage: 3.3V

Slow corner: Process: SS; Temp: 125C; Voltage: 3.0V

Iol/Vol Curves for 1.5V and 3.3V Signaling

Mode 2, Cat 1

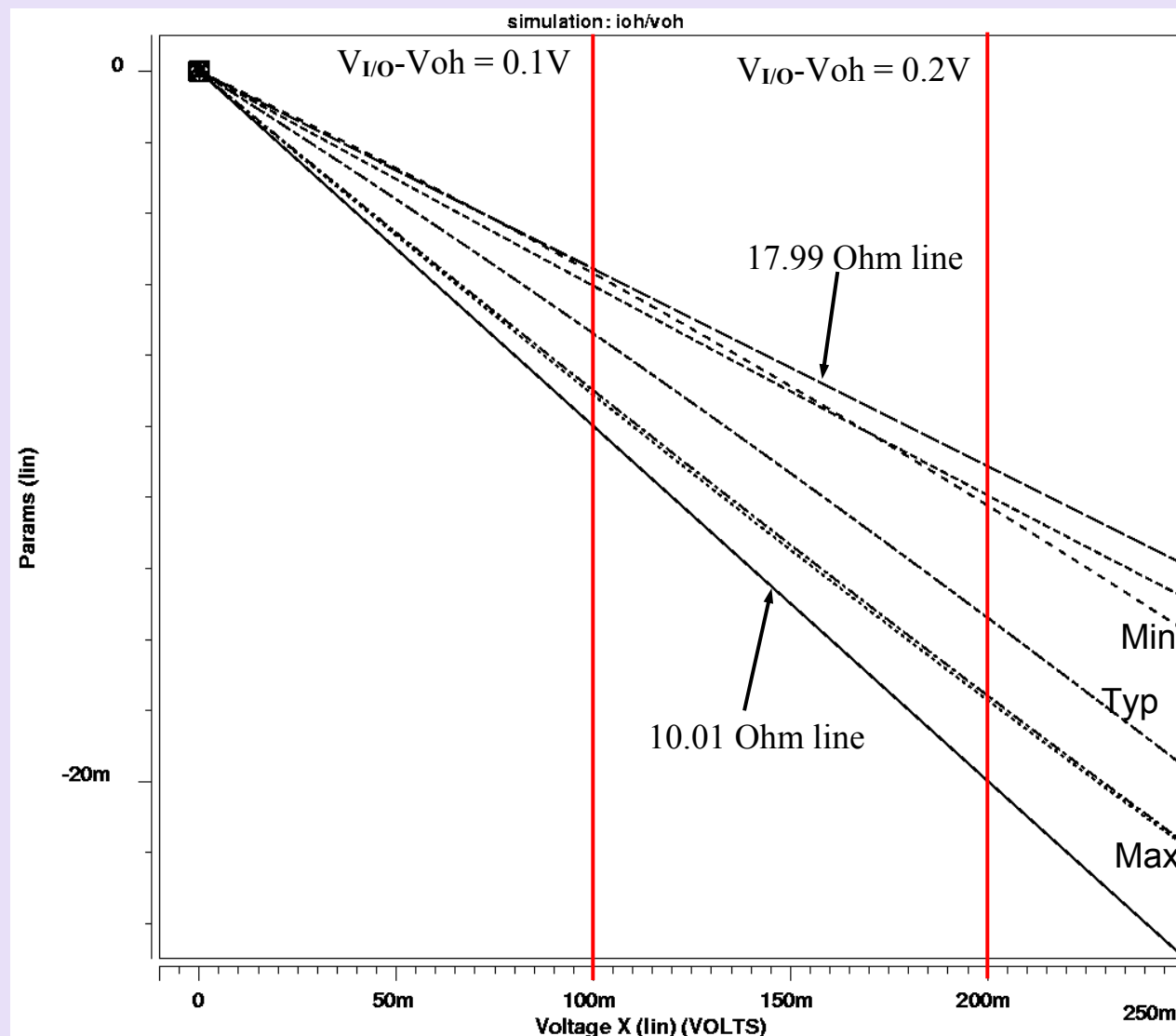
- Vol(DC) spec:
min = 0.1V max = 0.2V
with 57R to $V_{IO}/2$
- Recommended
pulldown impedance:
14R +/-4R (10 to 18R)
- Must be linear within
the Vol(ac) to Voh(ac)
range
- Subset of 3.3V
signaling pulldown
requirements
- Common design for
1.5V and 3.3V signaling



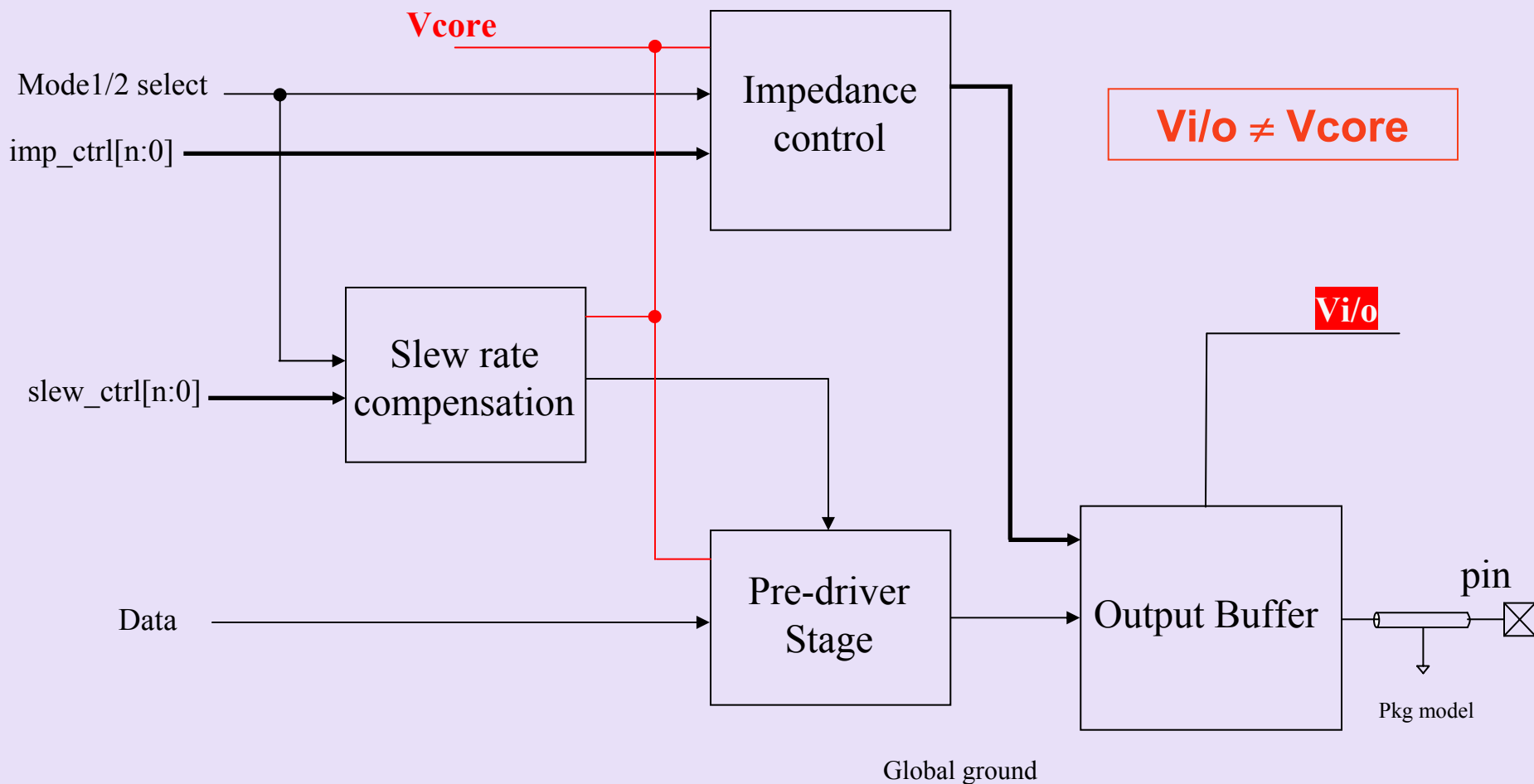
Ioh/Voh Curves for 1.5V and 3.3V Signaling

Mode 2, Cat 1

- Voh(DC) spec:
min = $V_{IO} - 0.2V$
max = $V_{IO} - 0.1V$
with 57R to $V_{IO}/2$
- Recommended pullup impedance: 14R +/-4R (10 to 18R)
- Must be linear within the Vol(ac) to Voh(ac) range
- Different designs for 1.5V and 3.3V signaling since different V_{IO}



Driver Block Diagram



Output Buffer Modeling

- Spice or Ibis models
- Due to slew rate control, strong driver models may not have the fastest edge rate, weak models the slowest edge rate
- Traditional PVT corner simulations not sufficient
- May require more than one Ibis model for system level simulations
 - ✓ strong-fast, strong-slow, weak-fast, weak-slow
 - Weak = $V_{ol_dc}(max)$; Strong = $V_{oh_dc}(min)$



PCB Layout Considerations



Board Layout Considerations (1)

- Spec for add-in card routing requirements
 - ✓ Impedance = $57R \pm 10\%$
 - ✓ Max trace length (Table 2-24)
 - ✓ Min spacing between data, strobe and data
 - ✓ Electrical length matching within a data subgroup
 - ✓ Timing skew between data subgroups
- Recommendations for system board
 - ✓ Same parameters as above

Timing skew between data subgroups is extremely important – to mitigate the effect of simultaneously switching signals through the connector

Add-in Card Trace Length Limits

- In Mode 2, electrical and physical dimensions are interchangeable

Table 2-24: Add-in Card Trace Length Limits

Parameter		PCI-X		Conventional PCI (ref)		Units	Notes
		Min	Max	Min	Max		
CLK length	Physical	2.4	2.6	2.4	2.6	inch	
	Electrical	360	468			ps	
32-bit interface signal length: AD[31::00], C/BE[3::0]#, REQ64#/ECC[6], ECC[5::2], ACK64#/ECC[1], PAR/ECC[0], FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, PERR#, LOCK#, REQ#, GNT#, IDSEL, SERR#	Physical	0.75	1.5	-	1.5	inch	
	Electrical	113	270			ps	1
64-bit interface extension signal length: AD[63::32], C/BE[7::4]#, PAR64/ECC[7]	Physical	1.75	2.75	-	2.0	inch	
	Electrical	263	495			ps	1
RST# length	Physical	0.75	3.0	-	-	inch	
	Electrical	113	540			ps	

Note:

- These limits are optionally adjusted by an amount specified by the device vendor for package electrical length compensation, as described below.

$$360\text{ps}/2.4'' = 150\text{ps}/\text{inch}$$

$$468\text{ps}/2.6'' = 180\text{ps}/\text{inch}$$

- Min params are with fastest PCB prop delay of 150ps/inch (microstrip)
- Max params are with slowest prop delay of 180ps/inch (stripline)

Board Layout Considerations (2)

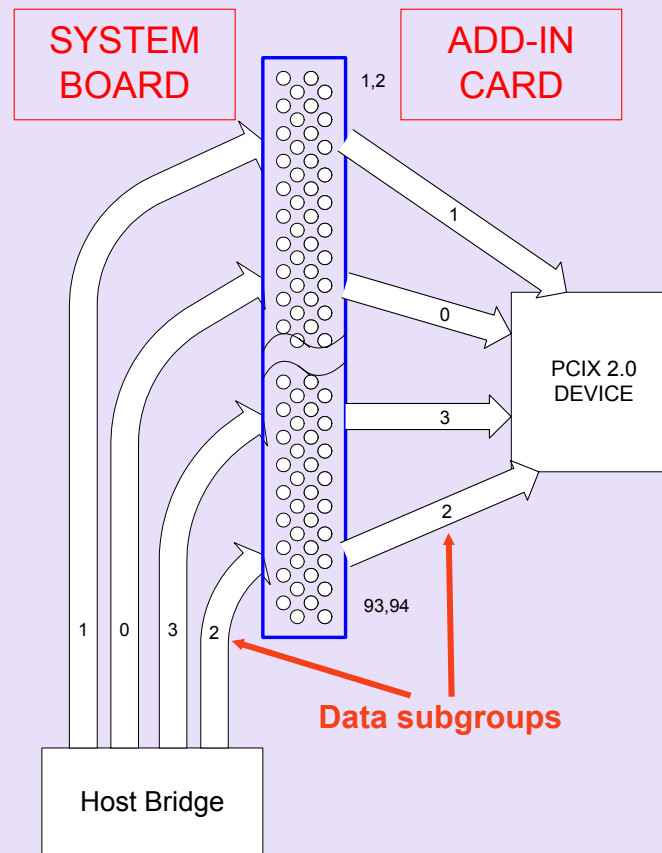
Table 2-11: Source-Synchronous Signaling Groups, Mode 2

Group Number (Note 2)	Data Strobes	Data Strobe Connector Signal Names (Note 1)	Source-Synchronous Signaling Group
0	FSTROBE[0], SSTROBE[0]	C/BE[1::0]#	AD[15::0], PAR/ECC[0], ACK64#/ECC[1], REQ64#/ECC[6]
1	FSTROBE[1], SSTROBE[1]	C/BE[3::2]#	AD[31::16], ECC[5::2]
2	FSTROBE[2], SSTROBE[2]	C/BE[5::4]#	AD[47::32]
3	FSTROBE[3], SSTROBE[3]	C/BE[7::6]#	AD[63::48], PAR64#/ECC[7]

Table 2-25: Add-in Card Signal Electrical Length Matching and Separation, Mode 2

Group Number (Note 1)	Maximum Base Difference Between Signals and Data Strobes	Maximum Device Package Compensation	Minimum Strobe-to-Strobe Separation (Note 2)	Units
0	±35	±75	±80	ps
1	±35	±75	±80	ps
2	±35	±75	±80	ps
3	±35	±75	±80	ps

Table D-5: Recommended difference in electrical length for system board between **strobes** of different groups = **180ps**



Board Layout Considerations (3)

- Pin swapping to ease system board layout
 - ✓ 2 pins are logically swapped so they are physically close to the rest of the data signals in their subgroup

	PCI-X 1.0 (ref)		PCI-X 2.0		
65	C/BE[6]#	C/BE[5]#	C/BE[6]#	CBE[5]#/AD[48]	Note 1
66	C/BE[4]#	+V/I/O (3.3V)	CBE[4]#/AD[49]	+V/I/O (3.3V/1.5V)	Note 1
78	AD[49]	Ground	AD[49]/CBE[4]#	Ground	Note 1
79	+V/I/O (3.3V)	AD[48]	+V/I/O (3.3V/1.5V)	AD[48]/CBE[5]#	Note 1

Notes:

1. C/BE[4]# swaps locations with AD[49] and C/BE[5]# swaps locations with AD[48] when the bus initializes in PCI-X Mode 2 relative to their locations in PCI-X Mode 1 and conventional mode.

- When assigning pins ECC[5-3] on add-in card *device* pay careful attention to the add-in card trace length requirements for those signals. Their connector pins (A-9, B-10, A-11) are farthest away

8 Layers Board Stackup Example

- 4 Routing layers, 2 striplines, 2 microstrips
- Calculations done with $\epsilon_r = 4.15$. PCB = FR4
- Ample decoupling caps between power Vi/o and GND layers

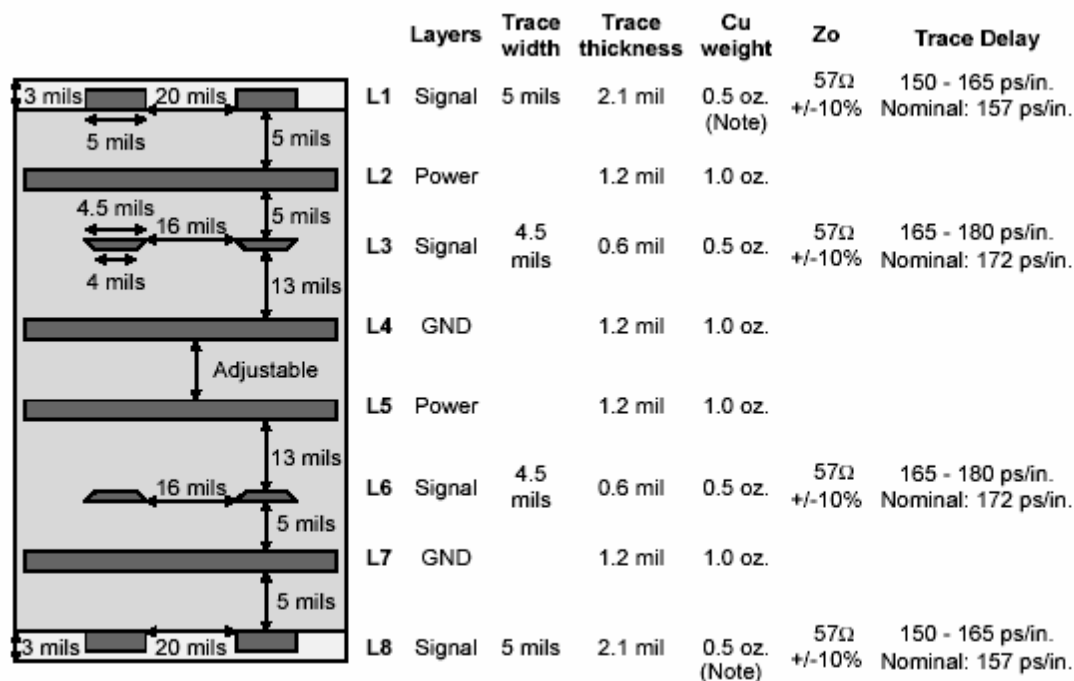


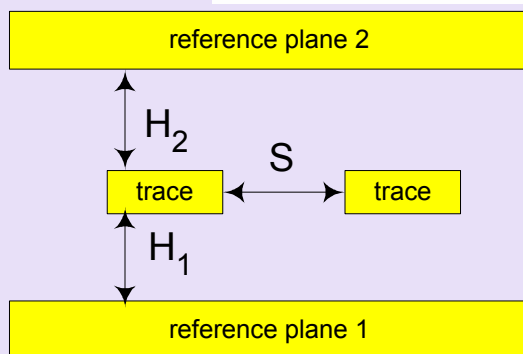
Figure B-2: Example Eight-Layer Stack-up

Trace Spacing Geometries

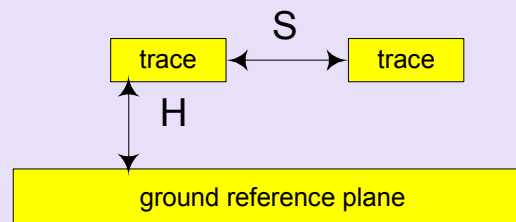
- Mode 2 spec requires a minimum spacing to height (S/H) ratio for add-in card, recommends S/H ratio for system board. ($H = \min(H_1, H_2)$) for stripline
- Keeps crosstalk $< 5\%$
- SS and CC timings were verified with given dimensions

Table 2-27: Mode 2 Add-in Card Trace Spacing and Height

Symbol	Parameter	Microstrip	Stripline
S/H	Minimum Spacing to Height Ratio	4	3



Stripline



Microstrip

System Board Geometries

- S/H ratio recommendation for system board
 - ✓ Assumes tight spacing (0.8" center) between adjacent connectors, ~ 0.5" routing area
 - ✓ Doable in 2 stripline, 2 microstrip @ 266MHz sys
 - ✓ Microstrip not recommended for 533MHz system due to excessive crosstalk and tighter timing

Table D-6: Mode 2 Trace Spacing and Height

Symbol	Parameter			Microstrip	Stripline
S/H	Minimum Add-in Card Spacing to Height Ratio (ref)			4	3
	Minimum System Board Spacing to Height Ratio	PCI-X 266 systems	Strobes	5	4
			Other than strobes	3	2.1
		PCI-X 533 systems	Strobes	(note)	4
			Other than strobes	(note)	2.1

Note: not recommended due to excessive crosstalk



System Level Simulation Considerations



PCI Connector Model

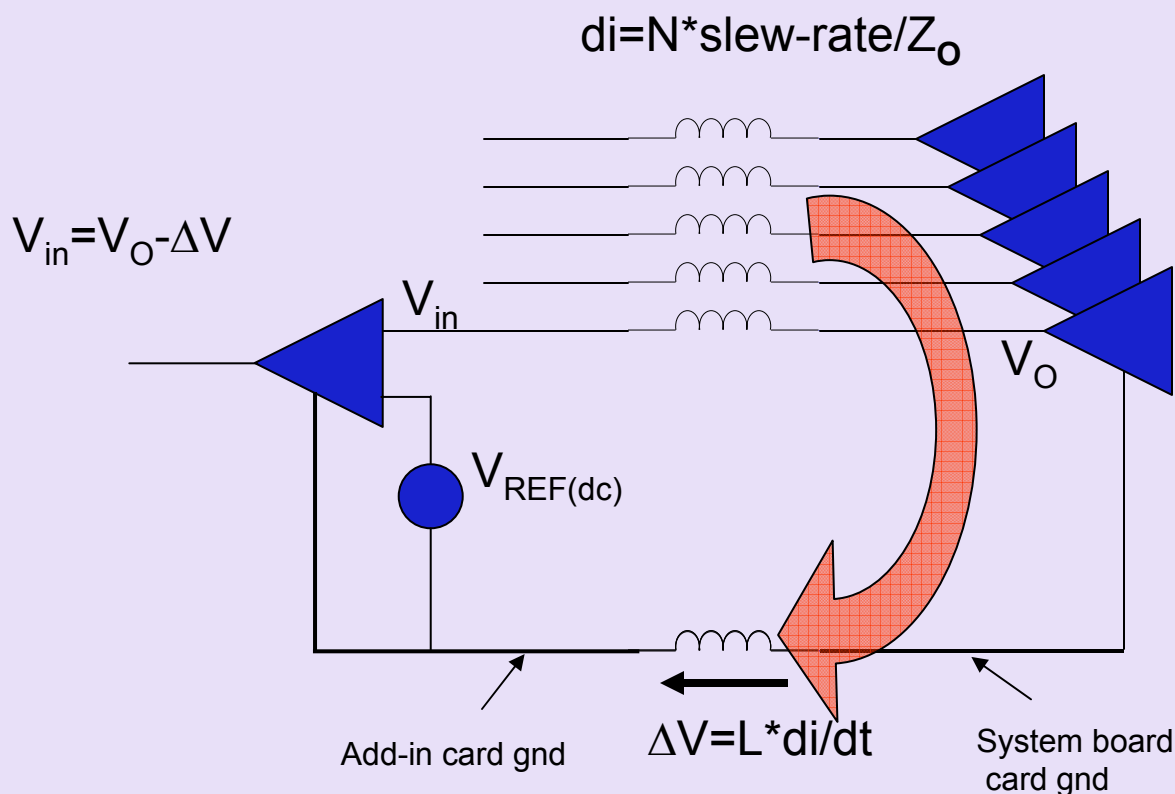
- Poor signal to power/gnd ratio thru connector
- Crosstalk from signal pins onto power/ground pins will cause 'ground bounce' thru connector
- Need to use coupled connector model, also called Multi-line Model (MLM)
- Cannot assume that add-in card ground and system board ground are at the same voltage potential (ground reference)

✦ *Need to float one relative to the other*

	KEYWAY	
63	Reserved	Ground
64	Ground	C/BE[7]#
65	C/BE[6]#	C/BE[5]#
66	C/BE[4]#	+V/I/O (1.5V)
67	Ground	PAR64/ECC[7]
68	AD[63]	AD[62]
69	AD[61]	Ground
70	+V/I/O (1.5V)	AD[60]
71	AD[59]	AD[58]
72	AD[57]	Ground
73	Ground	AD[56]
74	AD[55]	AD[54]
75	AD[53]	+V/I/O (1.5V)
76	Ground	AD[52]
77	AD[51]	AD[50]
78	AD[49]	Ground
79	+V/I/O (1.5V)	AD[48]
80	AD[47]	AD[46]
81	AD[45]	Ground
82	Ground	AD[44]
83	AD[43]	AD[42]
84	AD[41]	+V/I/O (1.5V)
85	Ground	AD[40]
86	AD[39]	AD[38]
87	AD[37]	Ground
88	+V/I/O (1.5V)	AD[36]
89	AD[35]	AD[34]
90	AD[33]	Ground
91	Ground	AD[32]
92	Reserved	Reserved
93	Reserved	Ground
94	Ground	Reserved

PCI Connector Issues (1)

The input voltage, measured relative to the local ground, will be affected by the number of simultaneously switching signals thru the connector



PCI Connector Issues (2)

- 15 AD signals (data and strobes), driven by a full and reduced data patterns
 - ✓ Full data pattern: all bits toggling
 - ✓ Reduced data pattern: AD[54:58] not toggling
 - ✓ Monitor bits AD[62], AD[63], C/BE[6]# and ground

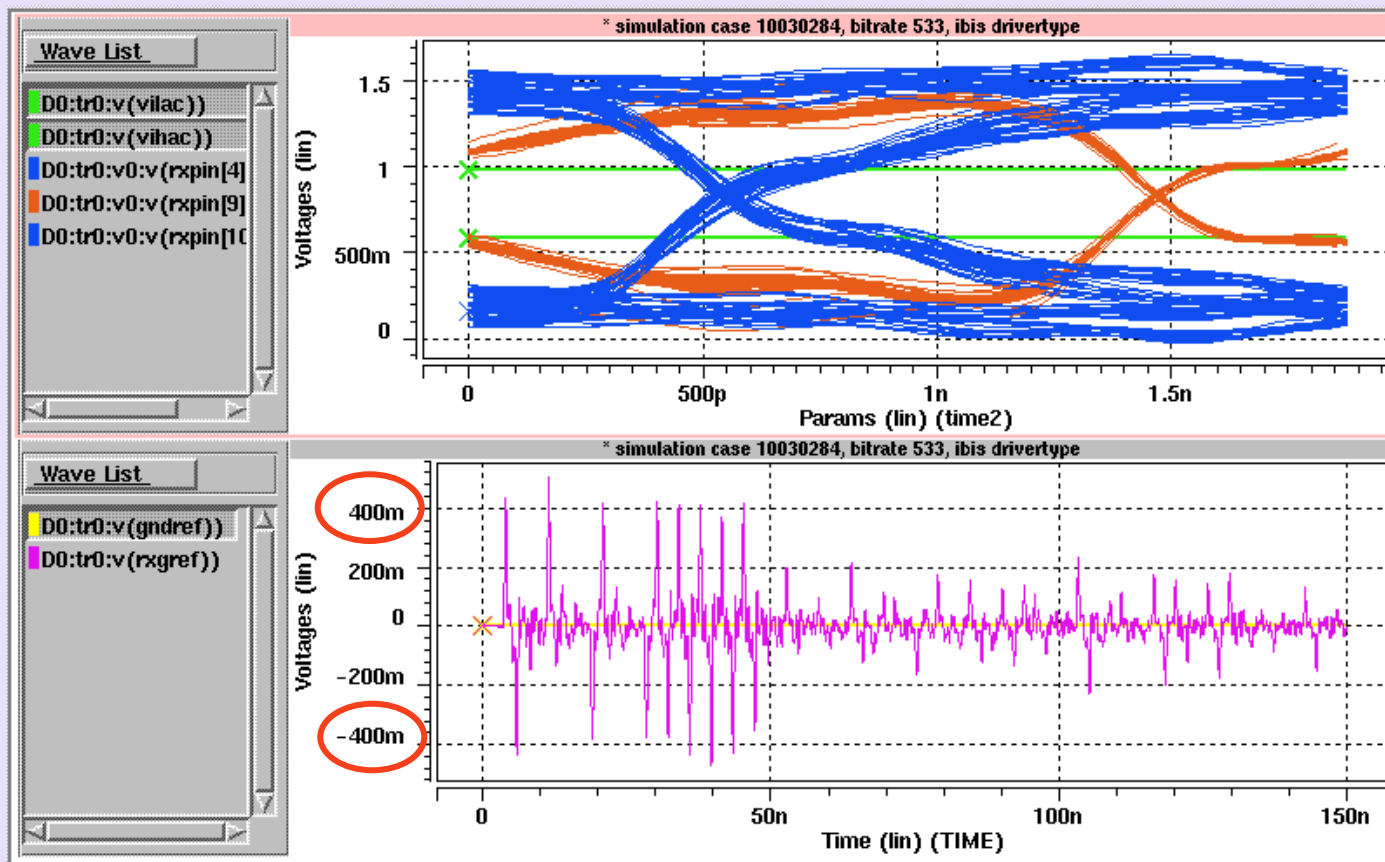
	KEYWAY	
	KEYWAY	
63	Reserved	Ground
64	Ground	C/BE[7]#
65	C/BE[6]#	C/BE[5]#/AD[48]
66	C/BE[4]#/AD[49]	+V/I/O (1.5V)
67	Ground	PAR64/ECC[7]
68	AD[63]	AD[62]
69	AD[61]	Ground
70	+V/I/O (1.5V)	AD[60]
71	AD[59]	AD[58]
72	AD[57]	Ground
73	Ground	AD[56]
74	AD[55]	AD[54]
75	AD[53]	+V/I/O (1.5V)
76	Ground	AD[52]

Selected group of signals

PCI Connector Issues (3)

- Data eye with full data pattern

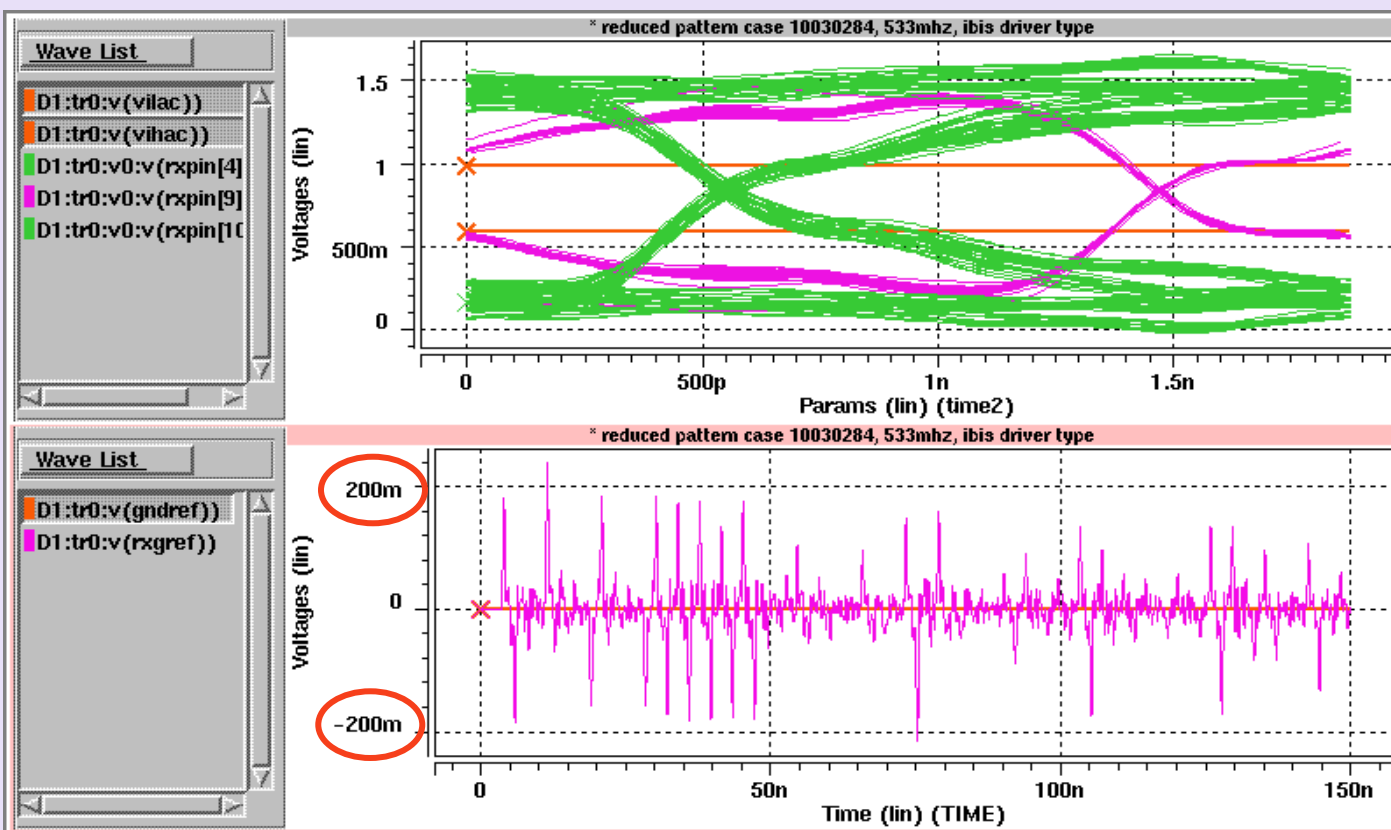
Red = strobe (C/BE[6]#); Blue = bits AD[62], AD[63]; Green = Vilac, Vihac
Magenta = local ground relative to reference ground



PCI Connector Issues (4)

- Data eye with reduced data pattern

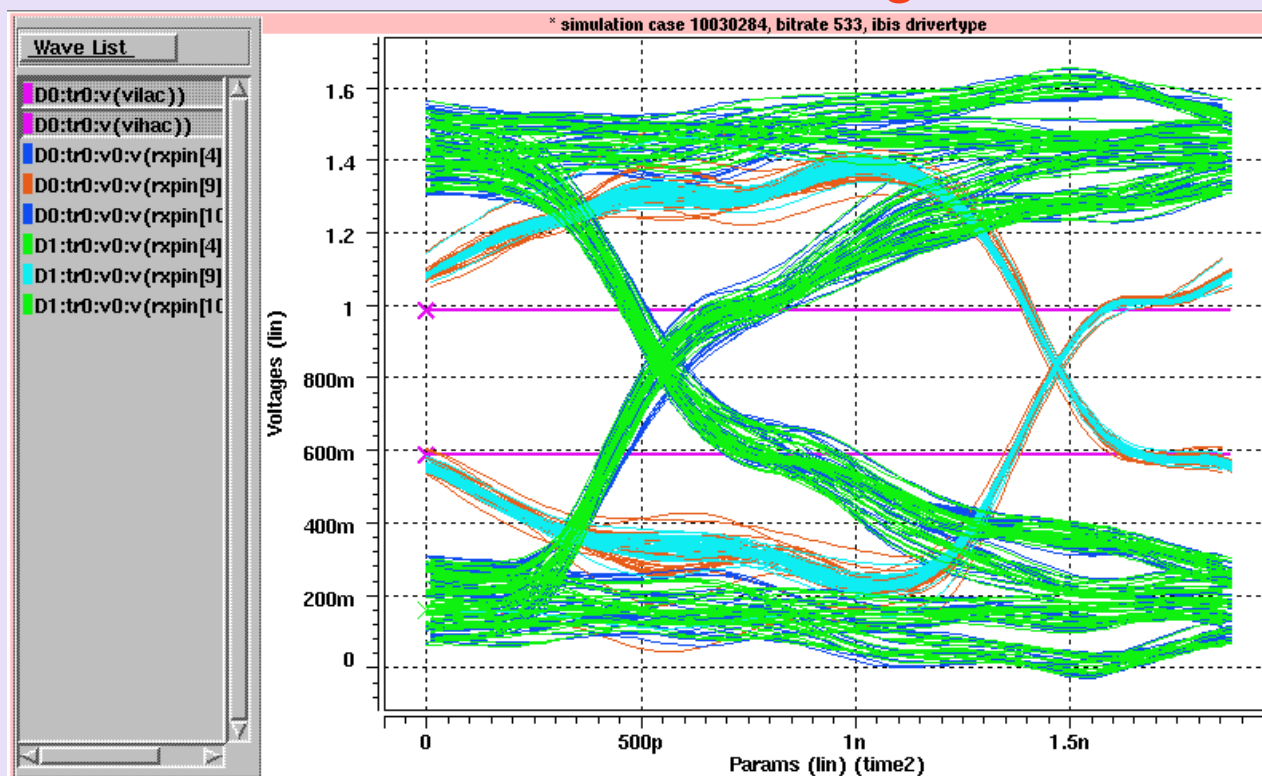
Magenta = strobe; Green = bits AD[62], AD[63]; Brown = Vilac, Vihac
Magenta = local ground relative to reference ground



PCI Connector Issues (5)

- Overlap of data bits from previous waveforms
 Turquoise = strobe, reduced pattern ; Brown = strobe, full data pattern
 Green = data, reduced data pattern; Blue = data, full data pattern
 Magenta = Vilac, Vihac

Effect on timing!!



Thank you for attending the
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Highlights of PCI-X Electrical Specification

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June 2004

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