System & Add-in Card Simulations for PCI Express™ Architecture

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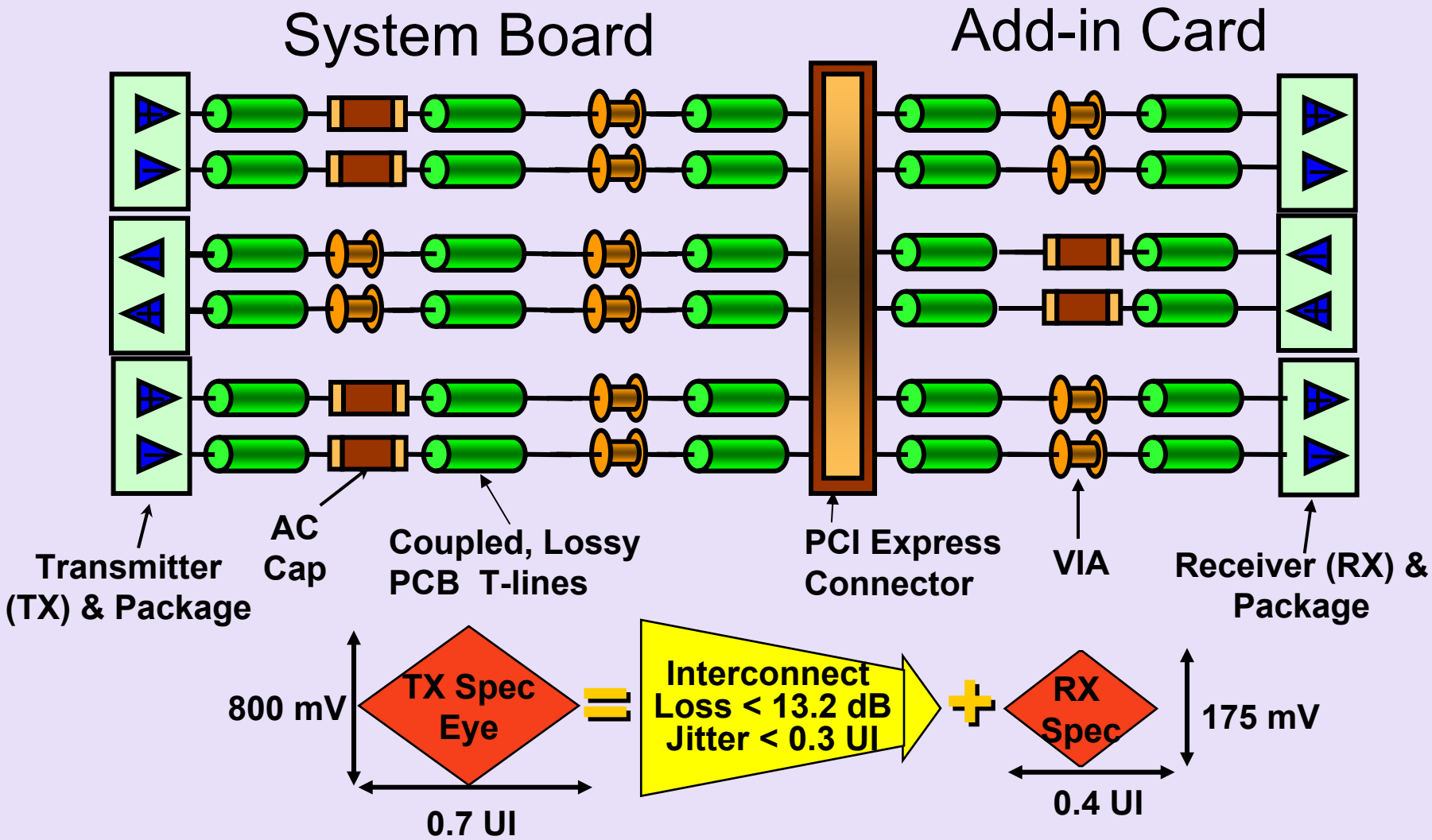
Agenda

- Topology and Modeling
- Simulation methodology
- Add-in card simulations
- System board simulations
- REFCLK simulations
- Package & Receiver considerations
- Summary

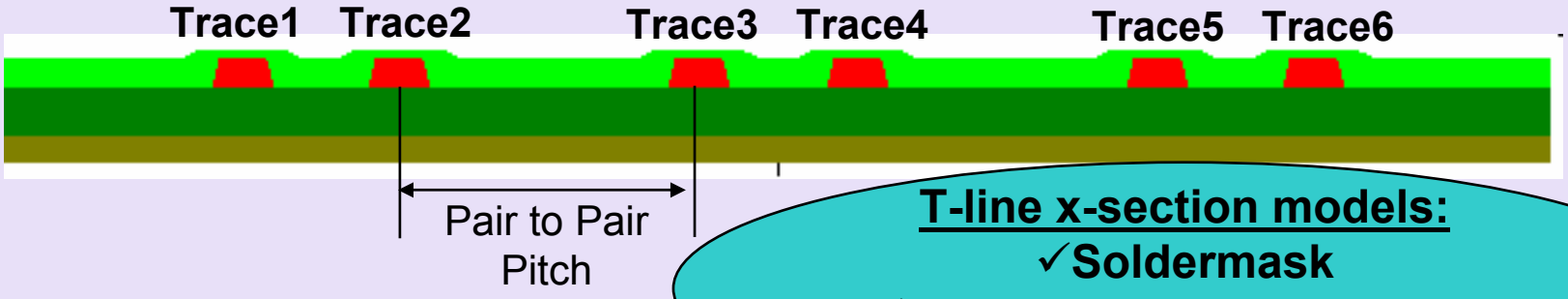
Topology & Modeling



UI = Unit Interval as defined in Base Spec

Topology & Modeling

- Accurate, lossy PCB models required
  - ✓ Use proper cross section in field solver for t-line models
    - T-lines models often needed for both PCB and package!
  - ✓ Create frequency dependant lossy models (RLGC)
  - ✓ 3-coupled pairs desired to enable crosstalk analysis
  - ✓ Corner case models required
    - Min, Max differential impedance & Max loss

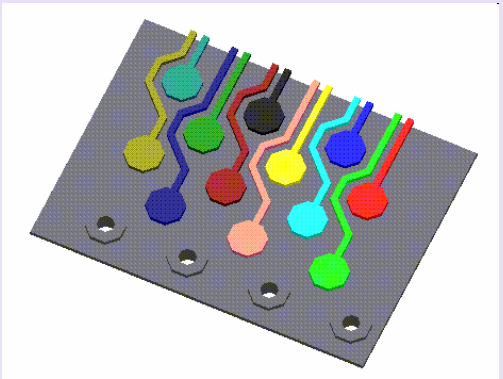


T-line x-section models:
✓Soldermask
✓ Proper trace pitch/spacing
✓Include loss tangent

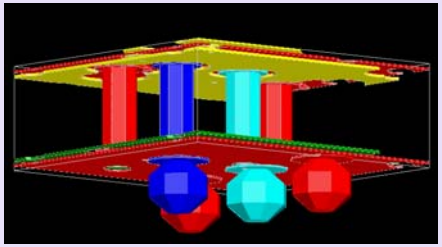
Topology & Modeling

- Accurate 3D models for complex features
  - ✓ Package components, vias, connectors
- Either SPICE lumped-element or full-wave S-param models
  - ✓ HFSS, Q3D, etc.
  - ✓ Included dielectrics, return paths, model for loop inductance, etc.

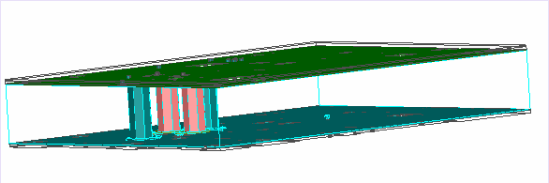
Die Breakout



Package PTH/ball



PCB Via



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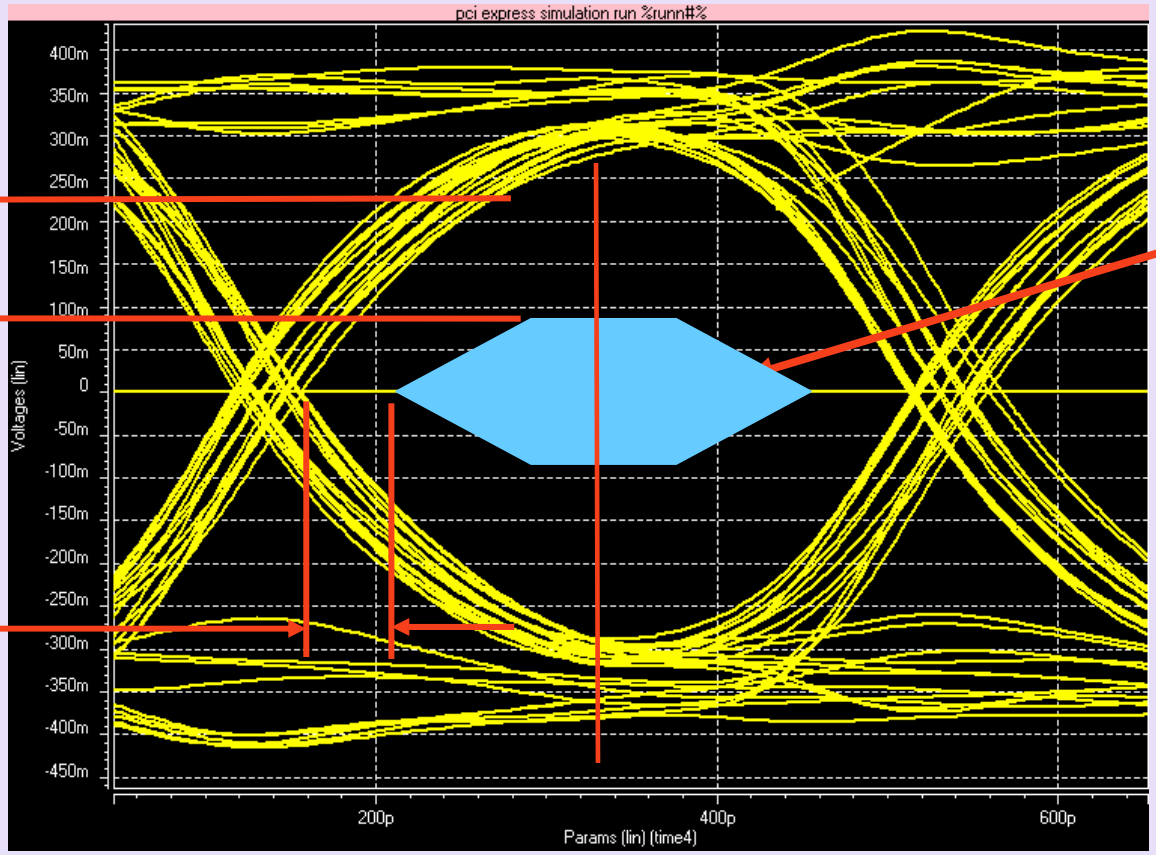
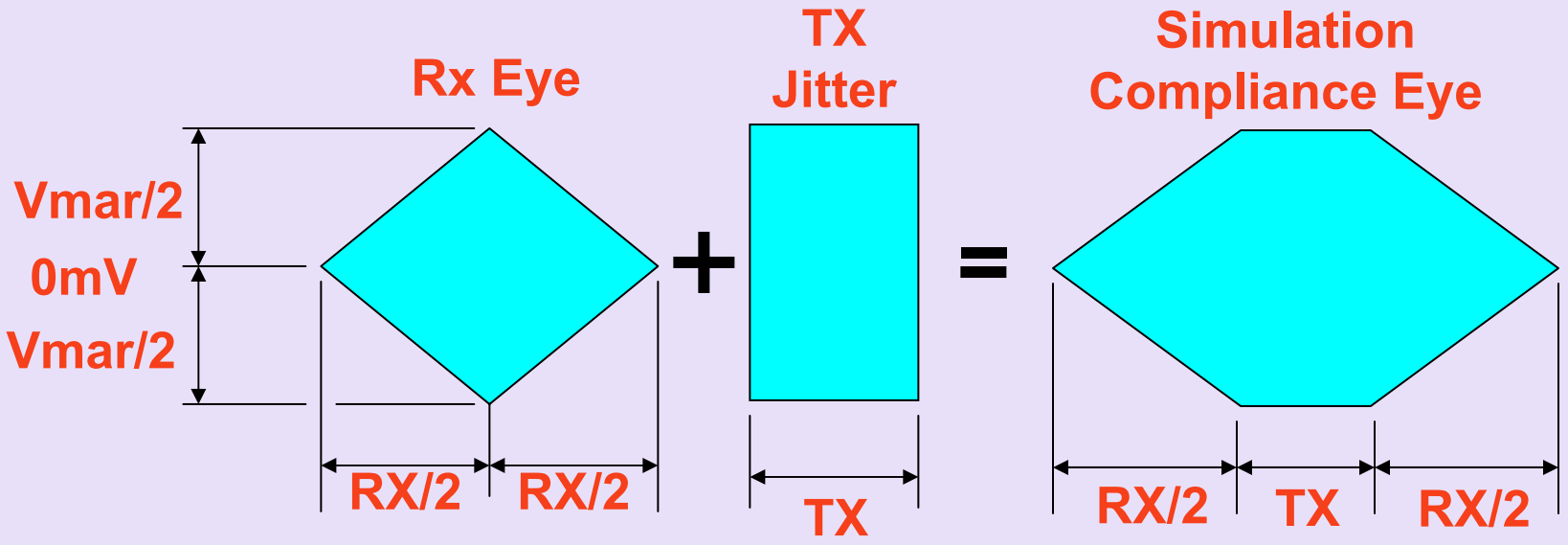
Eye Margins

- Simulations will determine channel Jitter and Voltage margins



Simulation Compliance Eye

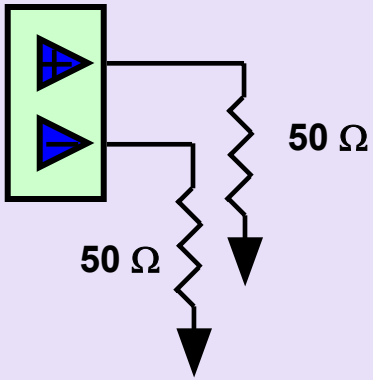
- Must meet compliance eye at specified junction
  - ✓ Min Rx eye width ⇒ Measured at 0 mV differential
  - ✓ Min Vdiff p-p at Rx ⇒ Measured as margin with respect to compliance eye
  - ✓ Add TX jitter (not included in modeling)



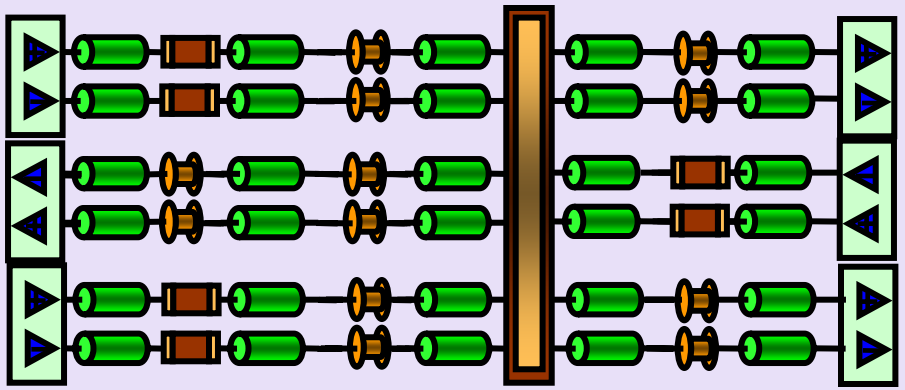
Accounting for TX Jitter

- First calculate the flight time of the signal
  - ✓ *Channel - Test load delay = Interconnect flight time*
- Use same data pattern for channel and test load
  - ✓ TX jitter is removed from interconnect analysis
  - ✓ Reallocate TX jitter to form simulation compliance eye

Test Load

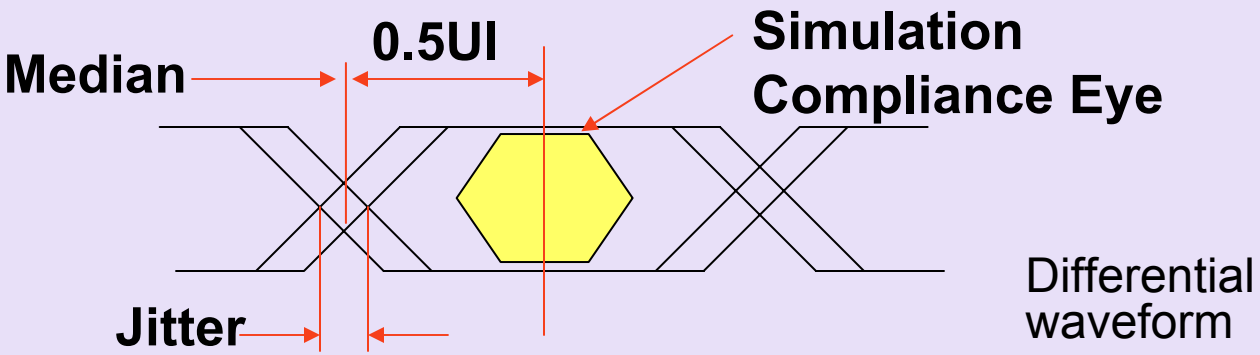


Channel

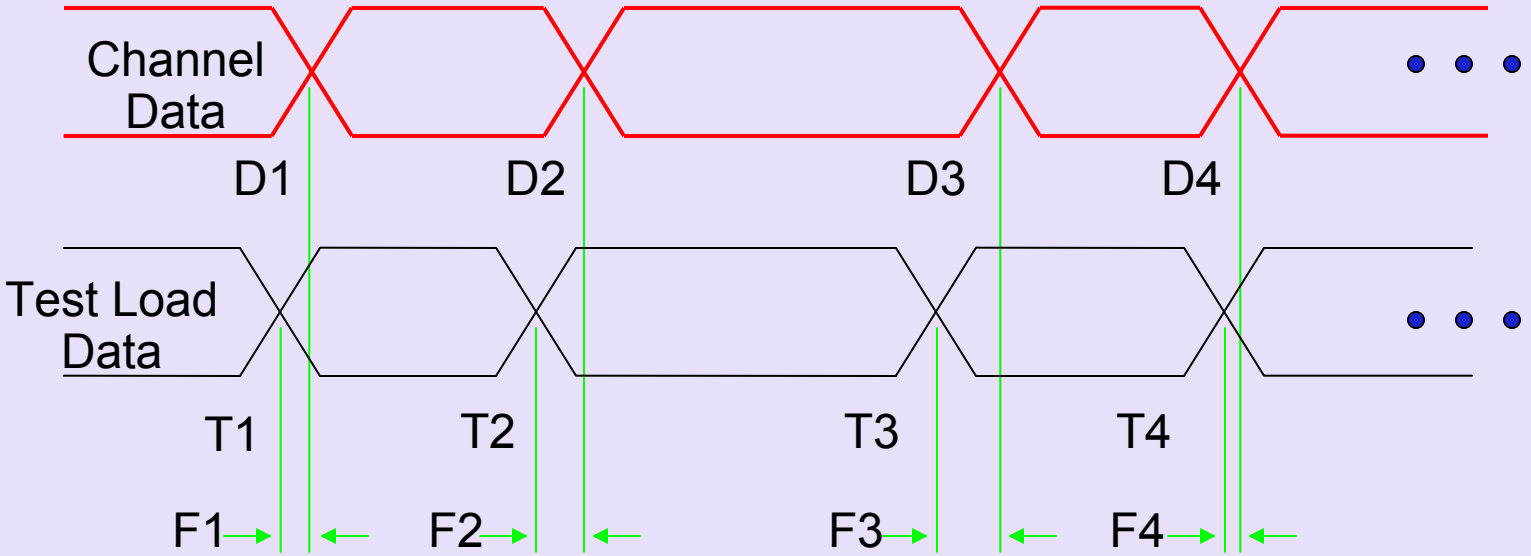


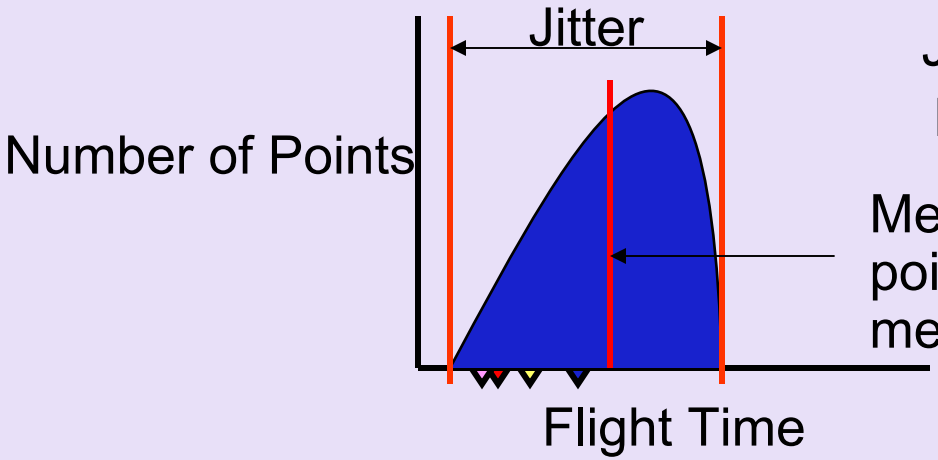
Jitter Margin

- Total interconnect jitter
  - ✓ Differential signal (V_{D+} - V_{D-})
  - ✓ Jitter Median calculated across 250UI
  - ✓ Center Eye 0.5 UI from jitter median
    - Eye center = Median + 0.5UI



Jitter Median Details

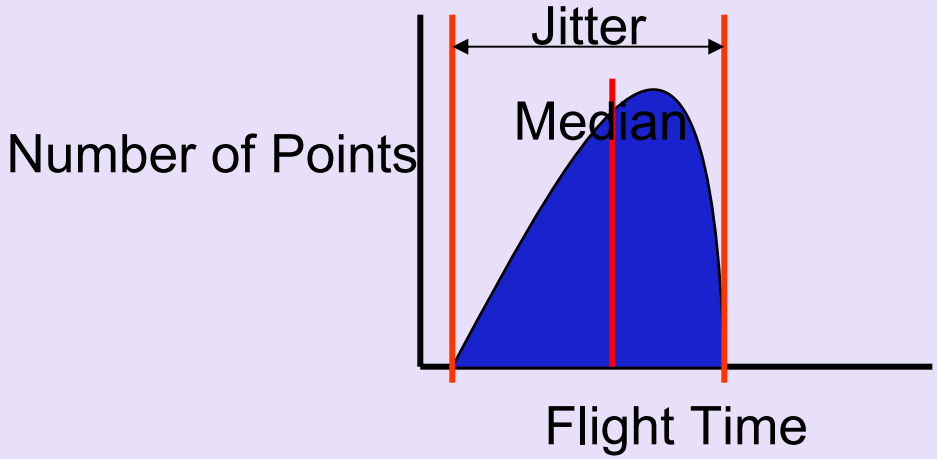


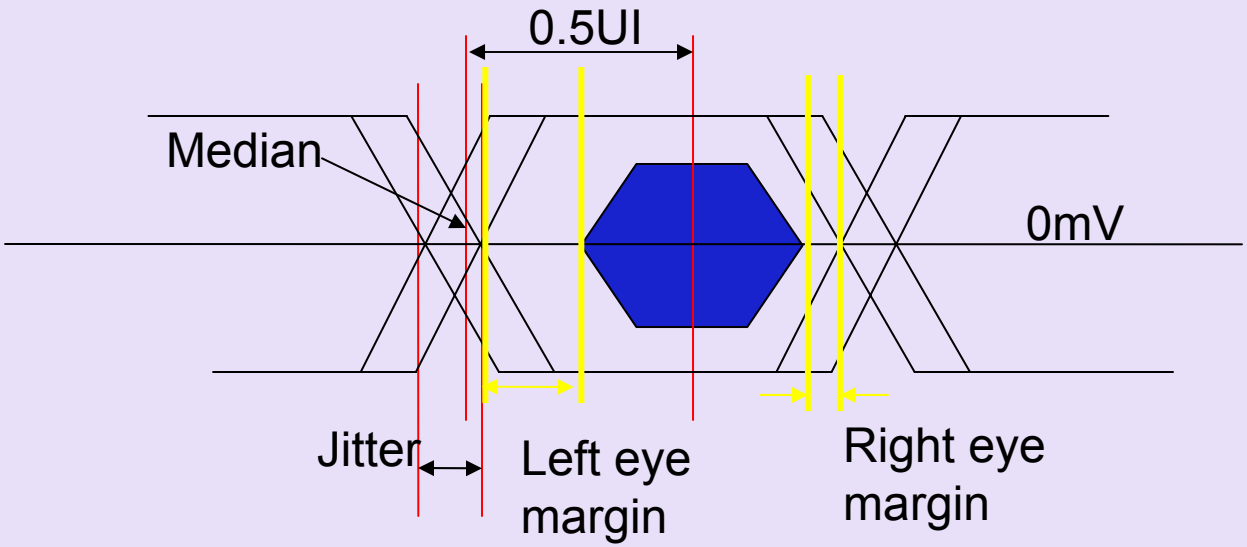


Jitter measured at RX =
Max Flight – Min Flight

Median : Equal number of data points on the left and right of the median line

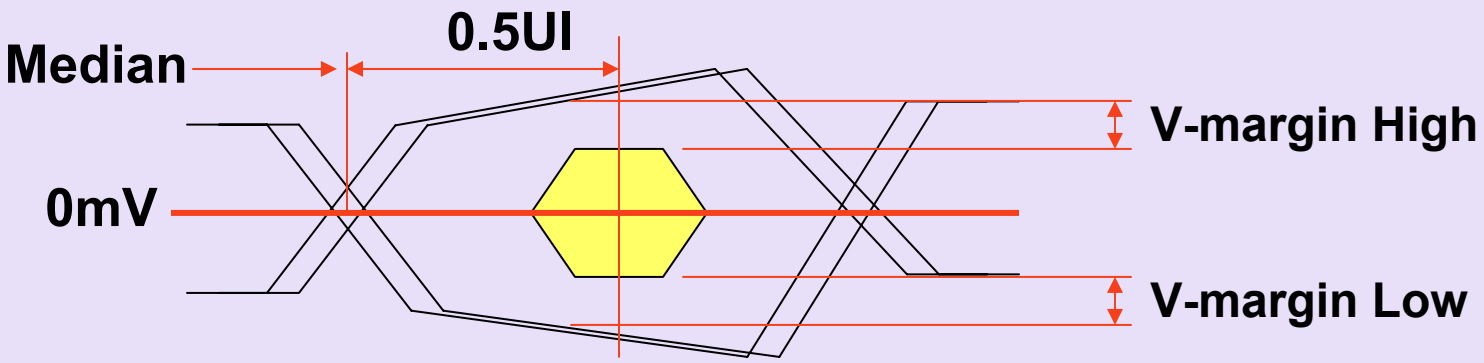
Jitter Outlier Details





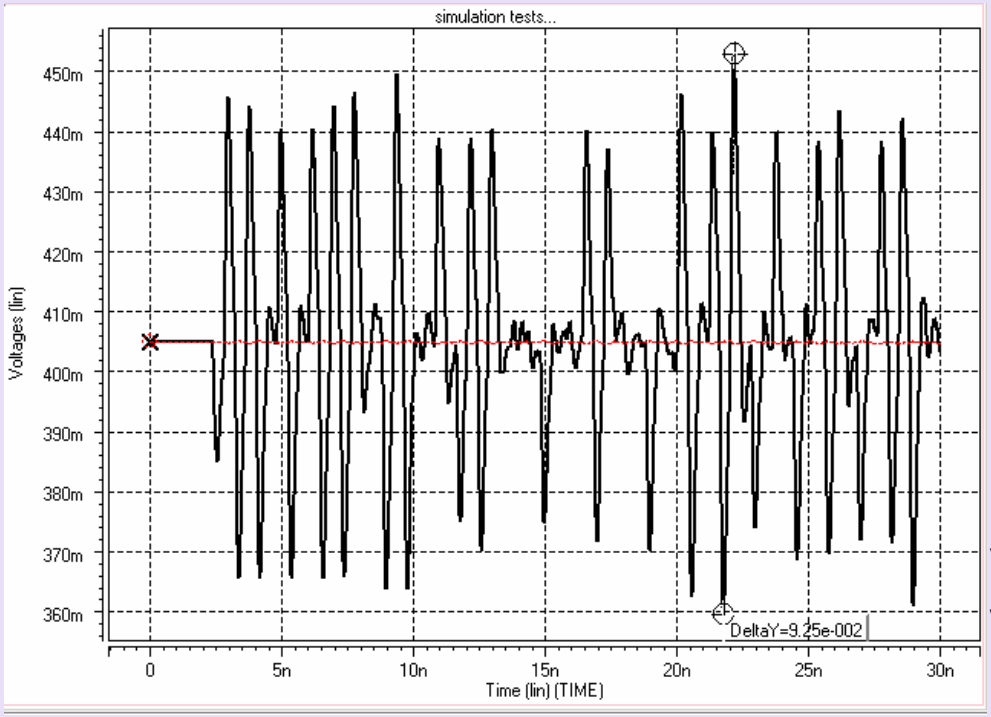
Voltage Margin

- Differential Voltage Margin
  - ✓ Center compliance eye at jitter median + 0.5UI
  - ✓ Voltage margin from differential signal to the simulation compliance eye must be positive



AC Common Mode

- Max AC common mode @ RX < 150 mV peak
  - ✓ $V_{AC\text{-}cm} = |V_{D+} + V_{D-}| \div 2 - V_{DC\text{-}cm}$
  - ✓ $V_{DC\text{-}cm}$ = DC (avg) of $| V_{D+} + V_{D-}| \div 2$



Example: 50 mV peak

$V_{AC\text{-}cm}$ waveform

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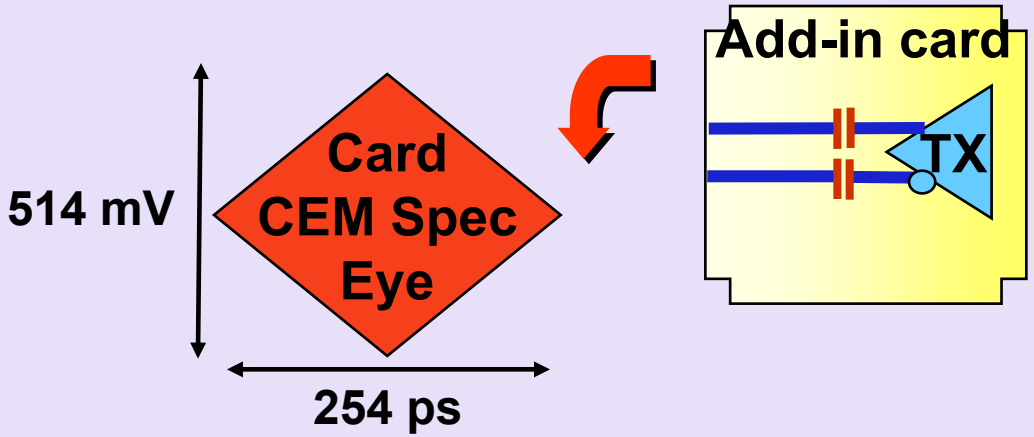
CEM* Card Simulations

- Card ElectroMechanical (CEM*) Spec 1.1 Compliance Eye Diagrams
- Card Transmit Path



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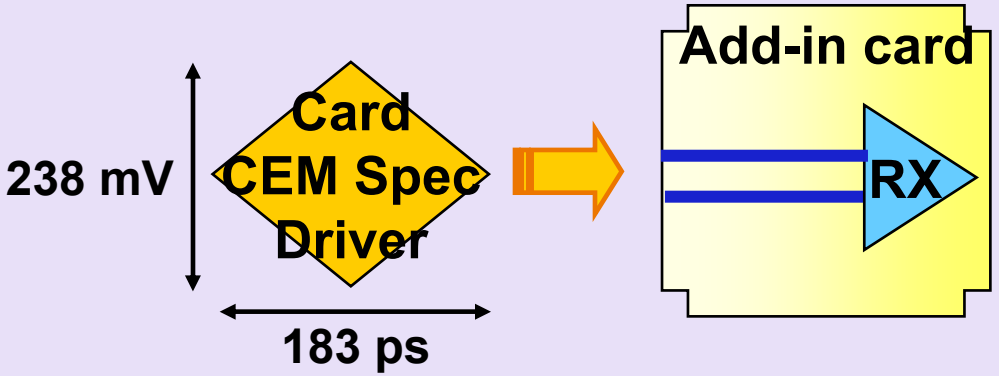

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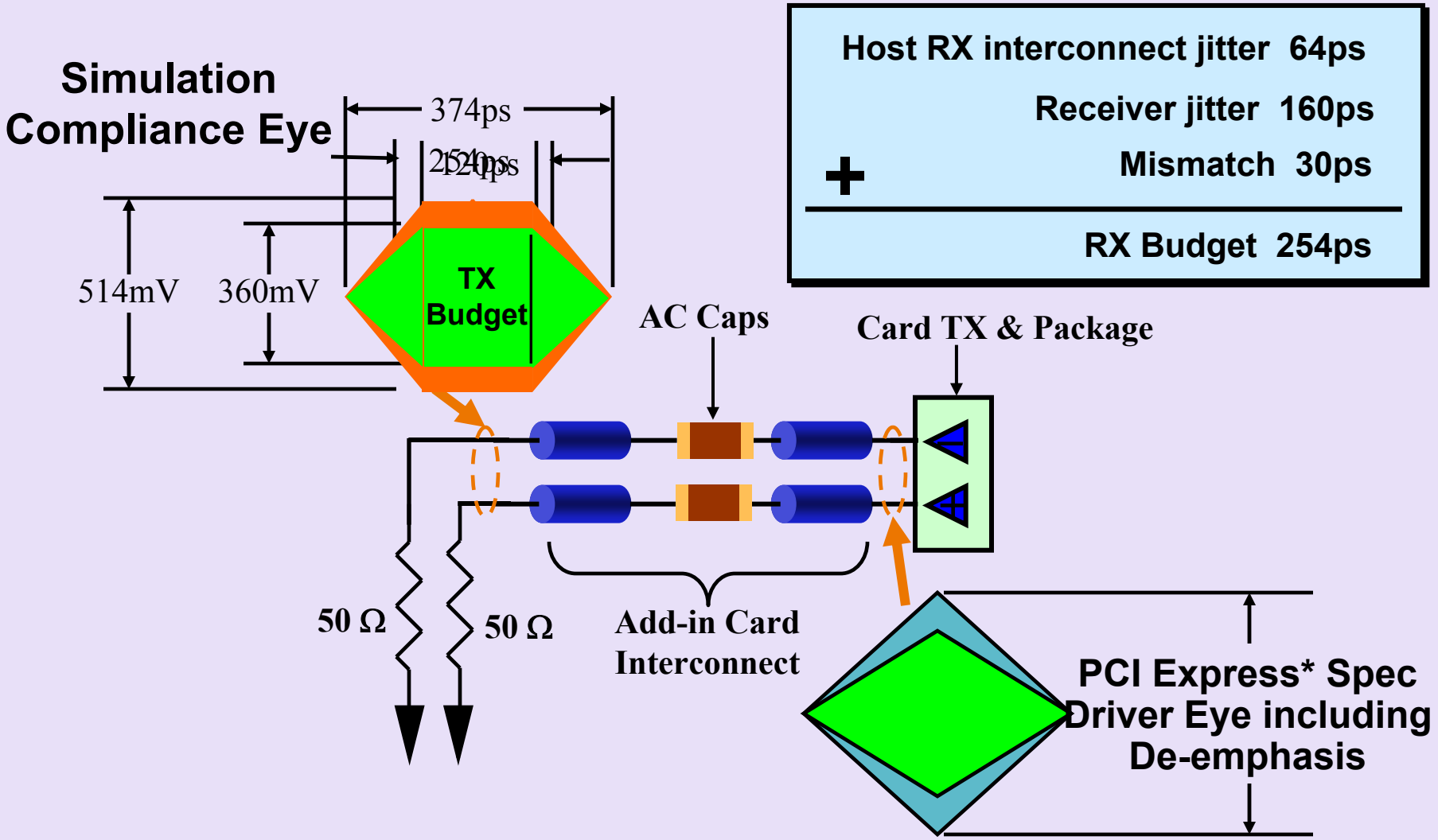

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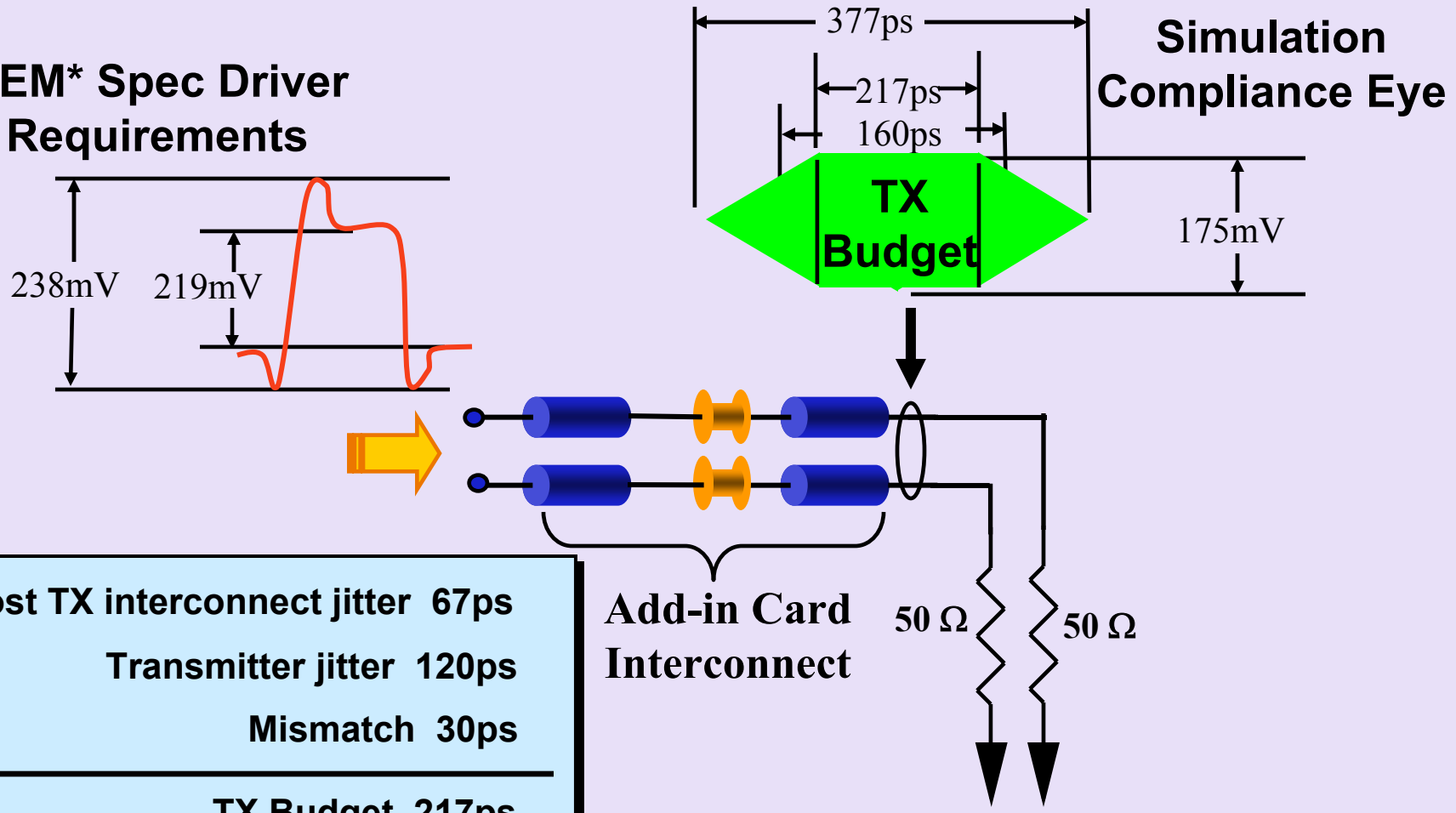

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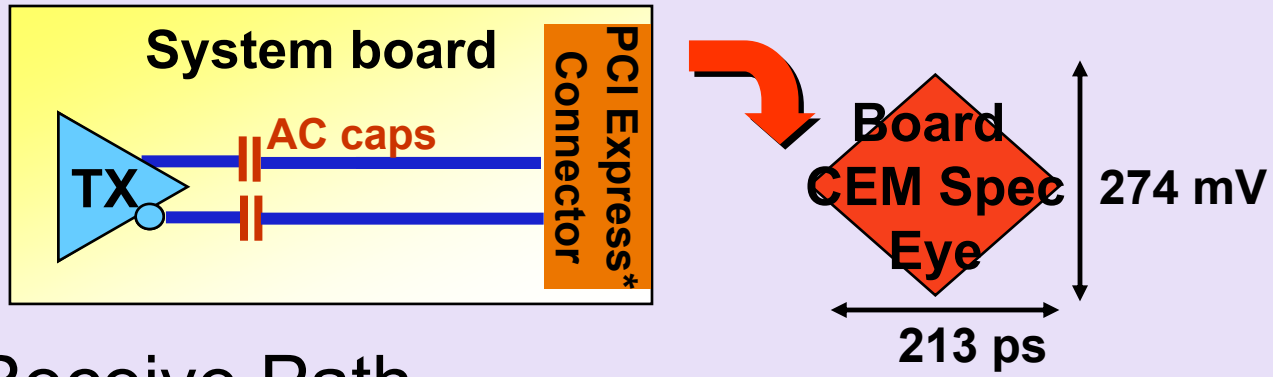
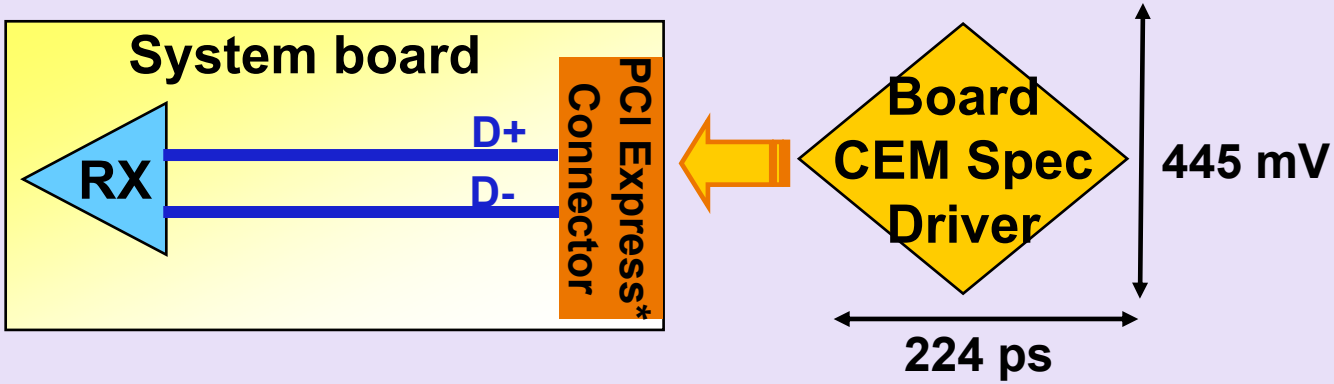


- System Receive Path



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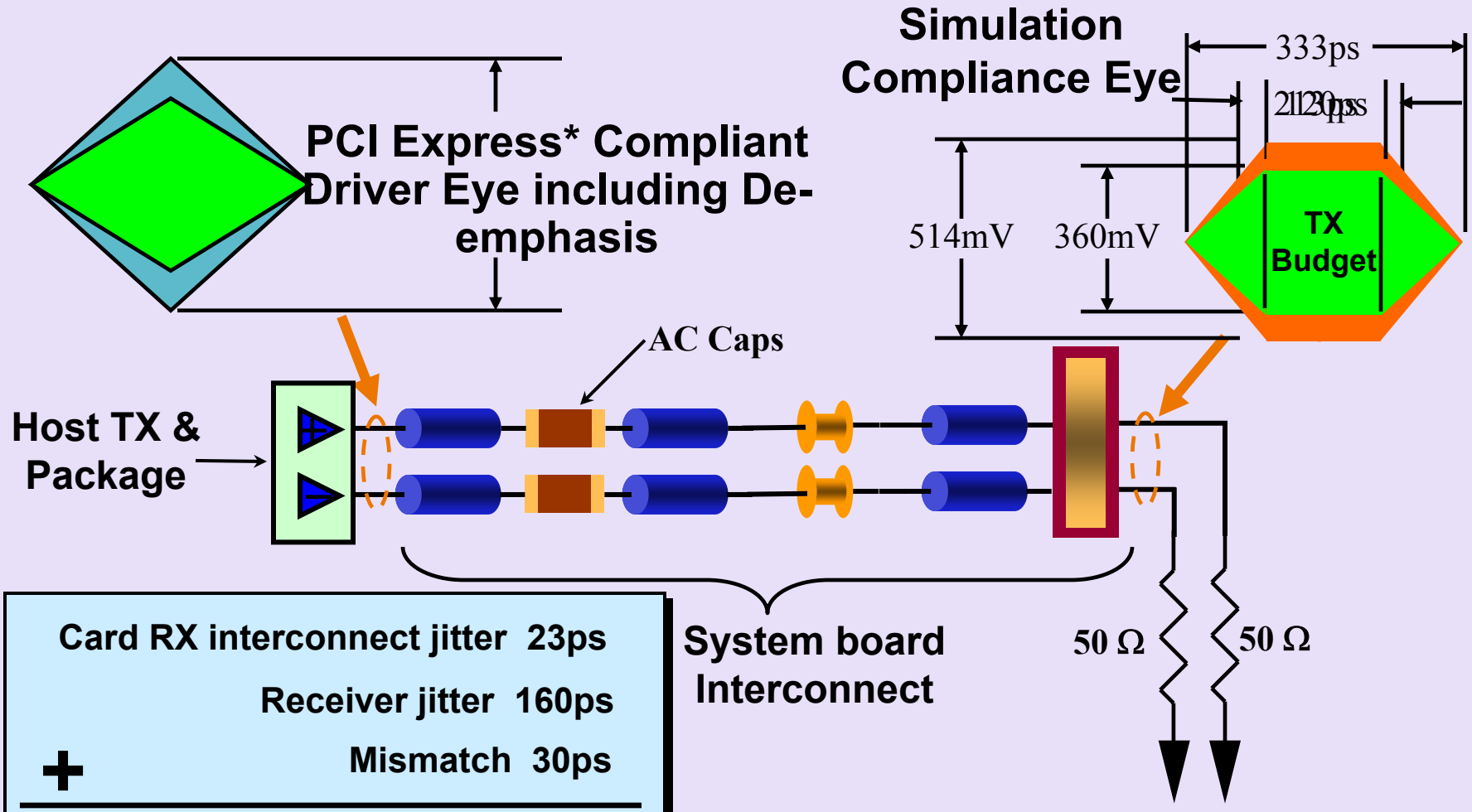

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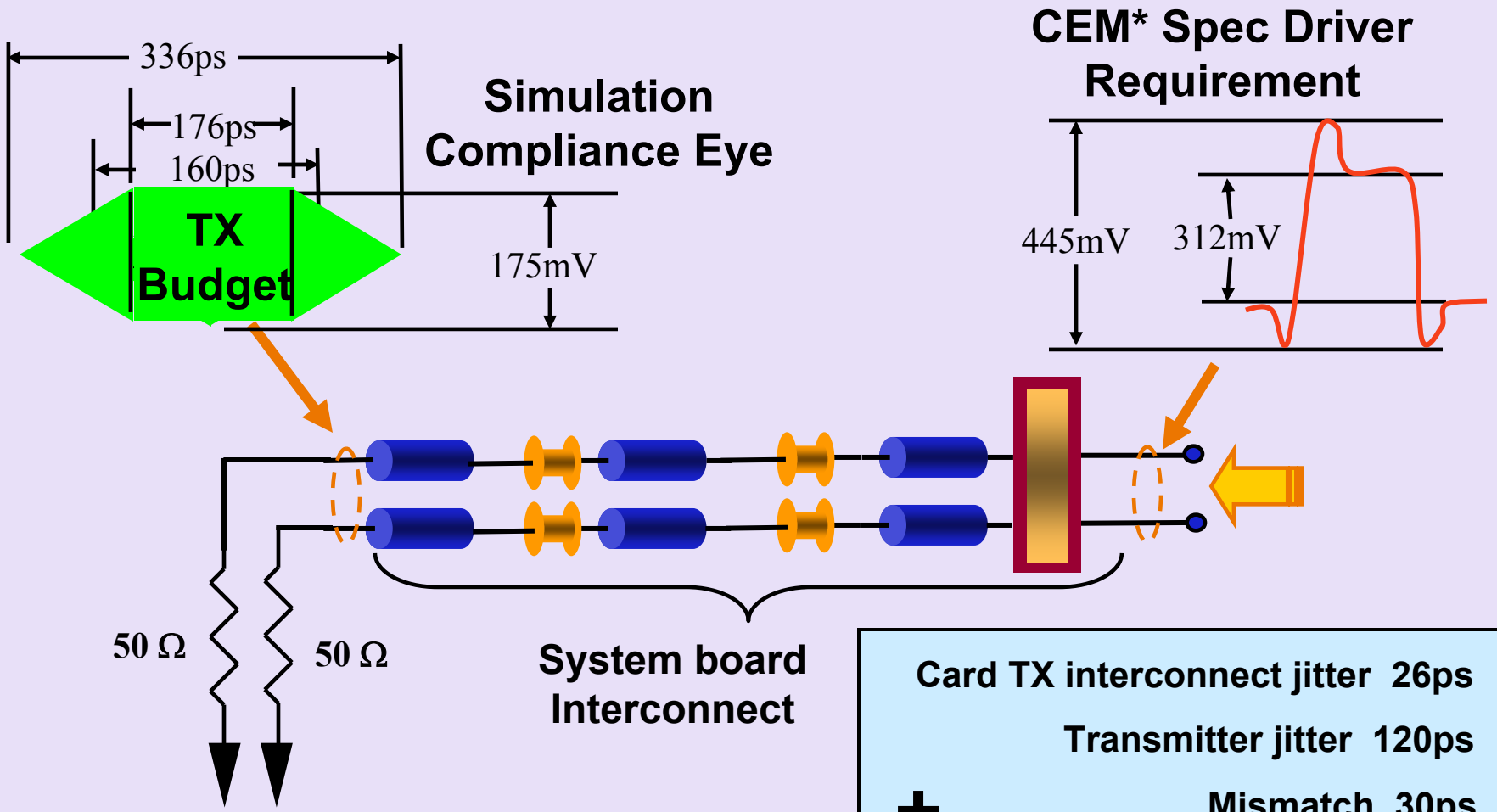

Card TX interconnect jitter	26ps
Transmitter jitter	120ps
+ Mismatch	30ps
TX Budget	176ps

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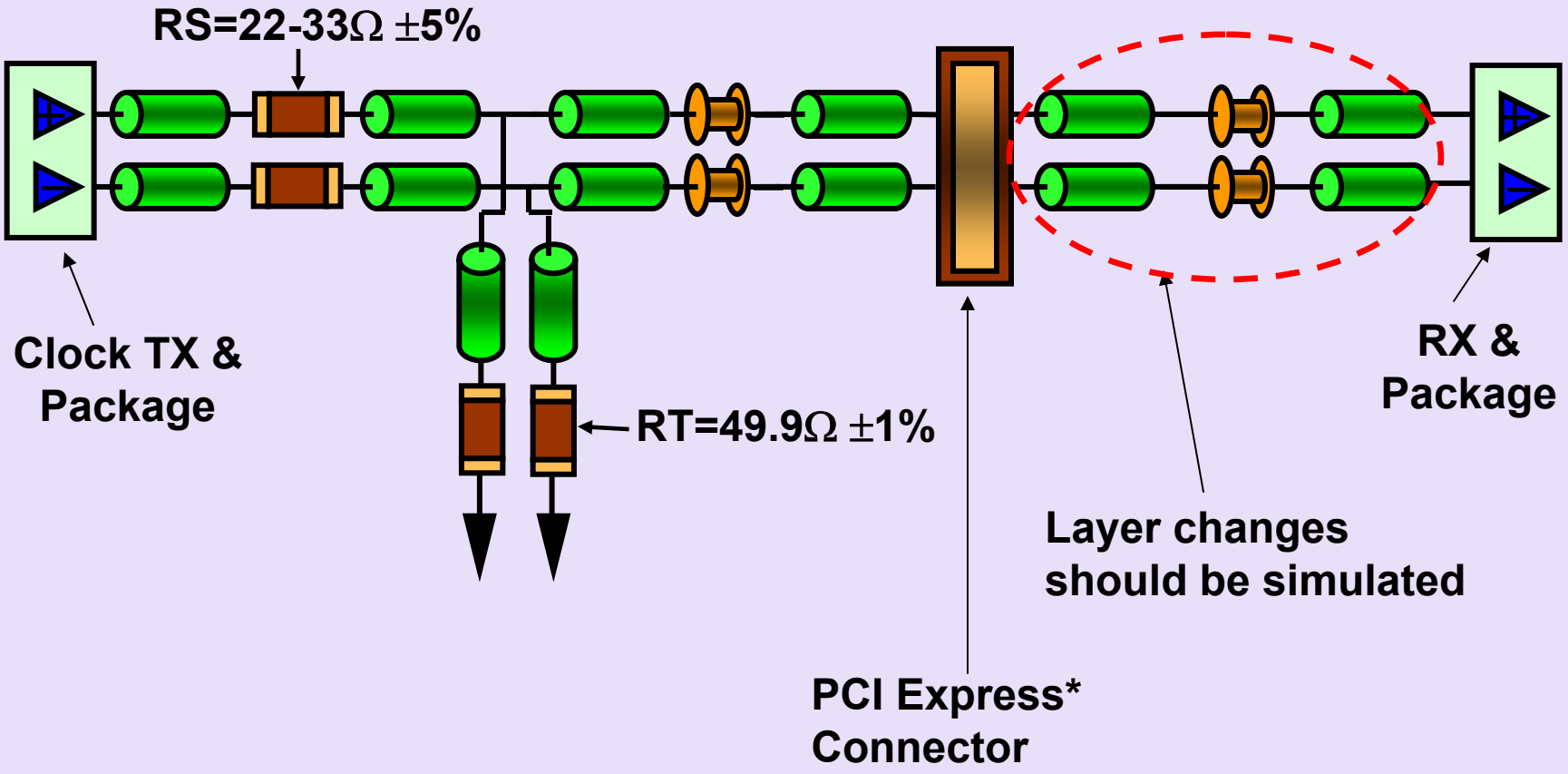
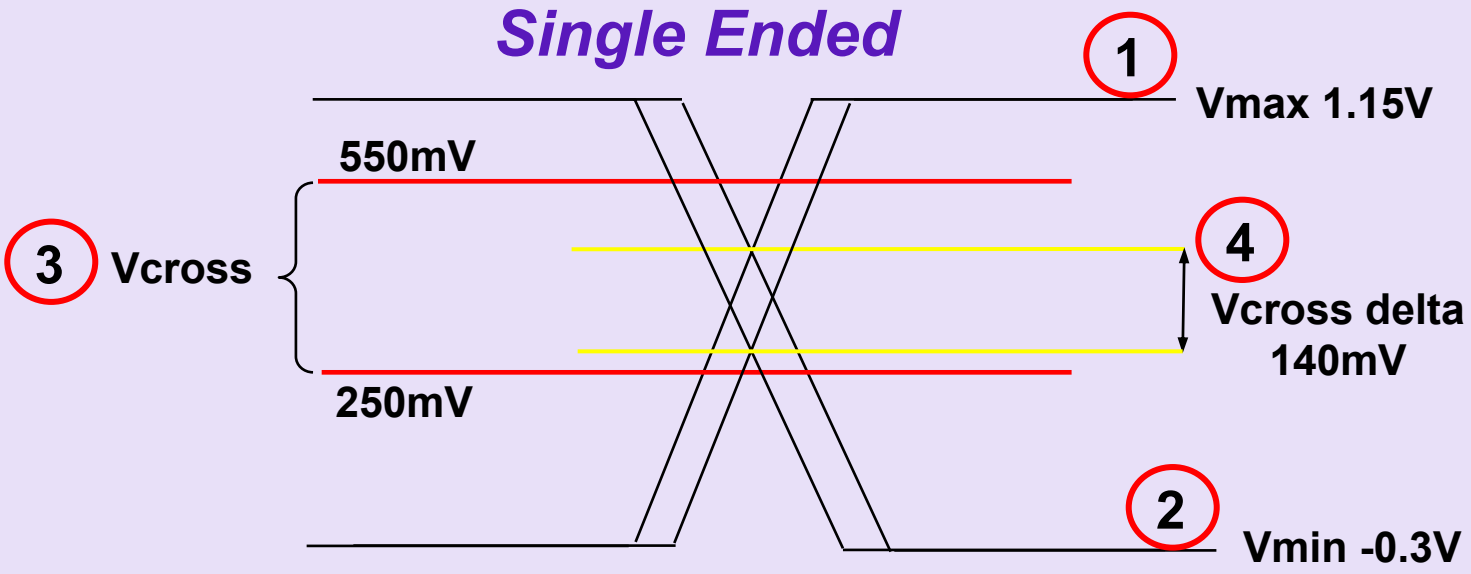
REFCLK Topology

- REFCLK System Topology



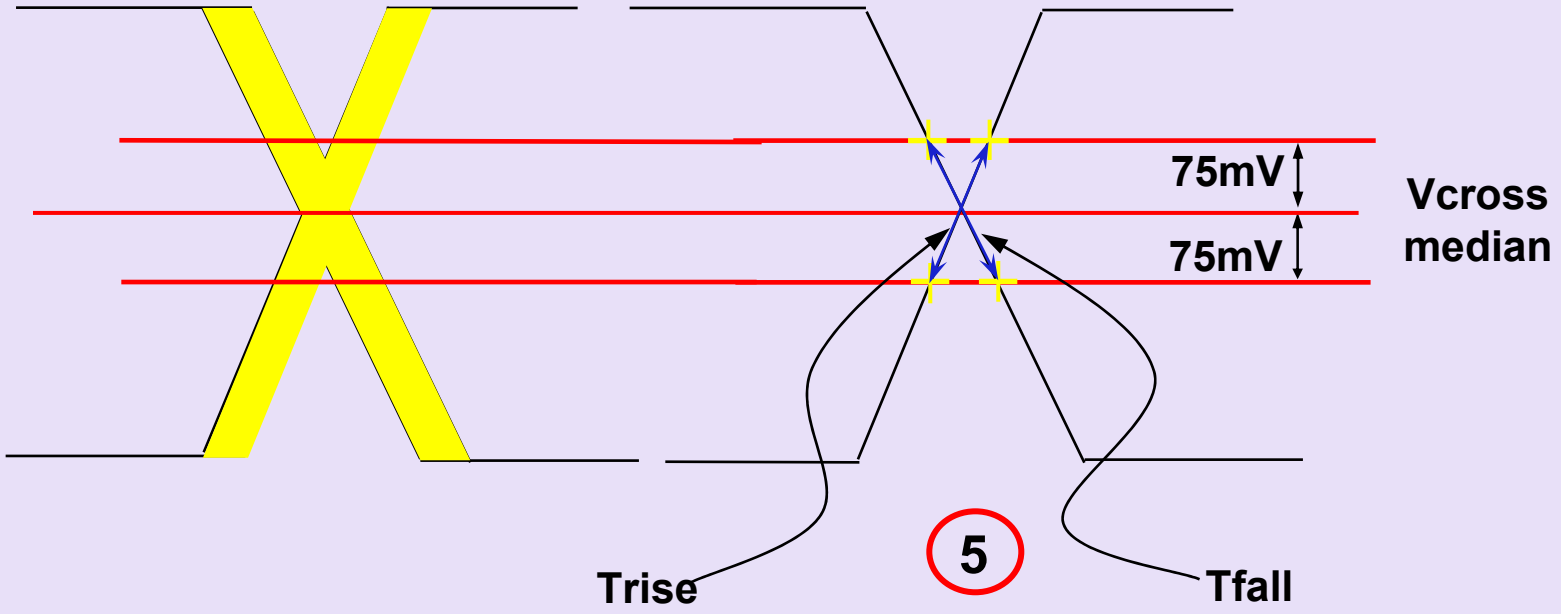
REFCLK Signal Integrity

1. Max overshoot (Clock and Clock#)
2. Min undershoot (Clock and Clock#)
3. Max and Min Clock and Clock# crossing voltage
4. Max and Min Clock and Clock# crossing voltage and determine the delta between the two voltages



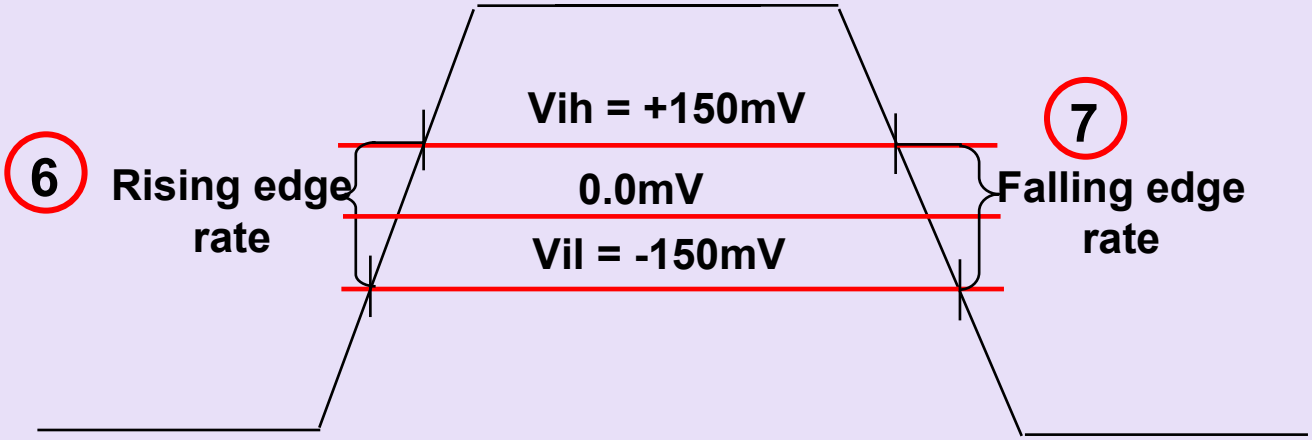
Single Ended Measurements

5. Trise (edge rate) and Tfall (edge rate) match within 20% from Vcross median ±75mV
   - ✓ Find Vcross median
   - ✓ Calculate rise and fall mismatch for each clock cycle
   - ✓ Report max percentage mismatch



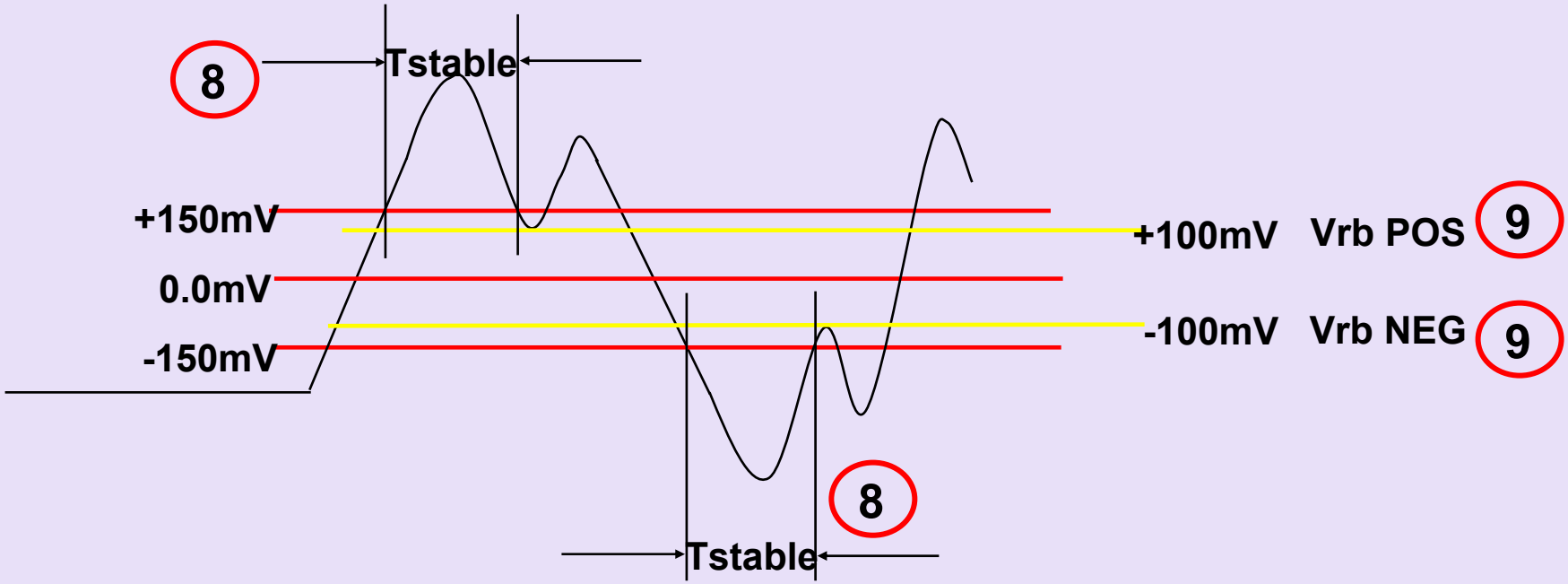
Differential Measurements

- Measure differential edge rates between +150mV and -150mV
  6. Rising edge
  7. Falling edge



Differential Measurements

8. Tstable (500ps) measurement:
   - ✓ After crossing Vih or Vil (rising or falling waveform) signal can not cross Vih or Vil within time Tstable
9. Test for ring back within Tstable
   - ✓ Report worst case ring-back voltage pos and neg



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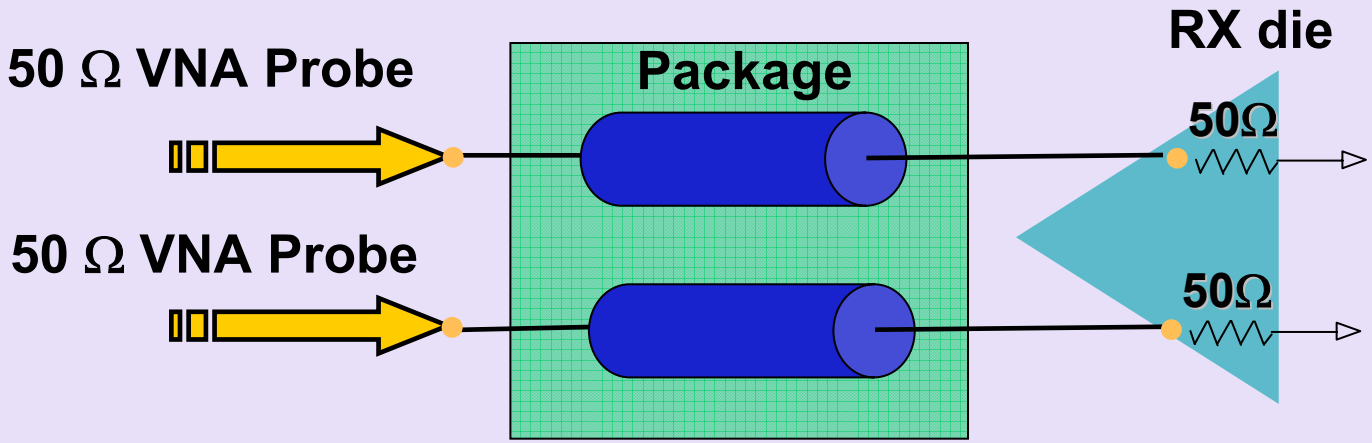
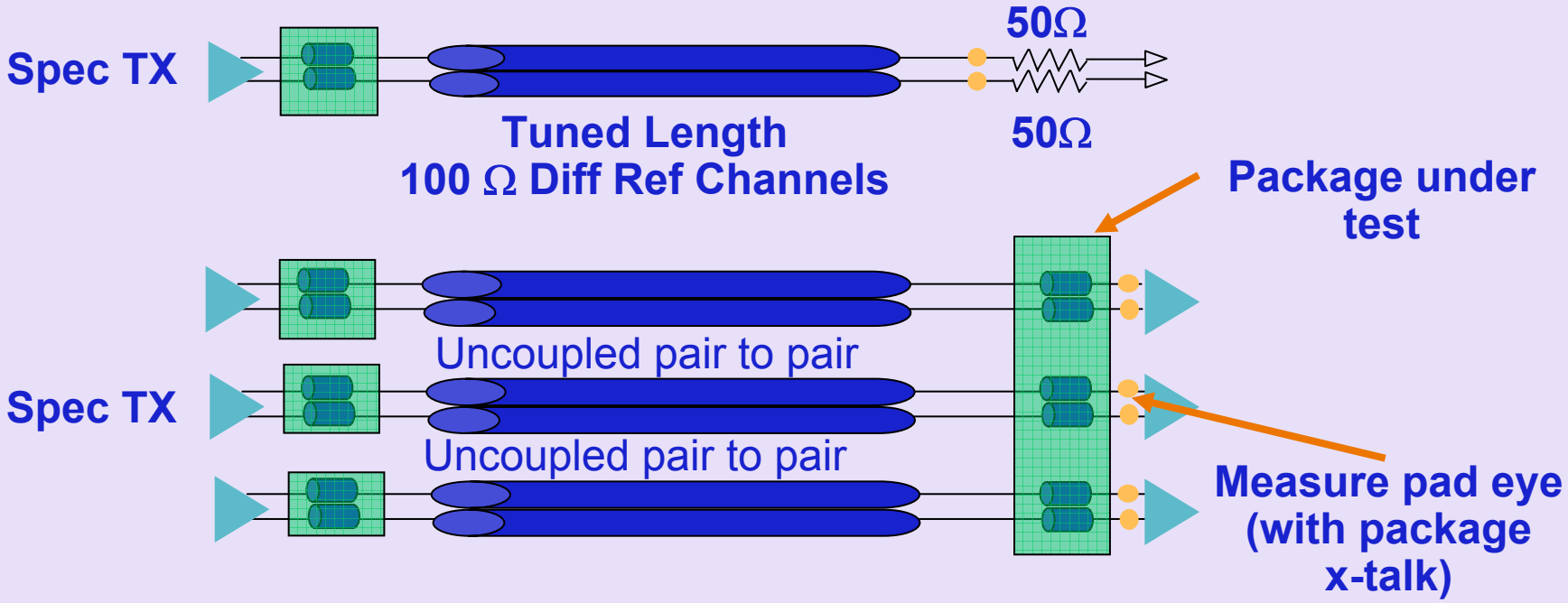
Package Return Loss

- Package performance greatly impacts channel
  - ✓ Return Loss (RL) spec helps to limit package impacts
- Differential RL of -10dB or better required
  - ✓ RL measured at package pins “looking into” device
  - ✓ Use 50 Ω Vector Network Analyzer (VNA)
  - ✓ Die termination (50 Ω) must be enabled



Ref model for RX simulations

- Return Loss is only 1st step for verifying RX
- Use Ref channel model for RX simulations
  - ✓ T-line 13.2dB loss calibrated to 175mV at 50Ω load
  - ✓ Use spec TX (800mV swing, -3.5dB de-emphasis, TX jitter)



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- Run time-domain simulations to design complex topologies
- Use accurate 2D and 3D models for simulations
- Calculate jitter and voltage margins from simulation compliance eye
- Use CEM* System and Add-in Card Compliance Eye Diagrams Specs
- Validate REFCLK signal integrity
- Verify RX design with return loss and reference channel simulations

Collateral

- Intel Developer Network for PCI Express*
  - ✓http://www.express-lane.org/
- Where attendees may get additional and updated information on PCI Express*
  - ✓http://www.pcisig.org

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