PCI Express 3.0 PHY Electrical and CEM Update

Jeff Morriss

Intel Corporation

Disclaimer

- NOTE: The information in this presentation refers to a specification still in the development process. This presentation reflects the current thinking of the workgroup, but all material is subject to change before the specification is released.

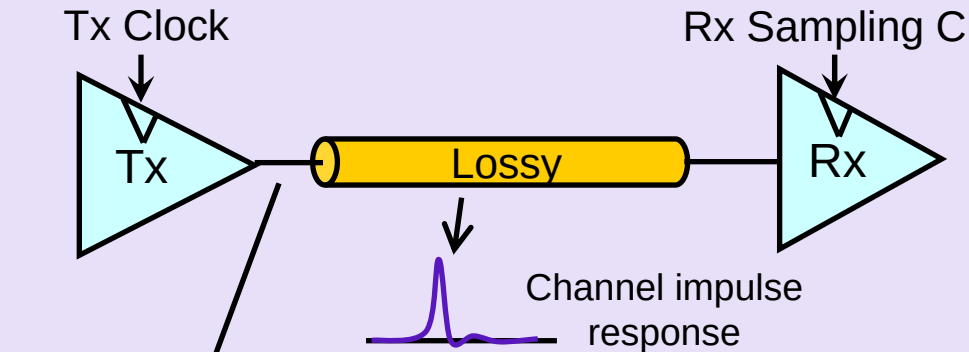
Agenda

- PCI Express* 3.0 Enablers
- Overview of key PCIe specification
  - ✓ Transmitter
  - ✓ Receiver
  - ✓ Channel
  - ✓ Reference Clock
- PCIe 3.0 CEM Requirements and Analysis
- Summary and Conclusions

8GT/s Enablers

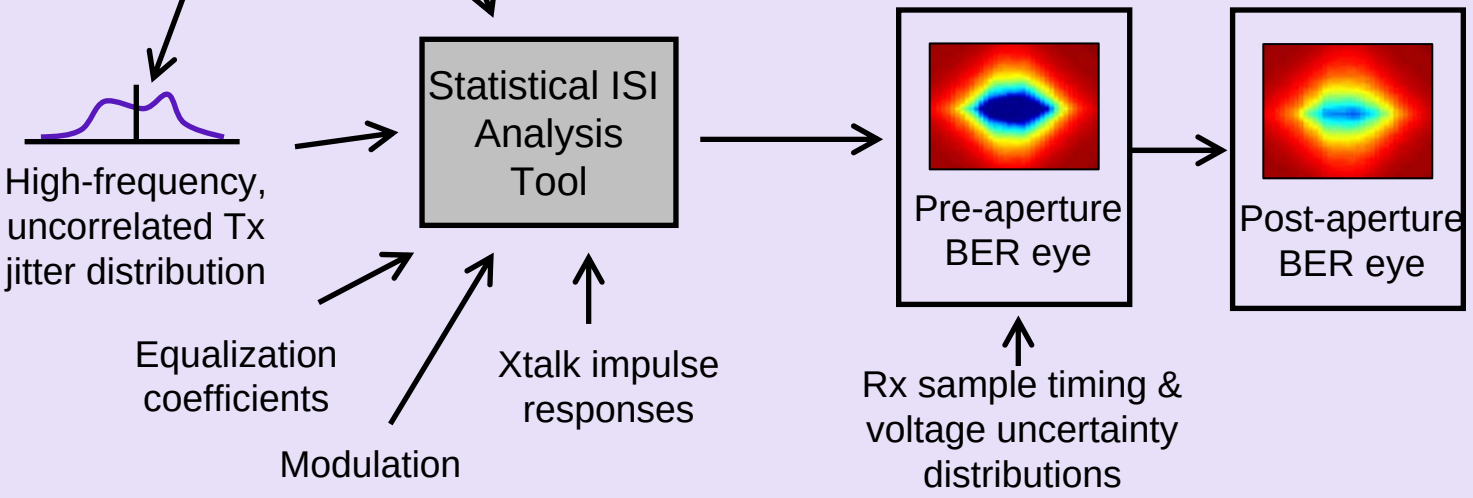
- Reduce conservatism in the 5GT/s specification for system jitter modeling
  - ✓ Use statistical techniques to analyze channel jitter
- Reuse of existing Common Ref Clock is a significant challenge
  - ✓ At 5GT/s Reference Clock jitter consumes significant portion of the timing budget (3.1ps RMS)
  - ✓ Take advantage of increased CDR BW to track most Refclk jitter
- Replace 8b/10b with scrambling to achieve 2x payload @ 8 GT/s
  - ✓ Quantify and minimize DC wander effects
  - ✓ Need to minimize pathologically bad crosstalk
- Tx, Rx Equalization
  - ✓ 3-tap Tx de-emphasis (2.5GT/s & 5GT/s used 2 taps)
  - ✓ Rx equalization is now required
  - ✓ Receiver may train or adapt its equalizers
    - – A low bandwidth feedback channel allows adjustment of the Tx de-emphasis

Statistical System Jitter Analysis



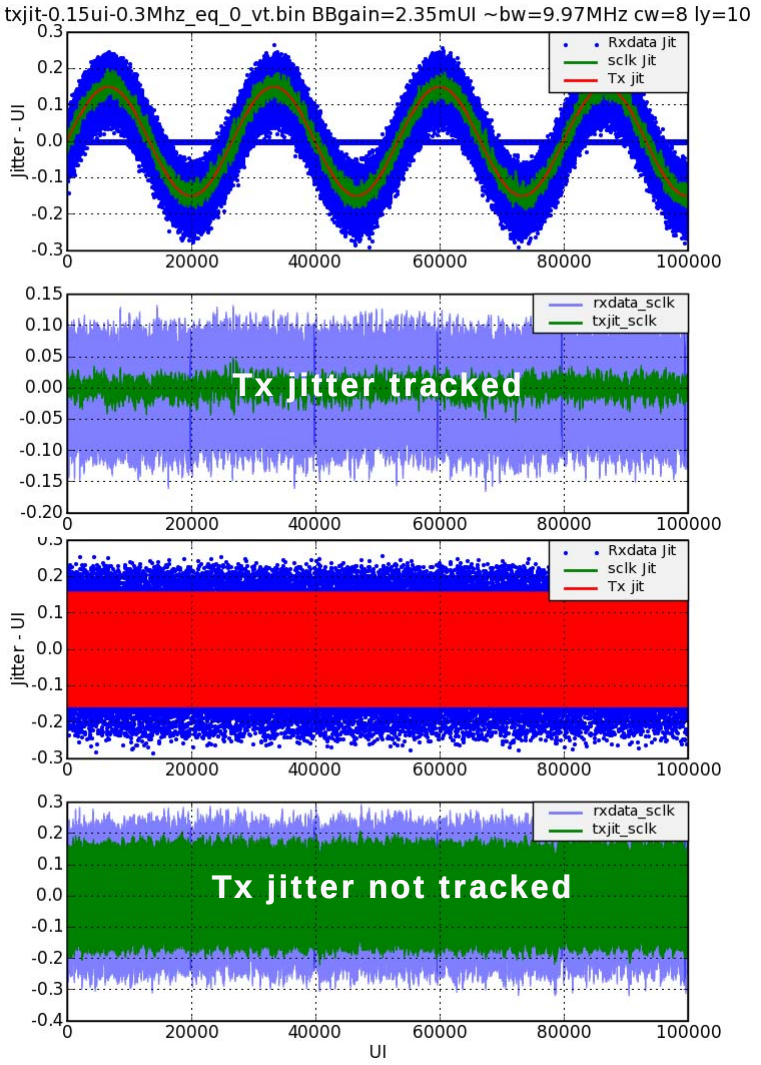
Method relies on LTI characteristics of transmitter, channel and receiver

Impulse response permits superposition of all possible data patterns weighted statistically to capture ISI effects

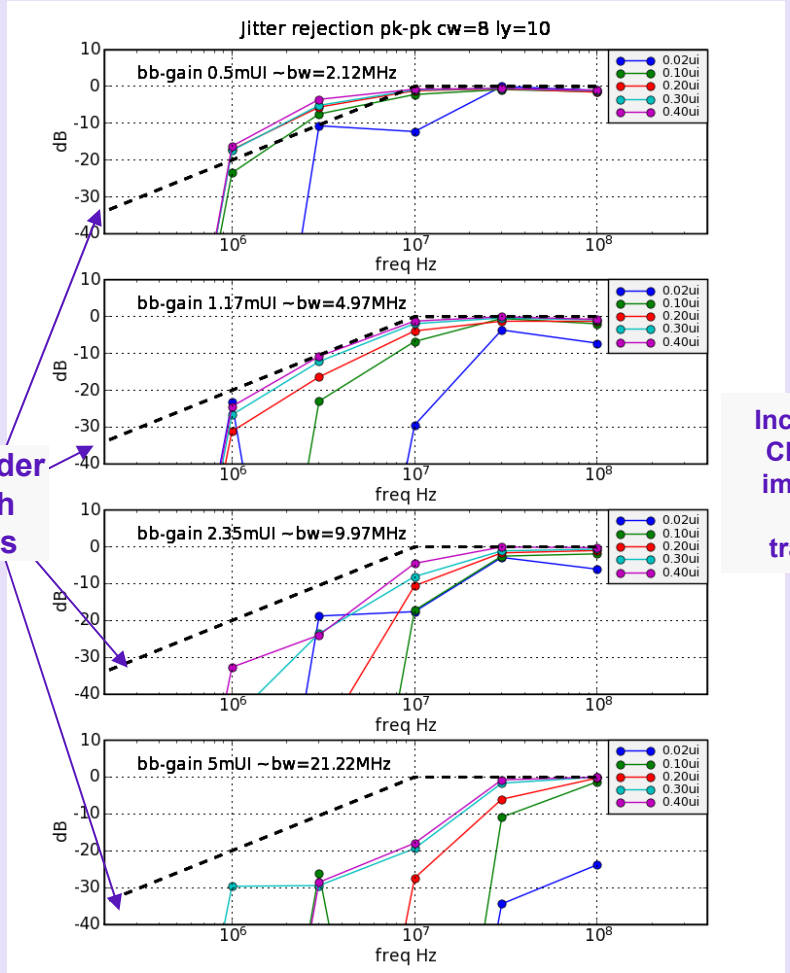


Bang-bang CDR Receiver Tracking

- Goal was to determine if nonlinear CDR behavior can be comprehended by HPF limit
- Step simulator used to generate channel jitter from client PCIe 3.0 channel using random data
- Behavioral bang-bang CDR with varying loop gains used to recover data clock phase
  - ✓ Update width of 8UI plus 10UI latency used in feedback loop
- Step simulator Tx is phase modulated with a sinusoid from 300kHz to 100MHz with different amplitudes
- Sample clock to data jitter extracted
  - ✓ TJ=1–eye_width
- Jitter rejection calculated from ratio of pk-pk increase in sample clock to data jitter versus the applied Tx jitter



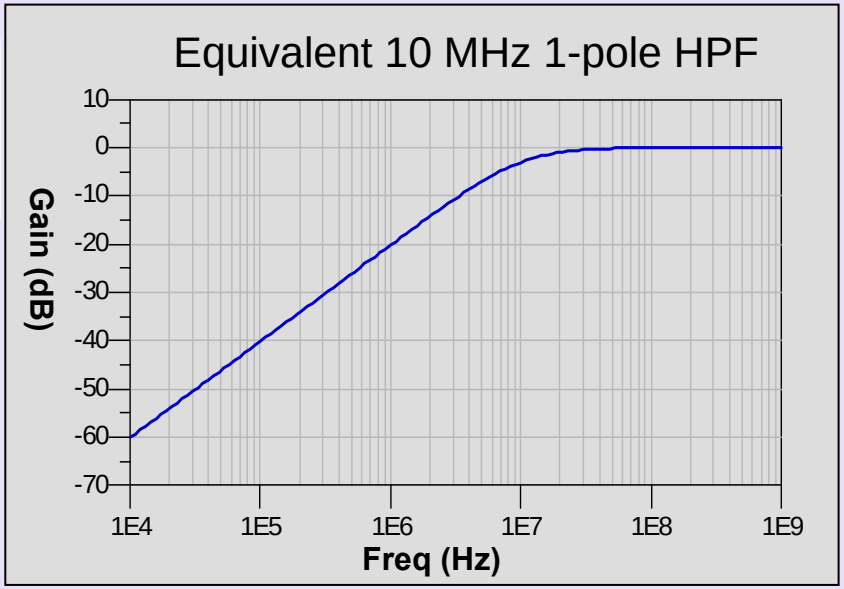
CDR Response to Sinusoidal Jitter



1st order high pass

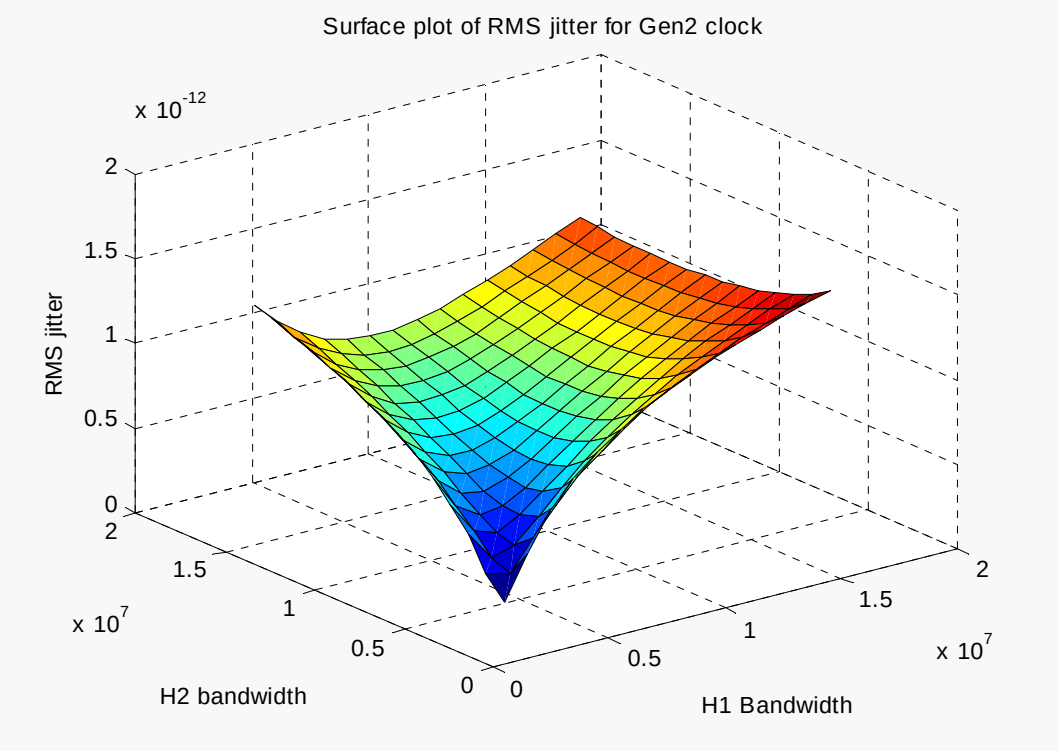
Increasing CDR BW improves jitter tracking

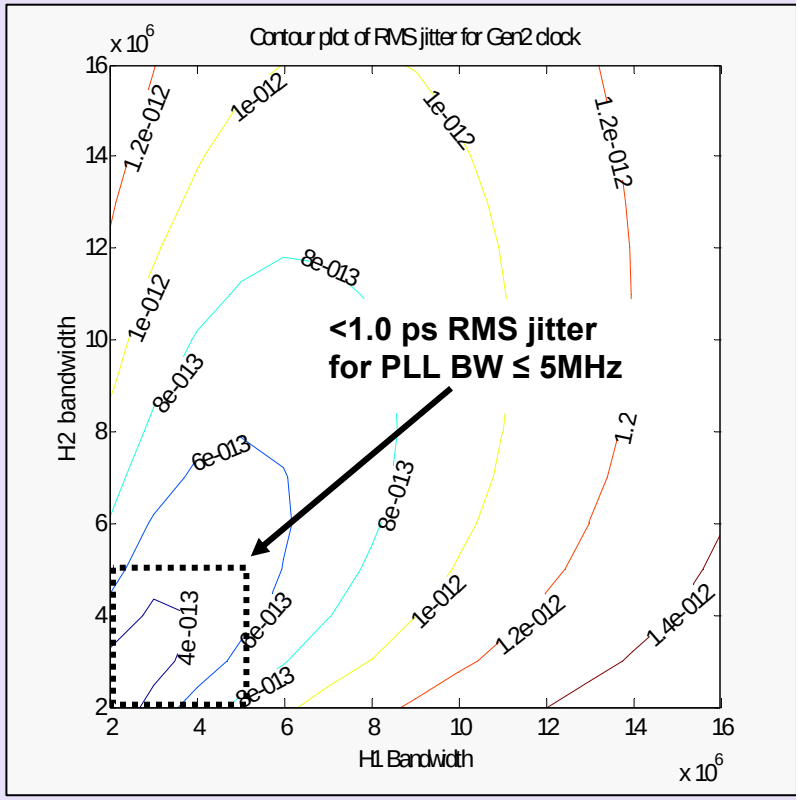
Despite its non-linear behavior, a CDR can be conservatively approximated by a first order high pass filter



Reference Clock Jitter For Marginal 2.0 Refclk Component

- Filter characteristics
  - ✓ 10 MHz H3 (3.0 target)
  - ✓ Sweep PLL bandwidths 2-16 Mhz. 1.5 dB Peaking
    - 12ns of delay lumped onto H2 transfer function



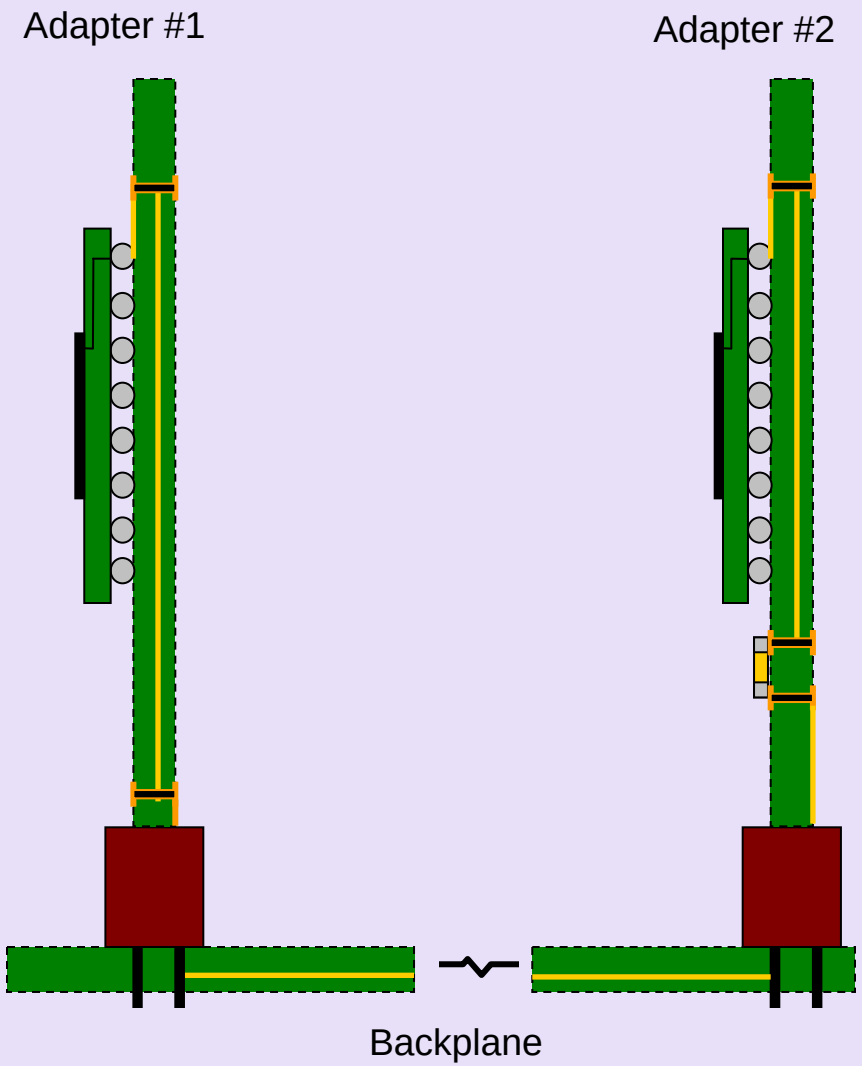


DC Wander and Crosstalk

- DC wander is an unavoidable consequence of replacing 8b/10b coding with scrambling
- Analysis was done using prbs23 polynomials with different # of taps and tap locations
  - ✓ 23 bits is a good tradeoff between DCW and randomness
  - ✓ DCW improved by spec'ing series caps at 220nf ±20%
  - ✓ Range of DC wander: 2.3 mVP vs. 6.0 mVP
  - ✓ Best polynomial: $x^{23} + x^{21} + x^{18} + x^{15} + x^{7} + x^{2}$ yields 2.3 mVP
- To gain maximum statistical relief from crosstalk the data pattern between lanes needs to be uncorrelated
  - ✓ De-correlating the crosstalk between lanes can be achieved by introducing a starting offset into the PRBS used for each lane
  - ✓ It is sufficient to have 8 different offsets that can be repeated in a 16 lane link

Identifying Worst Case Channels

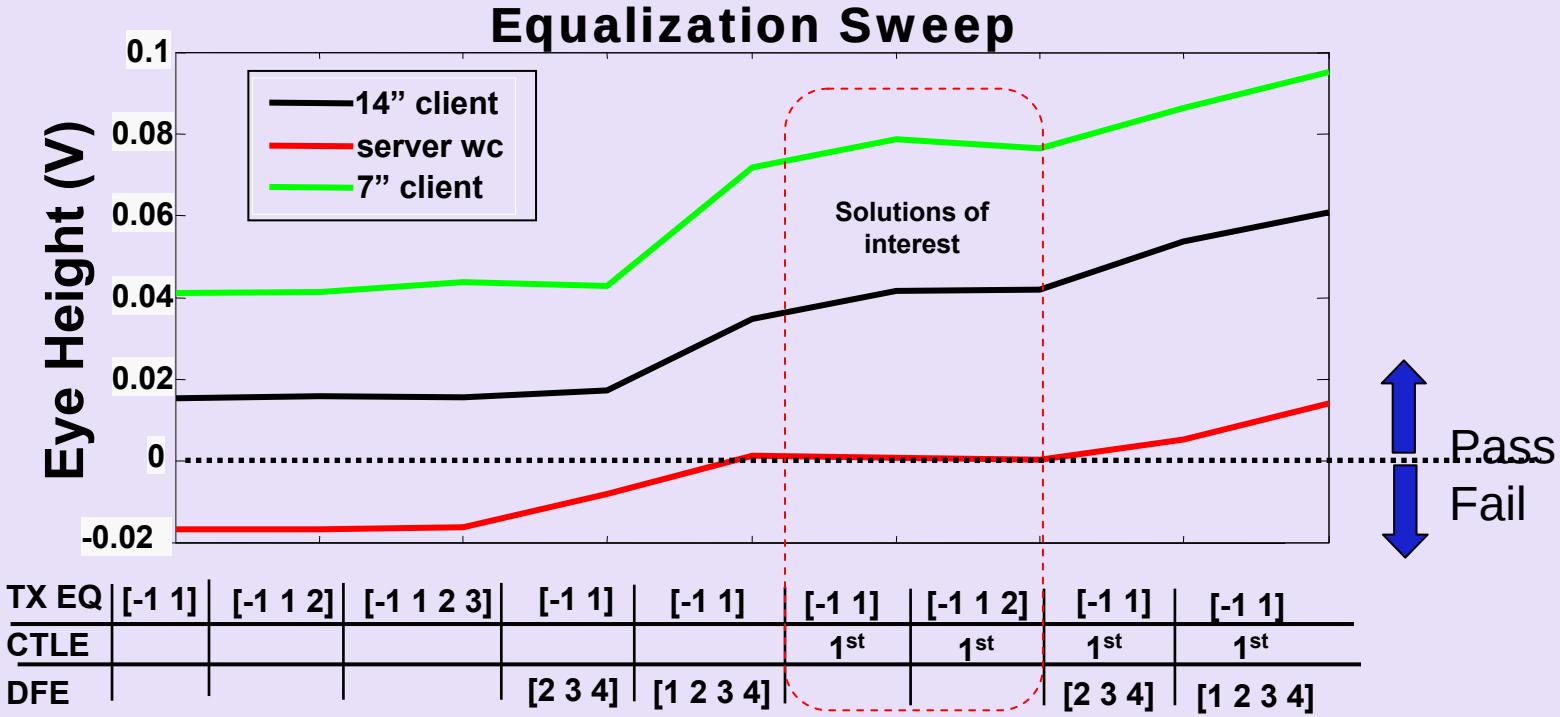
- Medium to long channel
  - ✓ Maximum length ~20”
  - ✓ Can have 1 or 2 connectors
- 6-8 layer PCBs, routing densities make via stubs more common
- Longer lengths reduce end-end reflection
  - ✓ Large discontinuities near devices can still create significant tail ripple
- Difficult to find very worst case channel because of large number of variables



Tx and Rx Equalization

- Analysis indicates that both Tx de-emphasis and Rx equalization are required for max loss channels
- Solution space analysis considered multiple combinations of Tx and Rx analysis
  - ✓ 2 or 3 taps of Tx de-emphasis
  - ✓ Rx CTLE and/or up to 4-tap DFE
- Minimum Rx equalization defined as 1st order CTLE
- Specification defines the following:
  - ✓ Magnitudes and tolerances for pre and post cursor Tx taps
  - ✓ Minimum behavioral Rx CTLE
    - Used for channel tolerancing and Rx stressed eye calibration
  - ✓ Receivers may implement equalization more capable than 1st order CTLE

Margins vs. Equalization Type

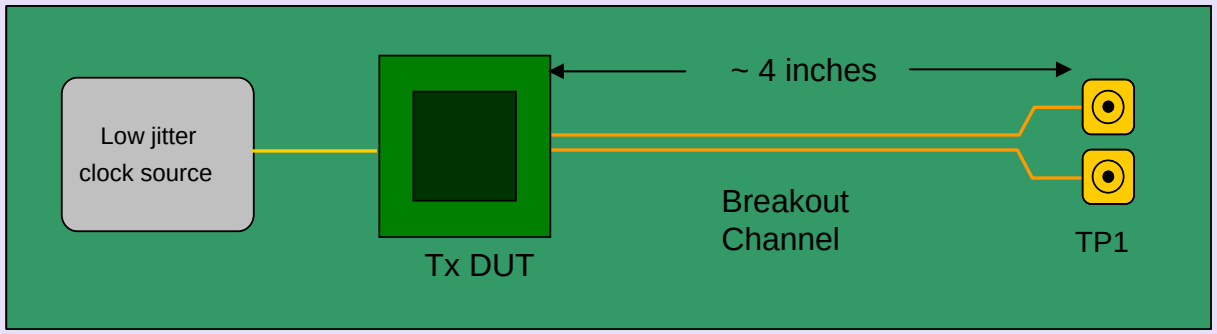


A combination of Tx de-emphasis and Rx LE yields positive margins. Voltage/jitter margins may be increased by use of more complex Rx equalization techniques. DFE may be included if Rx requires additional jitter margin

Transmitter

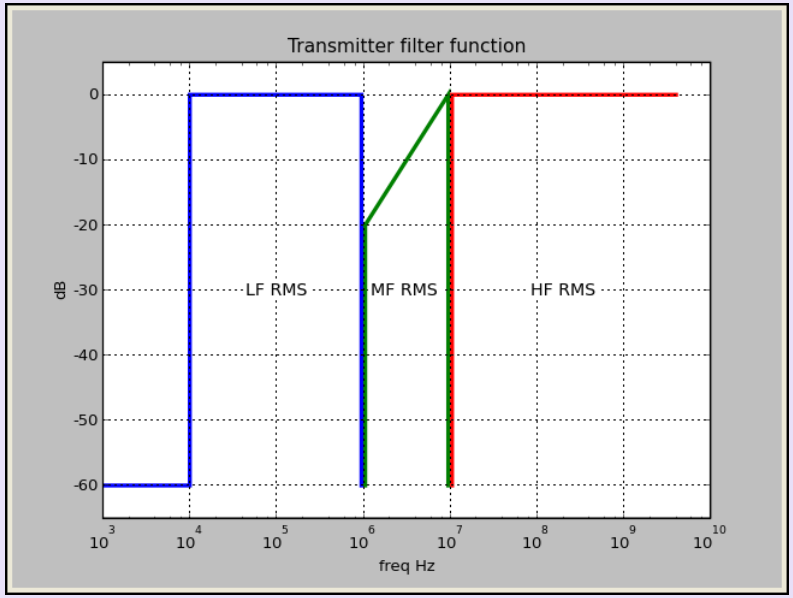
Transmitter Measurement

- The transmitter is measured at end of the break-out channel and this channel may be mathematically extended to match the Tx de-emphasis setting
  - ✓ Transmitter will likely have three fixed settings: -3.5dB, -6dB and -9dB
  - ✓ 0dB de-emphasis will also be required, Tx eye will be measured directly at the end of compliance channel
  - ✓ During training the receiver will be allowed to adjust the Tx de-emphasis in ~1dB steps from its nominally set de-emphasis level
- The frequency domain return loss measurement will be replaced with a time domain method
  - ✓ Favored approach is to construct a cumulative reflected voltage plot with a 1UI timebase whilst applying a random data pattern
    - Captures interaction between package flight time and pin and pad capacitance

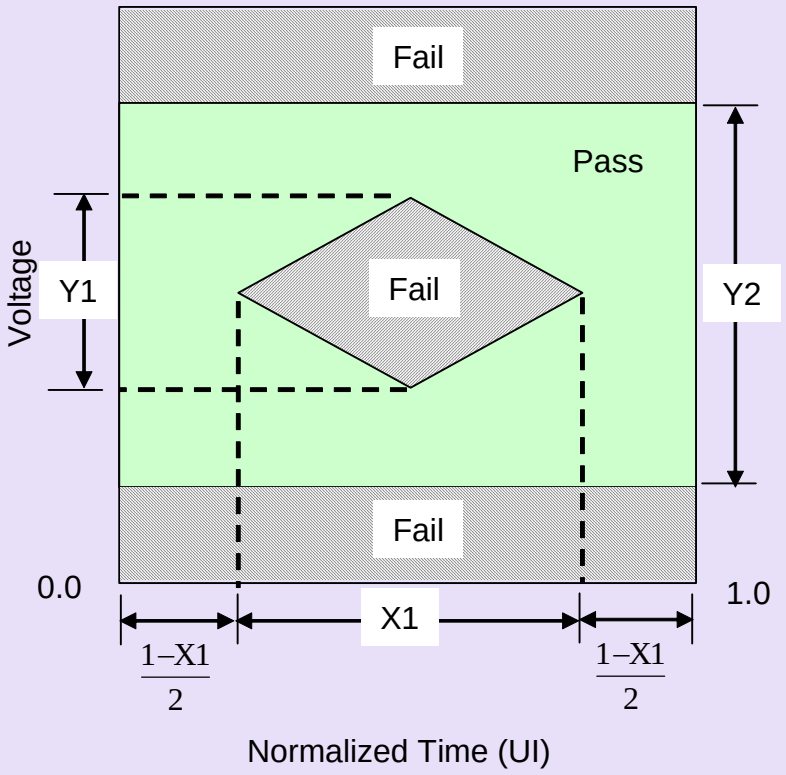


Transmitter Phase Jitter Filtering

- Split into 3 bands
  - ✓ LF RMS (10kHz-1MHz) similar 5GT/s
  - ✓ MF RMS (1MHz-10MHz) filtered with 20dB/dec high pass
  - ✓ HF RMS (>10MHz) similar to 5GT/s
- MF band takes advantage of Rx CDR rejection
  - ✓ Allows significantly more Tx eye closure at 1MHz
  - ✓ Provides relief for non-LC based PLL's
- LF and HF bands combined into the budget as per 5GT/s
- MF band RSS'd with refclk MF jitter sources



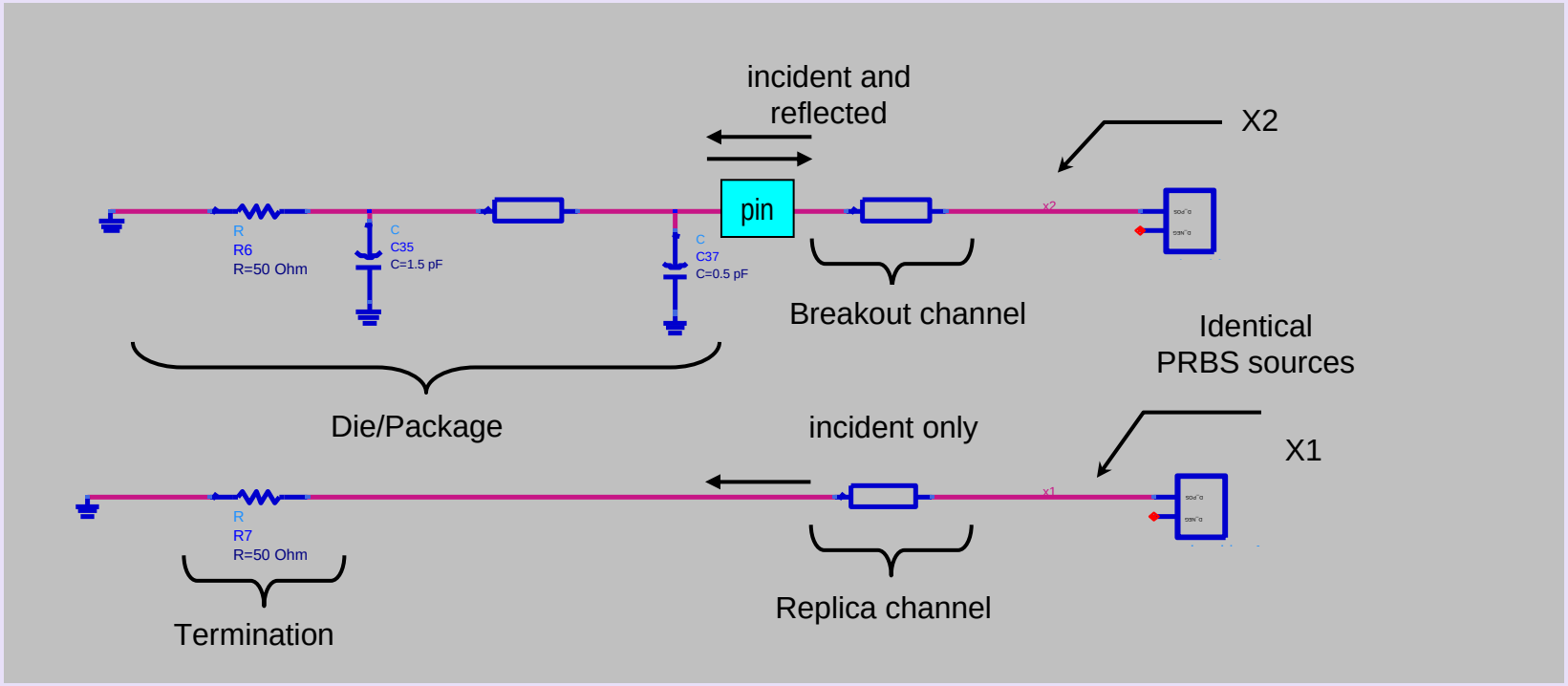
HF Tx Parameters



Symbol	Parameter	8.0 GT/s	Units	Comments
$V_{TX-EYE-FULL}$	Y2	1200 (max)	mVPP	Outside eye voltage
$V_{TX-EYE-HALF}$	Y2	800 (max)	mVPP	Outside eye voltage
$V_{TX-EYE-FULL}$	Y1	TBD	mVPP	Note 1
$V_{TX-EYE-HALF}$	Y1	TBD	mVPP	Note 1
$T_{TX-EYE-FULL}$	X1	TBD	ps	Note 2
$T_{TX-EYE-HALF}$	X1	TBD	ps	Note 2
$RL_{TX-DIFF}$	Differential return loss	TBD	TBD	Note: return loss parameter is a place holder
RL_{TX_CM}	Common mode return loss	TBD	TBD	Note: return loss parameter is a place holder
$T_{TX-PW-RJ}$	Pulse width distortion	TBD	ps RMS	Measured over 1 UI as rising to falling edge or falling to rising edge. Note 3

The Rev 0.7 spec will assign values to the TBDs in the table

RL Measurement Using Replica and Breakout Channels



Proposed specification format for Tx, Rx reflected voltage

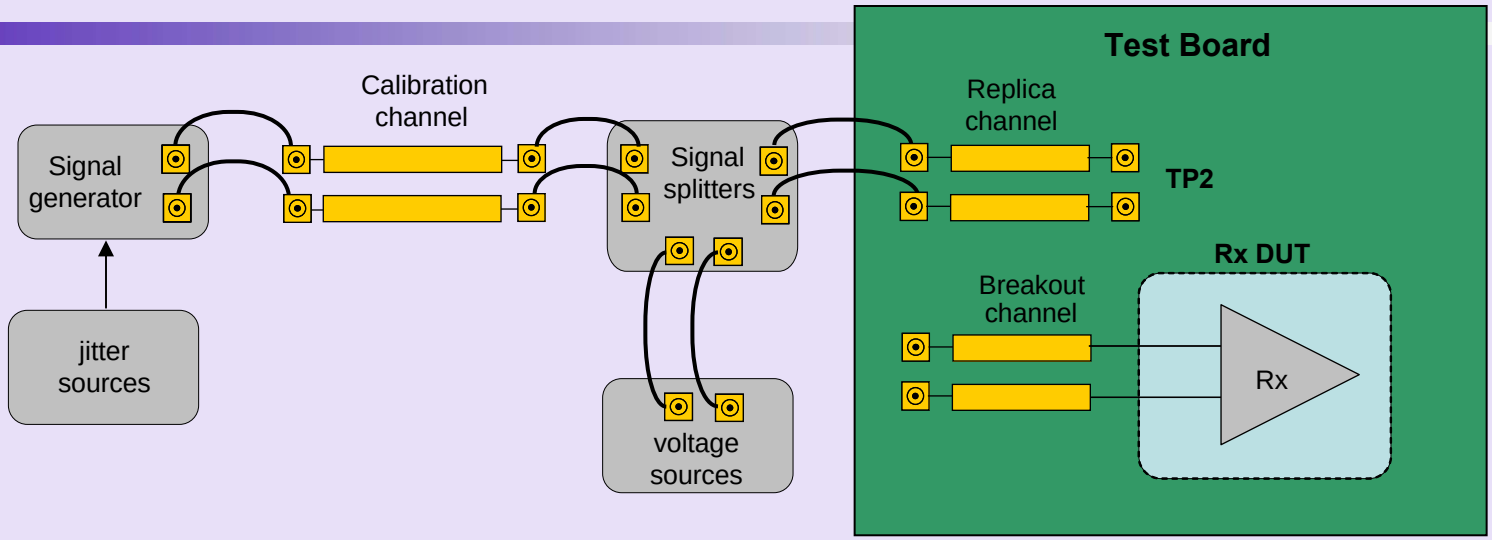
$VREFL_{DIFF}$	Reflected Tx differential voltage	TBD	% Pk	$V_{X2DIFF} - V_{X1DIFF}$ measured at end of breakout channel as a percentage of the launch voltage
$VREFL_{CM}$	Reflected Tx common mode voltage	TBD	% Pk	$V_{X2CM} - V_{X1CM}$ measured at end of breakout channel as a percentage of the launch voltage

Receiver

Receiver Testing Methodology

- As with 2.0, PCIe 3.0 receivers are tested using a stressed eye approach
  - ✓ Worst case voltage and jitter are applied to the DUT, which must meet BER
- PCIe 3.0 Enhancements wrt. PCIe 2.0
  - ✓ Stressed eye parameters are calibrated as they would appear at pins of DUT
    - Use of replica channel permits accuracy without de-embedding
  - ✓ Jitter is partitioned into LF, MF, and HF components
  - ✓ ISI generated by combination of calibration channel and FIR capabilities of generator
  - ✓ Reference equalization algorithm is required to see an open eye at calibration plane

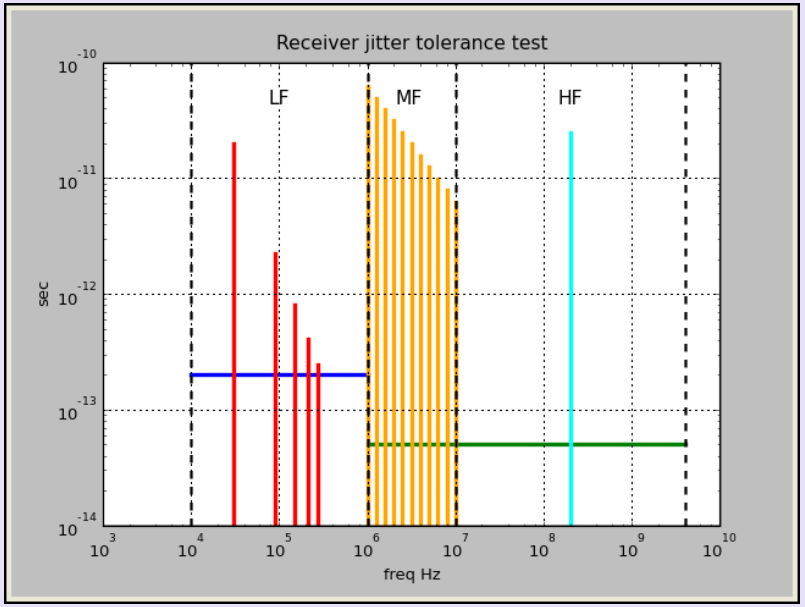
Receiver Tolerancing



- Receiver behavioral equalization
  - ✓ Minimum of first order CTLE
- Tolerancing approach similar to PCIe 2.0
  - ✓ Pass/fail requirement in term of BER with worst case input signal.
  - ✓ Precisely defined compliance channel(s) to inject ISI
  - ✓ Calibration done at output of signal generator (add setup picture)
- Jitter Injection
  - ✓ Low frequency (10 kHz – 1 MHz)
  - ✓ Mid frequency (1 – 10 MHz)
  - ✓ High frequency (10 MHz – 1 GHz)
- Voltage Injection
  - ✓ Common mode (Power supply noise)
  - ✓ Differential mode (crosstalk)

Jitter Injection for Rx Tolerancing

- To be able to rely on the receiver to follow a first order CDR high pass, we need to test its response
- We can add a jitter tolerance test that phase modulates the data source and sweeps the frequency
  - ✓ Voltage waveform generated like PCIe 2.0 with a calibration channel to generate ISI
- At high frequency (>10MHz) two sinusoids are calibrated to create a limit stressed eye as in PCIe 2.0
  - ✓ Use a variable and fixed frequency
  - ✓ 10MHz ~0.04UI pk-pk (5ps) + 200MHz ~0.2UI
- Variable frequency sinusoid is then swept to a lower frequency increasing its amplitude from 10MHz to 1MHz at 20dB per decade
  - ✓ 1MHz ~0.4UI pk-pk (50ps) + 200MHz ~0.2UI

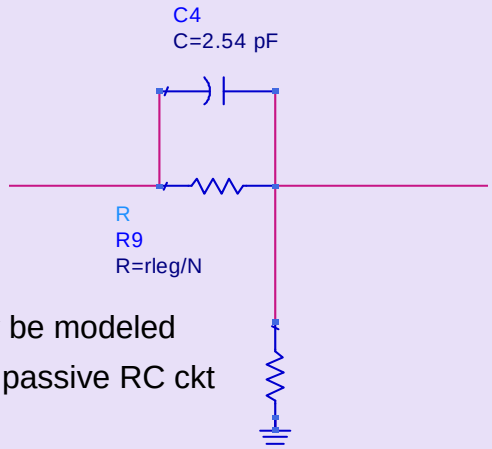


Key:
RED: residual SSC
BLUE: LF RMS
GREEN: HF RMS
ORANGE: MF sinusoidal
CYAN: HF DJ

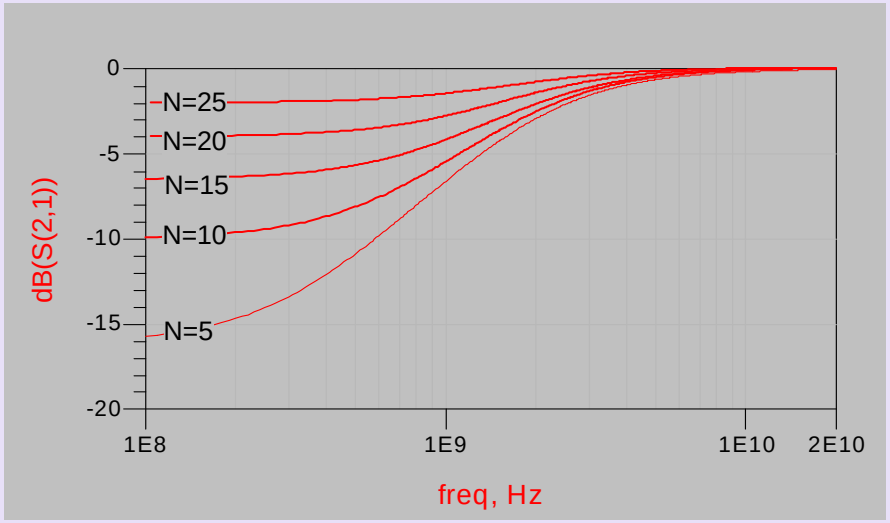
N.B. Only one MF spur applied at a time

Linear Receiver Equalization

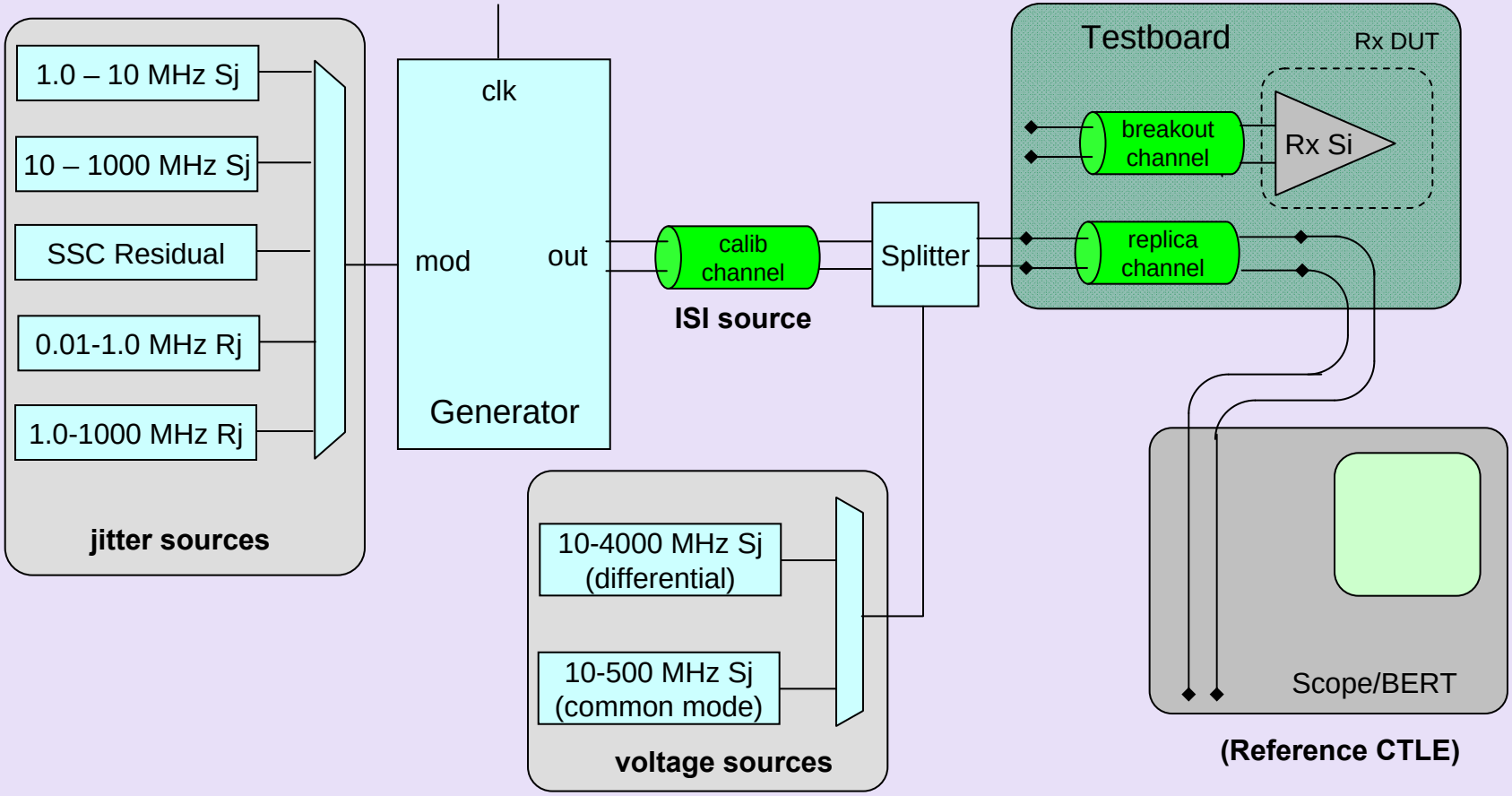
- The reference equalizer represents minimum Rx requirements to guarantee interoperability
  - ✓ Defined by a simple passive transfer function
  - ✓ DFE provides significantly better margins for the Rx and is expected to be used in many implementations
- Minimize number of parameters that need to be adjusted
  - ✓ AC vs. DC gain from K_{AC-DC} 0-16dB in ~1dB steps
  - ✓ Parameter adjustment must be as good as, but no better than, actual receivers
  - ✓ Example below shows 5-bit resolution achieved with 32 switched resistors.



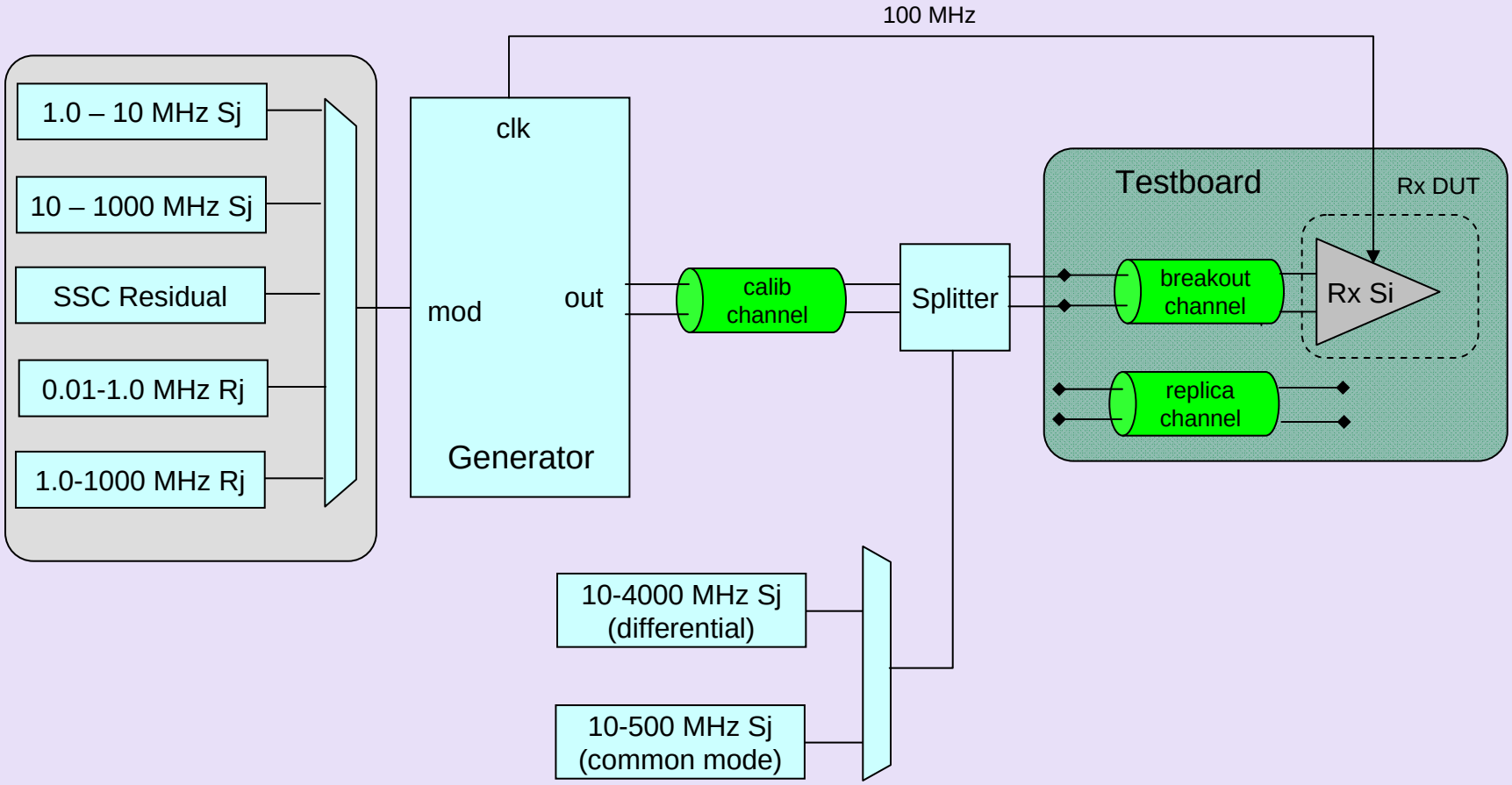
CTLE may be modeled as simple, passive RC ckt



Calibrating into scope
(Common Refclk arch)



Tolerancing Rx under test
(Common Refclk arch)



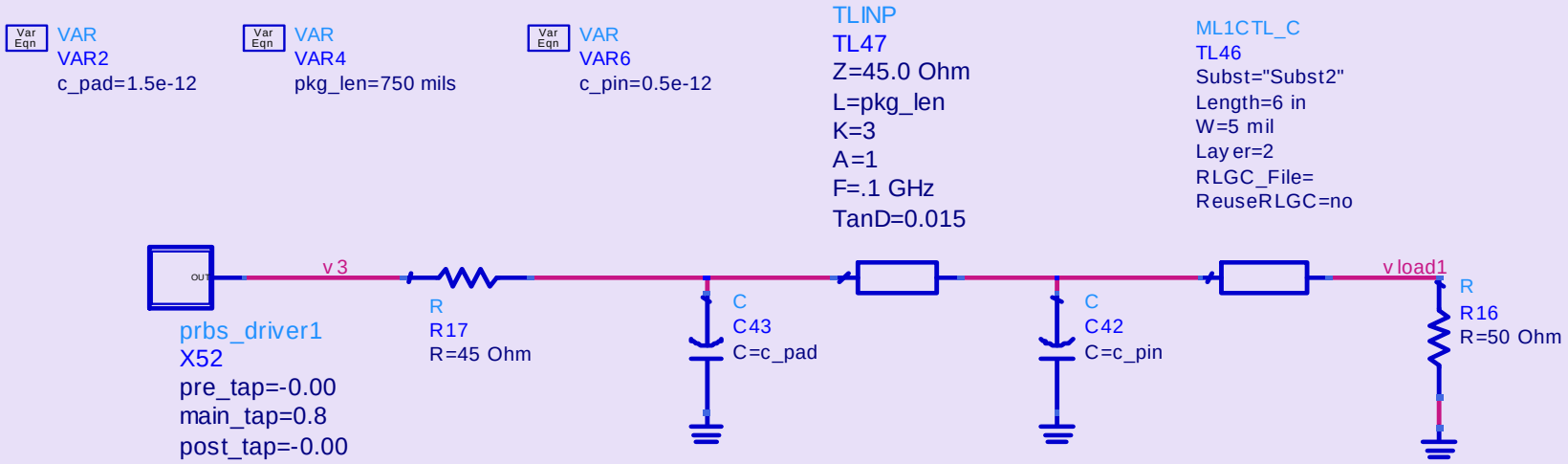
Channel Tolerancing

Channel Compliance

- To ensure adequate system margins it will be necessary to define a channel compliance methodology
  - ✓ Objective is create a uniform method to qualify a system channel for operation at 8GT/s
- To get unambiguous results the methodology has to measure eye margin at the die pad
  - ✓ Requires a behavioral package models for Tx and Rx
  - ✓ Simulate from Tx die pad to Rx die pad (with behavioral Rx eq.)
  - ✓ Package model has to be correlated to device measurements
- A behavioral Tx and Rx is required that performs no better than a marginally compliant Tx and Rx
  - ✓ The behavioral models need to be calibrated against the real device Tx and Rx measurements
- A statistical simulation is used to correctly convolve all jitter contributions
  - ✓ Convolves random and DJ-dd terms together

Behavioral Package Model

Channel tolerancing requires that worst case package and die parasitics be included in simulation



Package is defined by C_{PIN}, C_{PAD}, length, Z_0, conductivity, and tan(d).

For subsequent simulations C_{PAD} = 1.5 pf, C_{PIN} = 0.5 pf, Z_0 = 45Ω, and length swept from 200 – 1600 mils

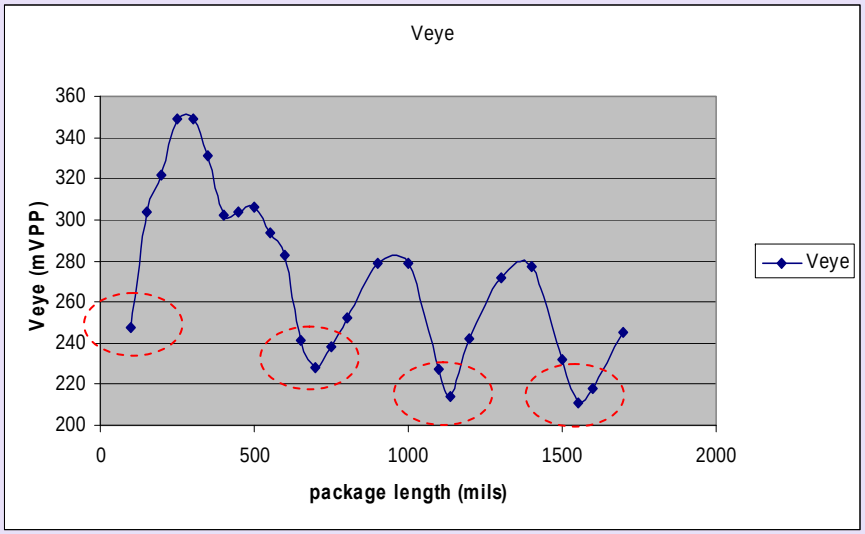
Identifying Worst Case Tx Packages

Packages typically contain impedance discontinuities causing interactions with the package itself plus with the channel.

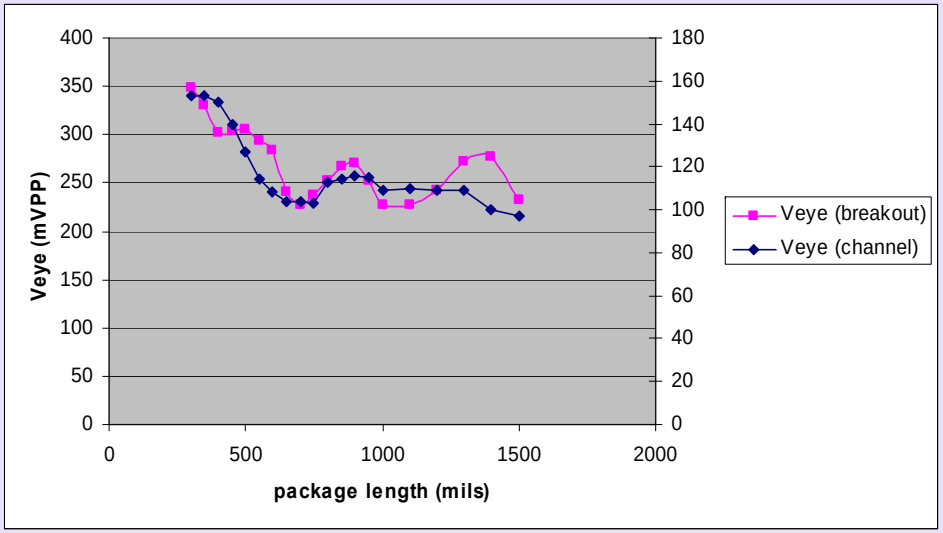
However, the locations of V_{EYE}(min) are well defined and correspond to package lengths corresponding to flight times of N UI.

Therefore it is possible to identify a small number of package configurations that constitute worst case.

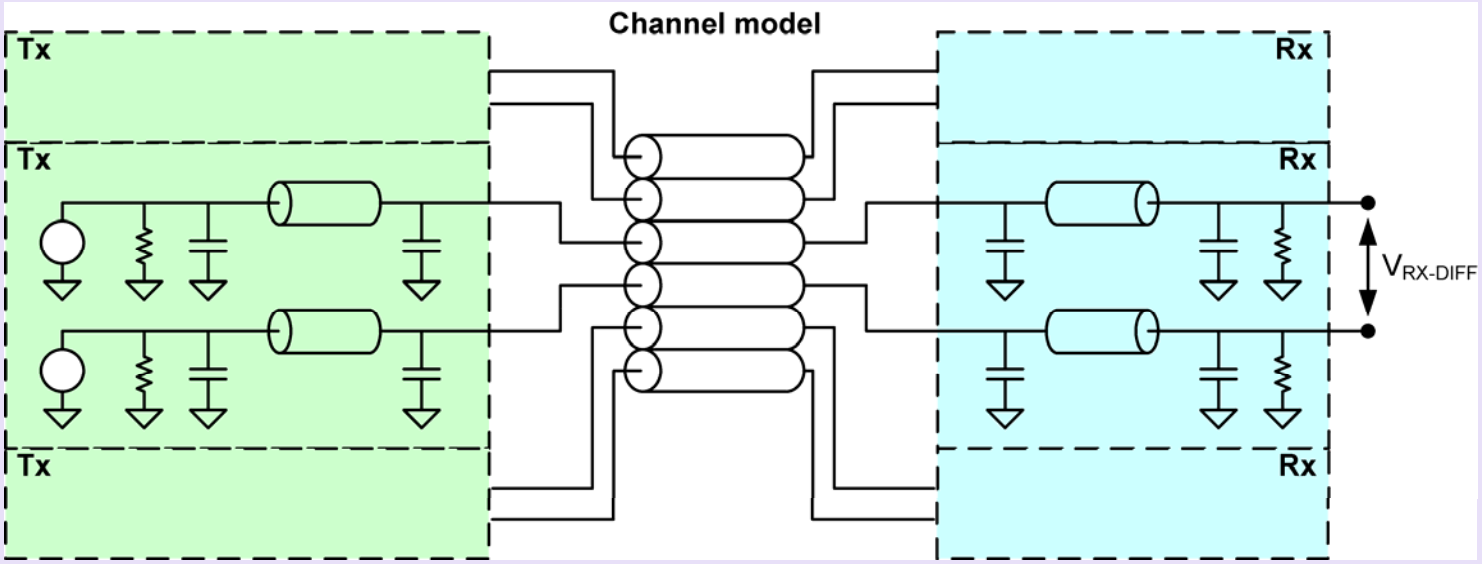
Package model only



Correlation between package and package plus breakout channel



Channel compliance modeling
(putting all the pieces together)

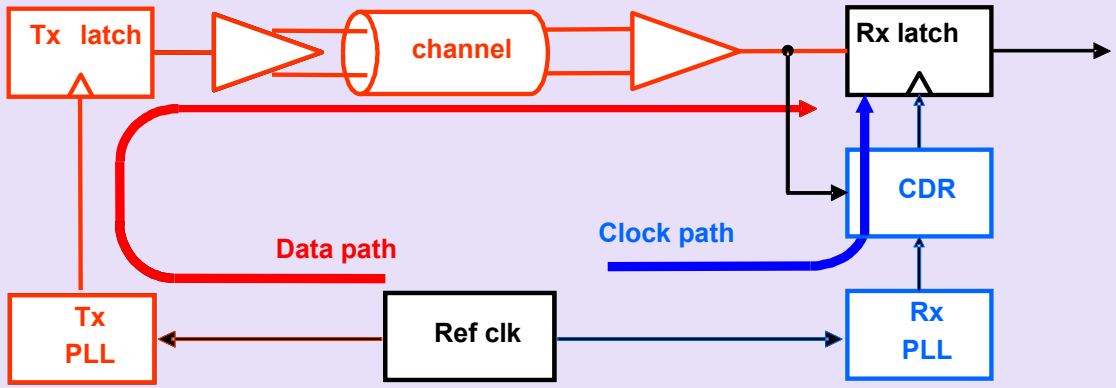


- Tx die pad waveform includes de-emphasis and jitter
  - ✓ Tx plus package calibrated to meet Tx spec
- Tx and Rx packages are modeled as a ‘pi’ network
  - ✓ Cpin, Cpad, Zpkg, Tpkg define behavioral package
  - ✓ Worst case package model found by sweeping package parameters
  - ✓ Package is not coupled, package crosstalk is modeled as additive noise
- Channel model represents system pin-pin model
  - ✓ From field solver or pin-pin measurement
  - ✓ At least 3 coupled pairs to capture crosstalk
- Network is statistically simulated to meet differential eye opening at Rx die-pad
  - ✓ Pass criteria at die pad determined by calibration of Rx package against Rx spec

Reference Clock

Reference Clock

- Same usage model as PCI Express* (PCIe*) 2.0
  - ✓ Common clock jitter defined by transfer function HT=(H1-H2*delay)*H3
- Challenging area
  - ✓ At 5.0 GT/s Reference clock consumes significant portion of timing budget. (3.1 ps RMS)
- Goal is to use the same reference clock components as used for PCIe 2.0
- Goal for 1 ps RMS effective jitter after CDR bandwidth and PLL bandwidth optimizations.

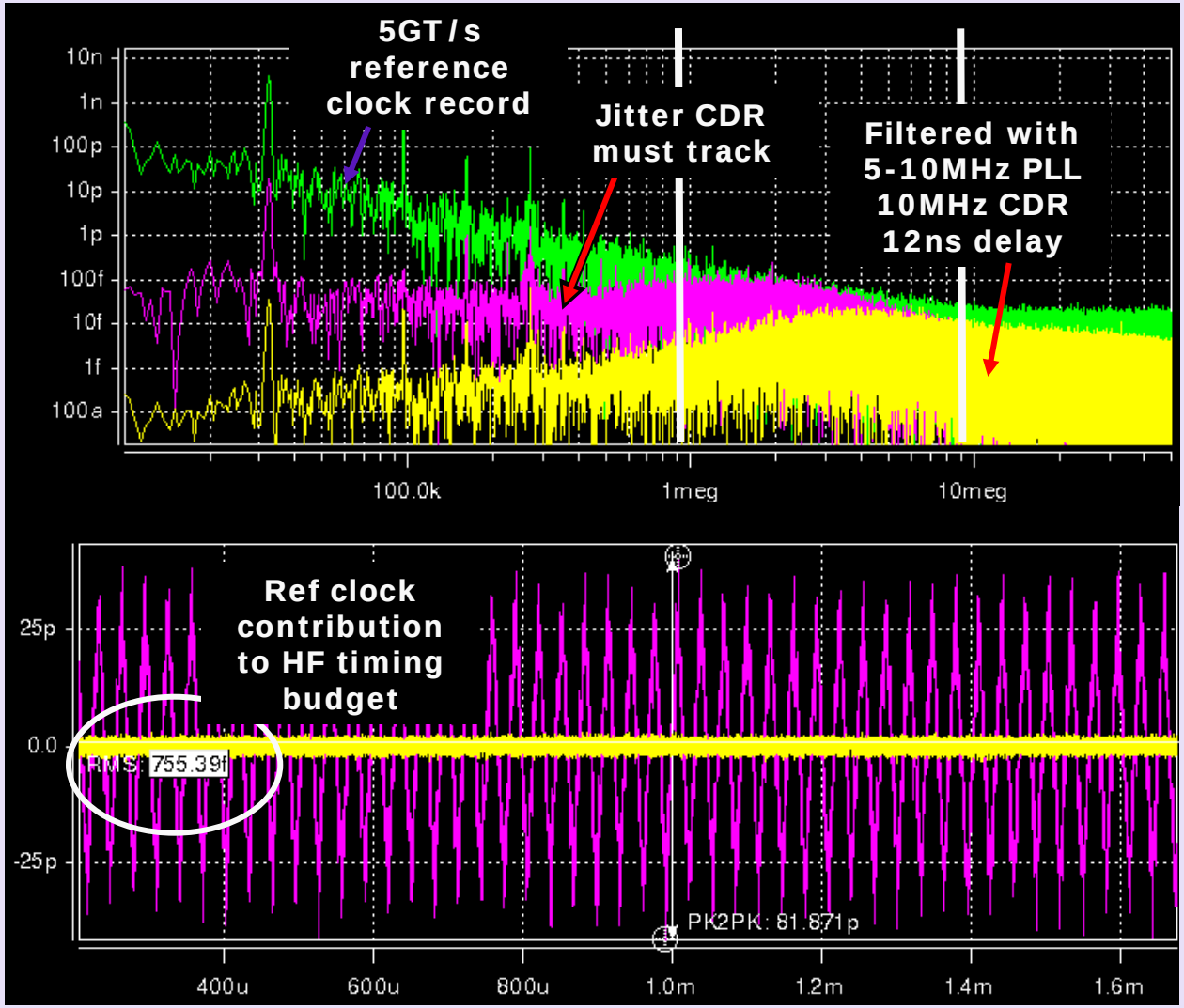


Reducing Sensitivity to Reference Clock Jitter

- Key to solving these problems is to place burden on the Rx CDR
  - ✓ 2.5GT/s and 5GT/s have no specific CDR phase tracking requirements
  - ✓ 8GT/s higher data rate allows CDR bandwidth to be increased
- 8GT/s Rx tolerance testing validates CDR tracking performance
  - ✓ Rx must tolerate 0.35UI of additional sinusoidal eye closure at 1MHz compared to minimum eye opening
- Studies of typical bang-bang digital CDR implementations indicate they can be designed to meet this requirement
  - ✓ Expectation is that existing Rx CDR's can be modified to meet these requirements for 8GT/s

Example: Reference Clock Filtering

- Typical 100MHz 5GT/s reference clock
- Filtered with PLL difference function defined for 2.5GT/s with:
  - ✓ 5-10MHz PLL BW 1dB peaking
  - ✓ 10MHz high pass for CDR
  - ✓ 12ns transport delay
- Will require an additional measurement of reference clock
  - ✓ Expect existing 5GT/s ref clocks will pass

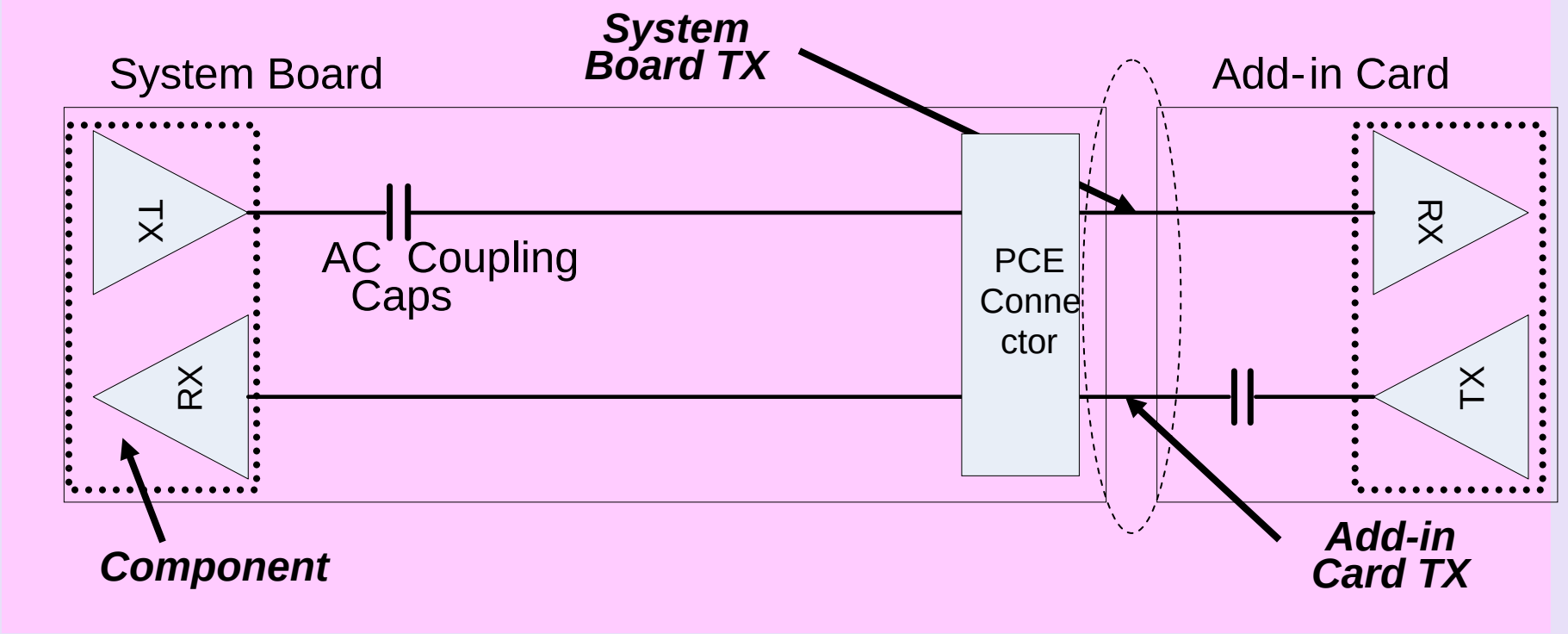


CEM Spec Update

PCI Express 3.0 CEM Goals

- Backwards compatibility
- No required changes to the connectors, card form factors, or material.
- Minimal or no changes to the measurement methodologies from those used in the PCIe* 1.x/2.0 specifications.
  - ✓ Use eye diagrams (jitter/voltage margin requirements). Minimize additional new requirements.

CEM Spec – TX Path



CEM Spec Defines TX Requirements for Chip + Interconnect

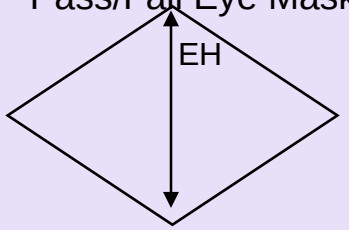
No Separate TX Chip Or Interconnect Only Requirements.

PCIe 3.0 CEM Methodology: End-End Simulation

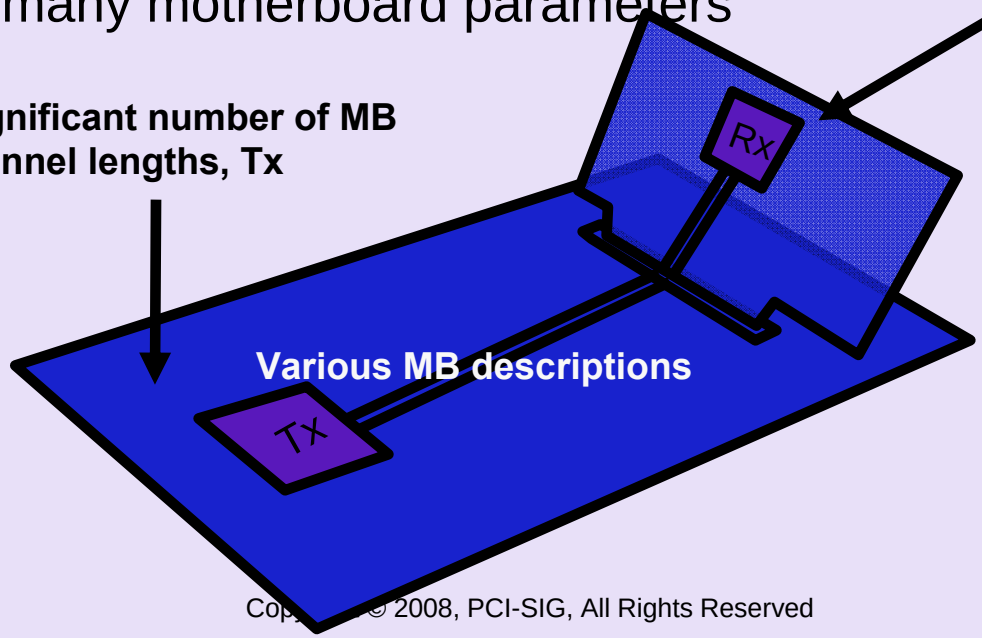
- Perform E2E simulations
  - ✓ Use target 1 connector and 2 connector solutions
  - ✓ Eye height (EH) and eye width (EW) examined after first order CTLE at die pad
  - ✓ Statistical tools used for all simulations
- Fix MB parameters and determine pass/fail conditions across expected add-in card solution space
- Repeat with many motherboard parameters

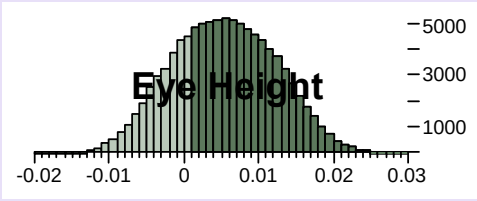
Sweep add-in card parameters over reasonable solution space

Pass/Fail Eye Mask

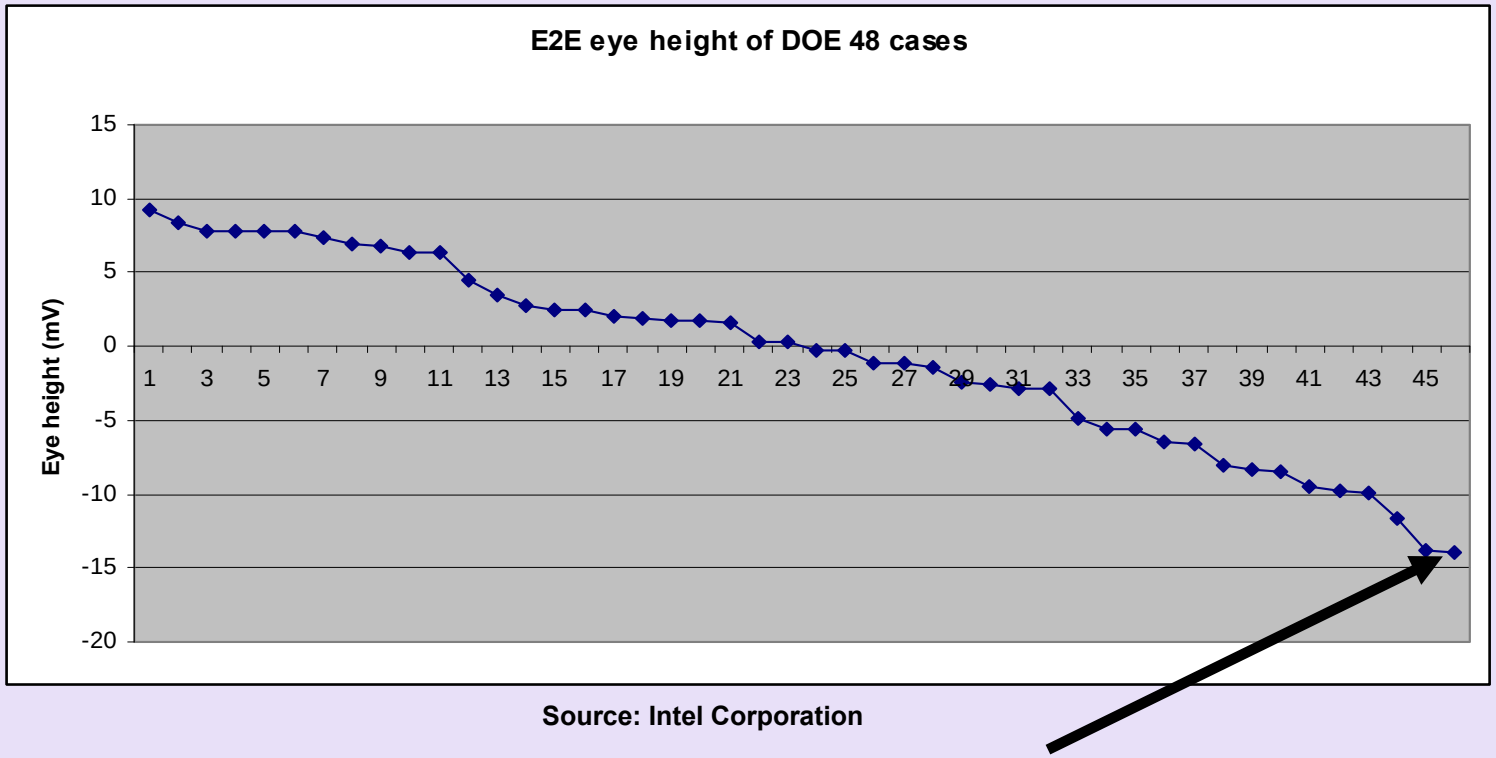


Create a statistically significant number of MB descriptions. (Vary channel lengths, Tx params, etc.)





CEM Simulations - Worst Case Eye Height



Source: Intel Corporation

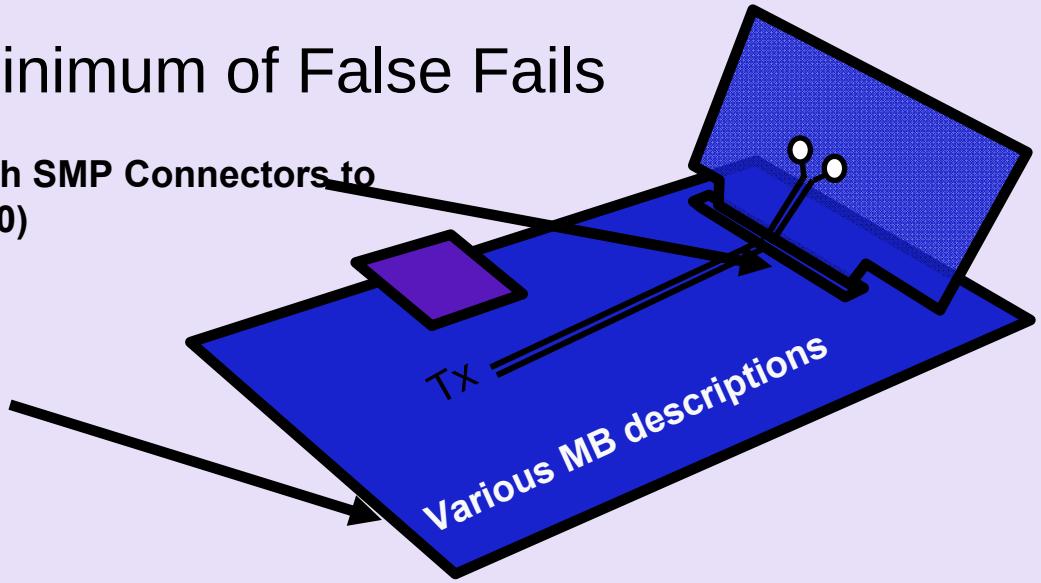
- Worst case Add-in card (AIC) parameters for given MB
- Repeat simulation with different MBs and find worst case for each
- THE ONLY POINT OF INTEREST FOR EACH SET OF MB PARAMETERS IS THE AIC PARAMETERS THAT GIVES WORST CASE

PCIe 3.0 Simulation Methodology Test Fixture Simulations

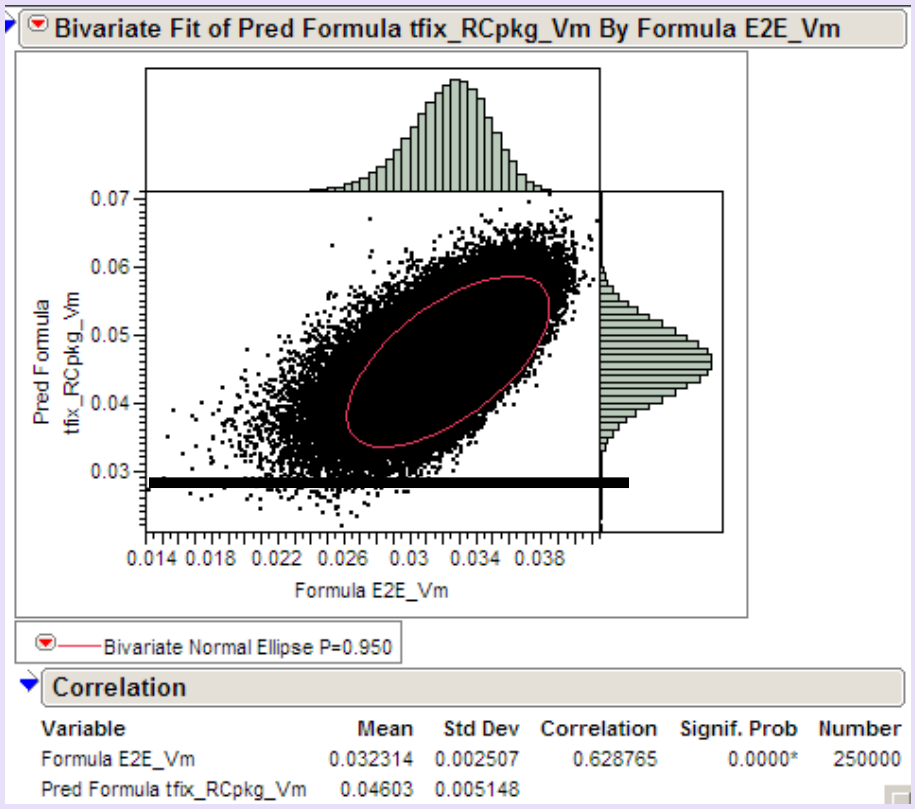
- Choose a test fixture
  - 2.0 CLB Test Fixture Used For Initial Investigation
  - No receiver equalization applied (eye is open)
- Repeat previous MB simulations with test fixture
  - Determine an eye mask at compliance Test Point
  - Find correlation between EH (and EW) at Test Point vs. end to end results
- No False Passes and a minimum of False Fails

Text fixture with SMP Connectors to 'scope (CLB 3.0)

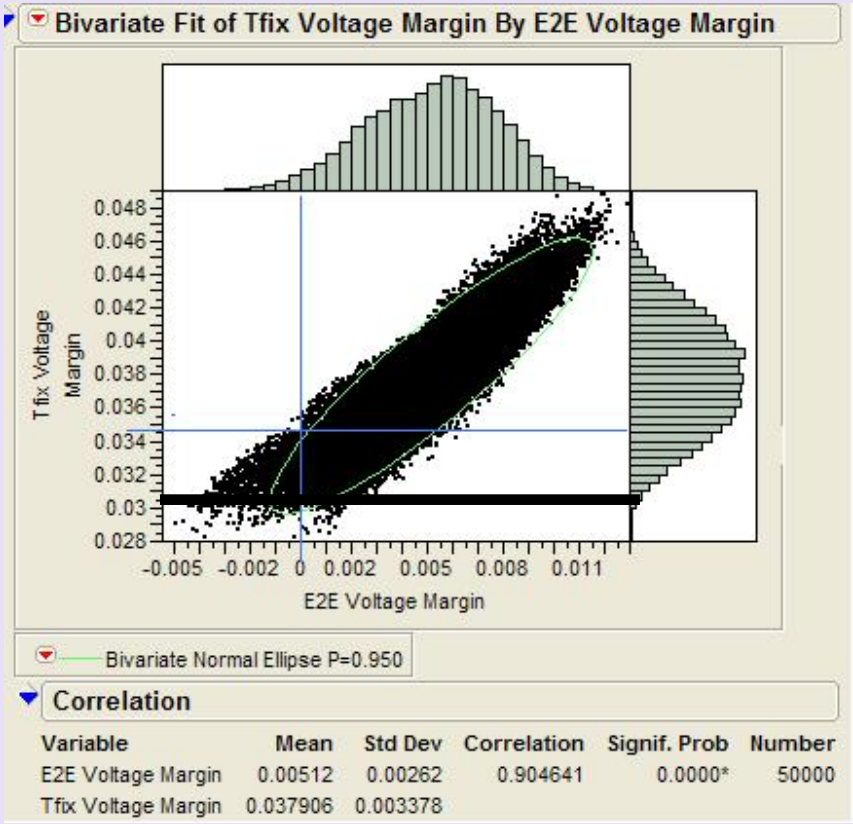
Statistically significant number of MB Descriptions (same as E2E simulations)



Package Model Test Fixture Performance With Product Design Targets



Client MB up to 11”



2 Connector Server up to 16”

Standard test fixture with eye specification can work for PCI Express 3.0 form factors without eliminating target solution space*

Summary/Conclusion

- Key enablers permits 2x PCIe 2.0 throughput with same infrastructure
- Electrical specification methodology and key parameters defined
  - ✓ Measurement at end of breakout channel
  - ✓ Tx, Rx equalization
  - ✓ Replacement for FD return loss
  - ✓ Rx tolerancing
- PCIe 3.0 CEM electrical requirements can be specified as a simple eye diagram measured with a standard test fixture.
- For latest PCIe 3.0 specifications, visit www.pcisig.com
  - ✓ Rev 0.5 PCIe electrical spec approved by EWG and should be ready on PCI-SIG website in Dec'08

Thank you for attending the PCIe Technology Seminar

For more information please go to www.pcisig.com