The Future of PCI Express® Architecture

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What They're Saying…

WIKIPEDIA

Outlook (2005)

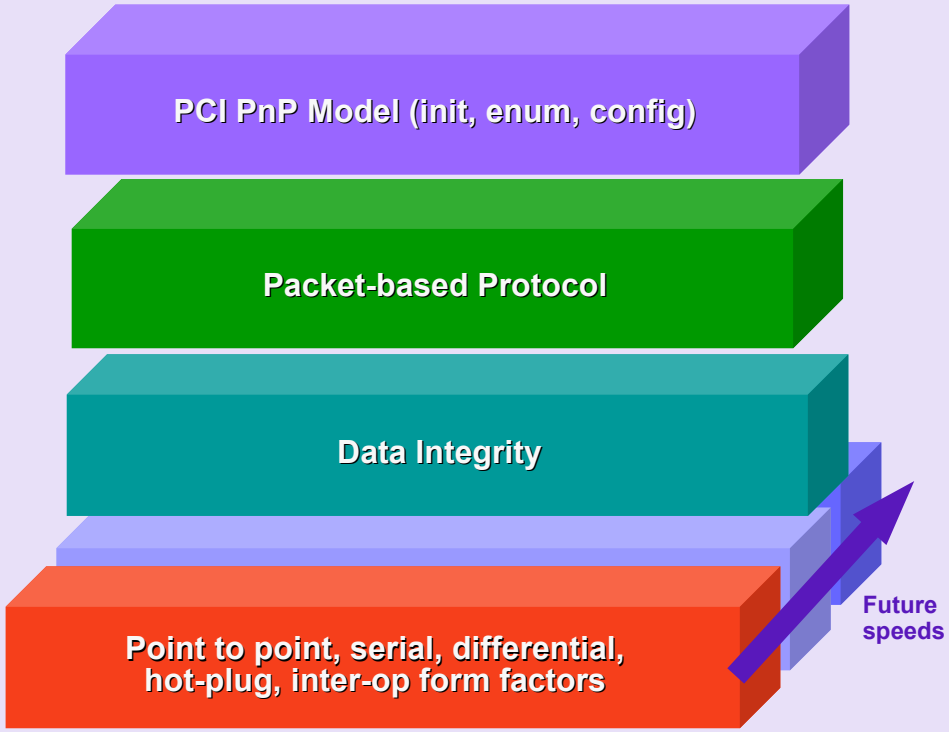
PCI Express appears to be well on its way to becoming the new backplane standard in personal computers … the principal reason is that it was designed to be completely transparent to software developers - an operating system designed for PCI can boot in a PCI Express system without any code modification. Other secondary reasons include its enhanced performance and strong brand recognition.

Most of the new graphics cards use PCI Express … Most new Gigabit Ethernet chips and some 802.11 wireless chips also use PCI Express … Other hardware such as RAID controllers and network cards are also starting to make the switch … hence supplanting the AGP and PCI-X® connectivity … ExpressCard* is just starting to emerge on laptops.

Agenda

- **PCI Express 2.0 Overview**
- The Future of PCI Express Architecture
- Call to Action

PCIe® 2.0 Snapshot



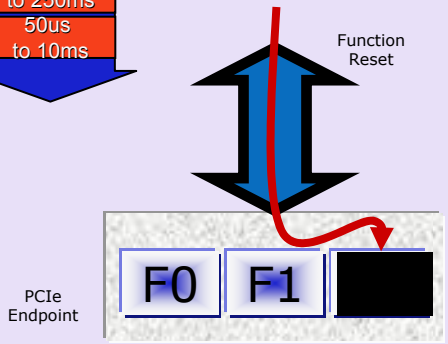
- **Software & Protocols**
  - ✓ Completion timeout
  - ✓ Function-level reset
  - ✓ Access control services
  - ✓ Link bandwidth notification
  - ✓ Link speed controls
- **Physical**
  - ✓ 5GT/s signaling
  - ✓ Speed negotiation
  - ✓ Dynamic link reconfiguration
  - ✓ Margining and compliance

Enhancements to the protocol layer
Significant changes to the PHY layer

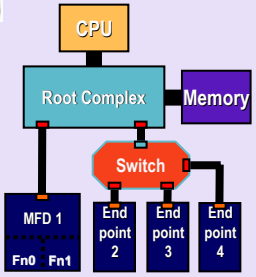
PCIe 2.0 Protocol Updates

- **Completion Timeout**
  - ✓ Required disable mechanism
  - ✓ Optional programmability

- **Function Level Reset (FLR)**
  - ✓ Optional enhanced software reset mechanism
  - ✓ Supports improved robustness, virtualization



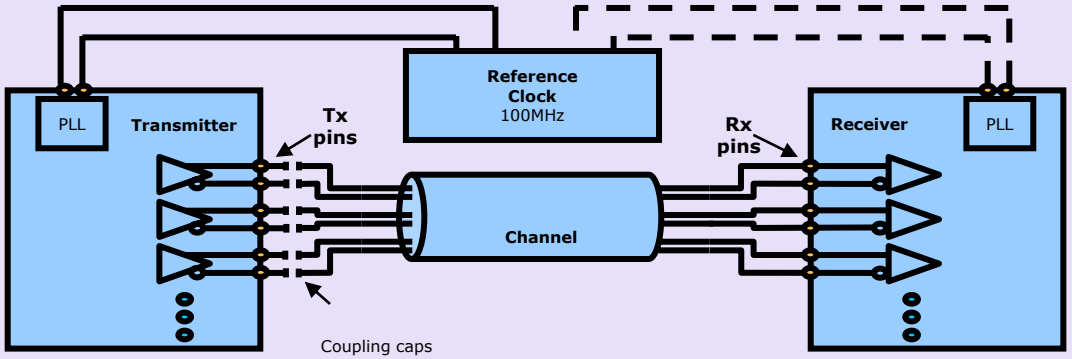
- **Access Control Services (ACS)**
  - ✓ Enhanced control/robustness for peer to peer traffic
  - ✓ Supports virtualization



- **Link Bandwidth Notification Mechanism**
  - ✓ Software notification of link speed/width changes

- **Link Speed Control**
  - ✓ Protocol changes to match the Physical Layer

PCIe 2.0 Electrical Updates



- **All interconnect components specified for interoperability**
  - ✓ PCIe 1.0a: Transmitter
  - ✓ PCIe 1.1: PCIe 1.0a + Reference Clock
  - ✓ PCIe 2.0: PCIe 1.1 + Channel + Receiver

- **Evaluating selectable Tx de-emphasis: -3.5 and -6 dB**
  - ✓ Design flexibility for short (reflective) and long (lossy) channels

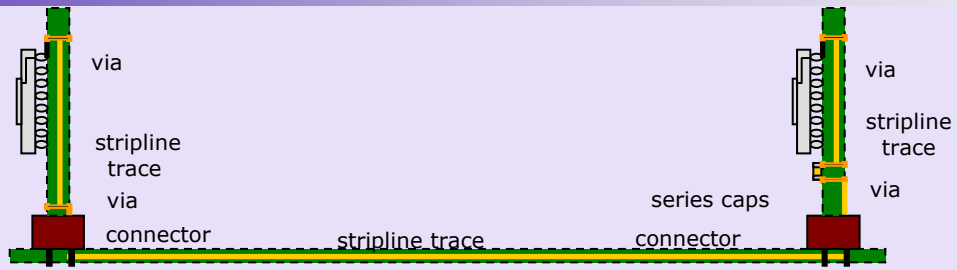
- **Tx margining: for high-speed interconnect reliability**
  - ✓ Supports wide dynamic voltage range (max 1.2V, min 0.8V) to drive system into failure

Design and validate all parameters to the limit of the allowed budgets

PCIe 2.0 LTSSM Updates

- **Speed Negotiation**
  - ✓ Dynamic link speed adjustment
  - ✓ Improves RAS and power savings
- **Compliance Speed**
  - ✓ In-band and programmable compliance pattern speed
  - ✓ Flexibility and reduced cost to implement compliance testing
- **Electrical Idle Entry/Exit**
  - ✓ Protocol enhancements to facilitate circuit design
  - ✓ Improves RAS, yield and ease of design
- **Link Width Reconfiguration**
  - ✓ Increase link width to original trained width
  - ✓ Improves power savings
- **Compliance Entry/Exit**
  - ✓ Device configuration despite failures
  - ✓ Improves RAS

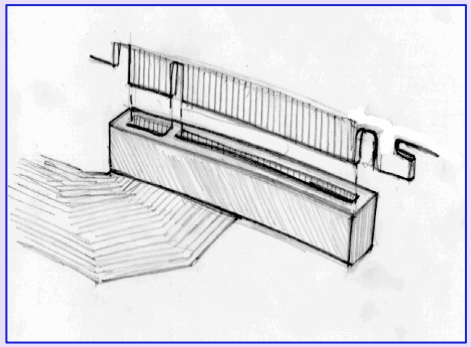
PCIe 2.0 Cards/Slots

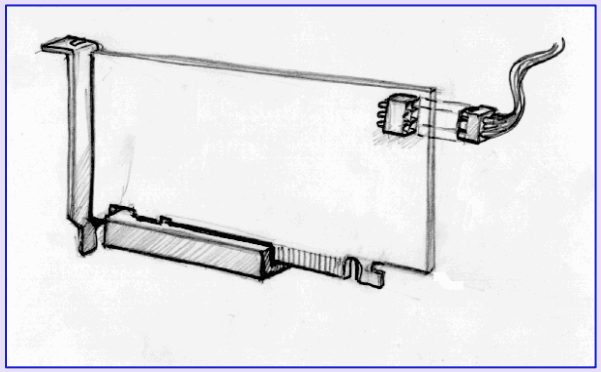


- **High-volume design guidelines and considerations**
- **Simulation modeling in progress for various topologies**
  - ✓ Impedance targets
  - ✓ Trace lengths
  - ✓ Connectors
- **Evaluating behavioral variations for optimum solution space**
  - ✓ Data pattern
  - ✓ De-emphasis settings: -3.5 or -6 dB
  - ✓ 85Ω PCB impedance target
  - ✓ 1pf package model

Focus: Interoperability by construction

Graphics Updates





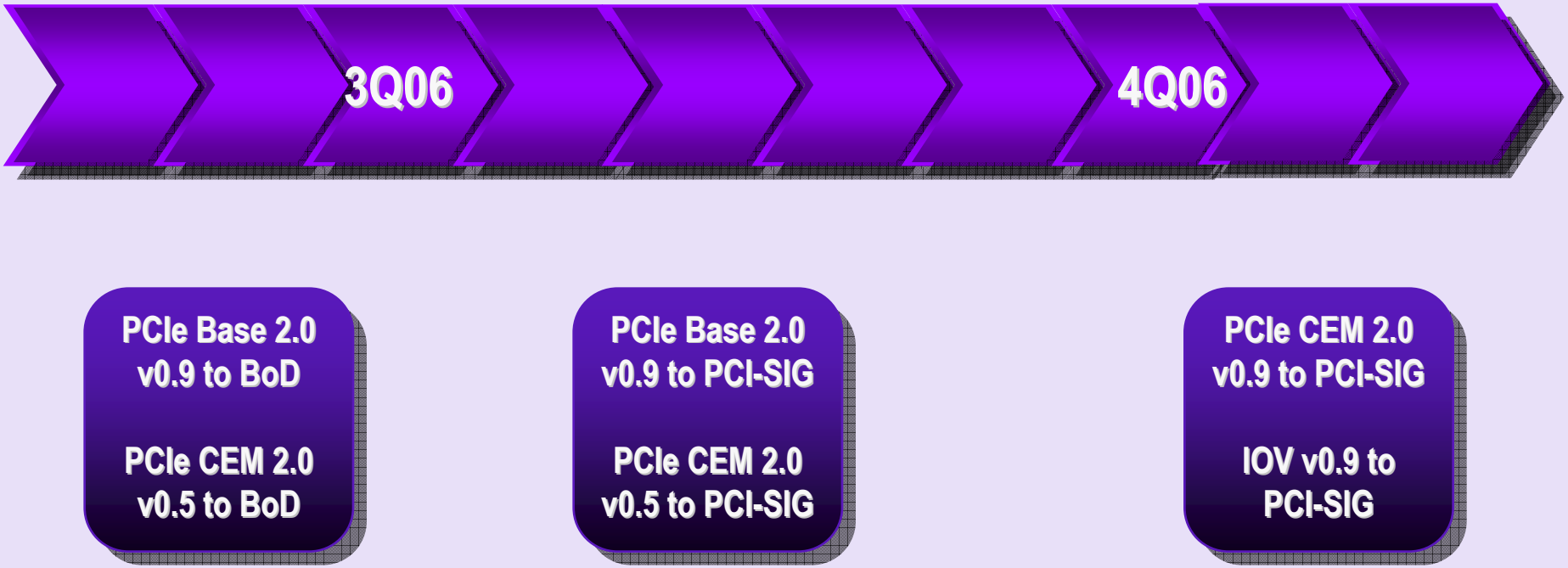
- **Slot short-wiring (a.k.a. downshifting) to enable dual-graphics and other applications**
  - ✓ Interim (CEM 1.1): short-wired slot
  - ✓ Long-term (CEM 2.0): downshifted ports
- **225W/300W specification for high-end discrete graphics (ATX)**
  - ✓ Comprehends thermals/cooling/air flow
  - ✓ Power delivered via new 2x4 connector

Other Form Factors

Picture courtesy of Molex

- Cable specification is at draft 0.7 revision
  - ✓ Decoupled from 5G signaling
  - ✓ Cable assemblies have been measured and validated
  - ✓ x16 Connector pin-out has changed
- Moving to draft 0.9 in 3Q06
  - ✓ Prove worst-case budgets meet PCIe 1.1 signaling requirements

Looking Ahead



PCI-SIG member collaboration needed for 2007-2008 product ramp

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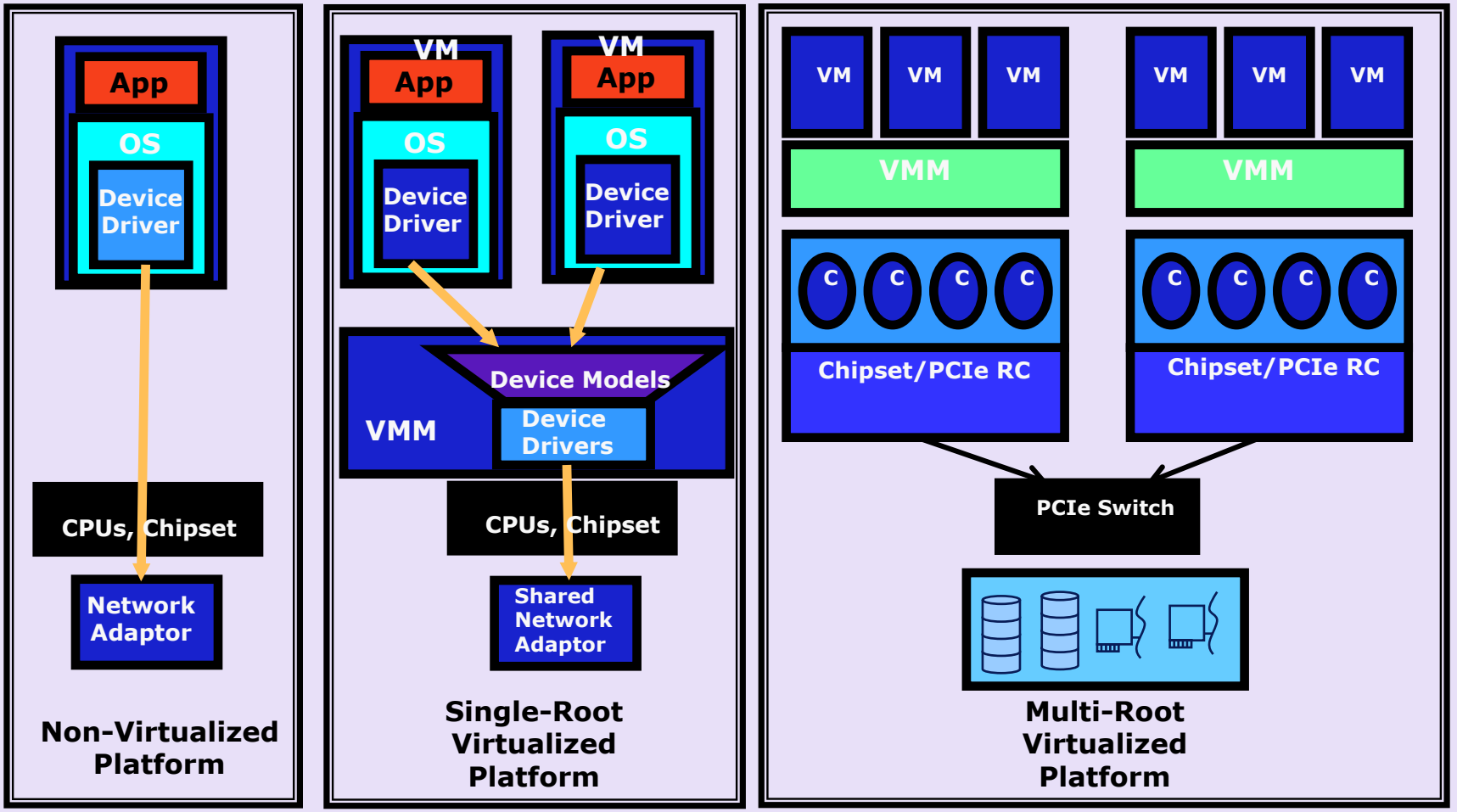
Factors Driving PCIe Futures

- **Multi-Everything!**
  - ✓ CPUs, multi-core, operating systems
  - ✓ Device virtualization and sharing
  - ✓ Multiple graphics cards
- **Higher Performance**
  - ✓ Next generation graphics, storage, networking and fabrics
  - ✓ Need for more connectivity: flexible interconnect width/speed
  - ✓ Lower power
- **Technology advances**
  - ✓ Si process
  - ✓ High volume manufacturing
  - ✓ Materials

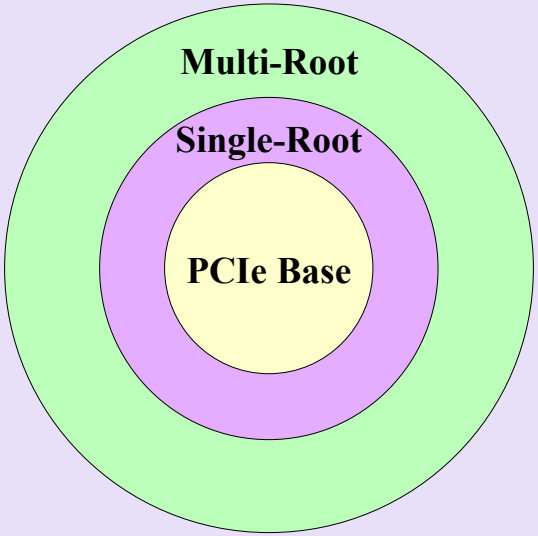
I/O Virtualization Extensions



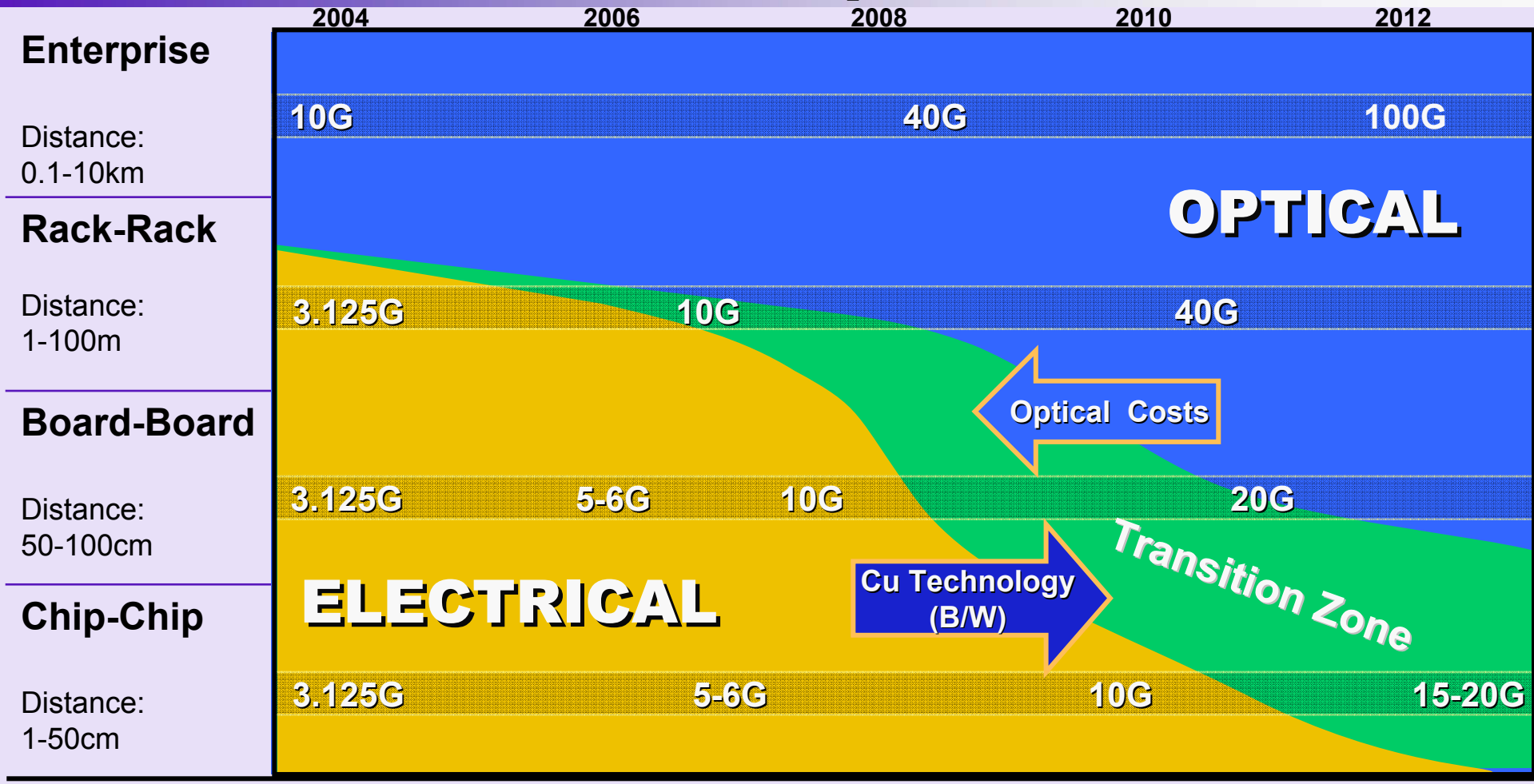
PCIe enables efficient virtualization of I/O devices

IOV Technical Approach

- **Limited to PCIe specification suite**
  - ✓ Base, PCIe Bridge, etc.
- **Enables endpoints to be shared by guest operating systems**
  - ✓ Single- and multi-root scenarios
  - ✓ Create, manage, remove virtual resources
- **Compatibility**
  - ✓ New IOV capabilities defined as supersets of PCIe specifications
  - ✓ Limited functionality with existing software
  - ✓ Software intermediary owns configuration space
- **Control of inter-domain peer-to-peer**
- **Endpoint caching of address translations**



Interconnect Speeds



Cu is the incumbent technology

Future PCIe Specifications

- **Compatibility**
  - ✓ Interoperability with previous generations
- **Performance Target**
  - ✓ ~2x increase over PCIe 2.0 data rate
- **Cost**
  - ✓ High-volume manufacturing considerations
- **Architectural Enhancements**
  - ✓ I/O device virtualization
  - ✓ Form factor innovations
- **Schedule**
  - ✓ Driven by market requirements

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Call to Action

- Immerse yourself in the PCI Express architecture training at this Conference!
- Innovate and differentiate your products with PCI Express 2.0 technology
- Contribute to the evolution of PCI Express architecture
- Visit www.pcisig.com for specification updates

PCIe 2.0 @ DevCon

Day 1		Track 1 - PCI Express
8:30am - 9:00am	Keynote	The Future of PCI Express Architecture *Ajay Bhatt*
9:00am - 10:00am	Session 1	**PCIe 2.0 Phy Architecture** *Debendra Das Sharma*
10:00am - 11:00am	Session 2	**PCIe 2.0 Electricals Tutorial - Part 1** *Jeff Morriss, Gerry Talbot*
11:00am - 12:00pm	Session 3	**PCIe 2.0 Electricals Tutorial - Part 2** *Jeff Morriss, Gerry Talbot*
12:00pm - 1:30pm	Exhibit Area	*Lunch and Exhibit*
1:30pm - 2:30pm	Session 4	**PCIe 2.0 Cards/Slots** *Dan Froelich*
2:30pm - 3:30pm	Session 5	**PCIe 2.0 Protocol Updates** *Joe Cowan*
3:30pm - 4:00pm	Exhibit Area	
4:00pm - 5:00pm	Session 6	Mobile Form Factor Updates *Ron Shaw*

For other tracks and sessions, refer to the full conference schedule

Thank you for attending the PCI-SIG Developers Conference 2006.

For more information please go to www.pcisig.com