

The cover features a vertical split. The left side shows a blue-tinted, high-angle view of a server room with rows of racks and cables. The right side is a dark background with several overlapping, semi-transparent grey geometric shapes, including triangles and lines, creating a dynamic, abstract design.

PCI-SIG Developers Conference 2006

June 8 - 9, 2006

San Jose McEnery Convention Center

San Jose, California



Come Celebrate PCI-SIG Technology!

You're invited!

PCI-SIG DevCon Evening Mixer

Thursday • June 8 • 6:00 pm

Join us Thursday in the Exhibit Area at 6:00 pm for the Annual Meeting of the Members, with PCI-SIG Chairman Tony Pierce's "State of the SIG" presentation.

Immediately following will be the Evening Mixer, with food, refreshments and a great opportunity for some informal Q&A, networking and time to chat with the speakers, sponsors and other attendees.

This year NVIDIA is sponsoring a hosted beer bar.



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The Sponsor Exhibit Area showcases industry-leading member companies and their most recent product developments and designs based on PCI architectures and tools.

PCI-SIG Developers Conference 2006: Floor Plan



PCI-SIG Developers Conference 2006: Agenda

Day 1		Track 1 - PCI Express	Track 2 - I/O Virtualization
8:30 - 9:00	Keynote	The Future of PCI Express Architecture	
9:00 - 10:00	Session 1	PCIe 2.0 Phy Architecture	IOV Architectural Overview
10:00 - 11:00	Session 2	PCIe 2.0 Electricals Tutorial – Part 1	Address Translation Services
11:00 - 12:00	Session 3	PCIe 2.0 Electricals Tutorial – Part 2	Single Root IOV
12:00 - 1:30	Exhibit Area	Lunch & Exhibit	
1:30 - 2:30	Session 4	PCIe 2.0 Cards/Slots	Multi-Root Resource Allocation
2:30 - 3:30	Session 5	PCIe 2.0 Protocol Updates	Multi-Root IOV
3:30 - 4:00	Exhibit Area	Break & Exhibit	
4:00 - 5:00	Session 6	Mobile Form Factor Updates	Error, Interrupt & Event Handling
5:00 - 6:00	Session 7	PCIe Ask the Experts	IOV Q&A Session
6:00 - 8:00	Exhibit Area	Annual Meeting & Evening Mixer	

Day 2		Track 1 - PCI Express	Track 2 - I/O Virtualization
9:00 - 10:00	Session 8	PCIe 2.0 Phy Architecture	IOV Architectural Overview
10:00 - 10:30	Exhibit Area	Break & Exhibit	
10:30 - 11:30	Session 9	PCIe 2.0 Electricals Tutorial – Part 1	Address Translation Services
11:30 - 12:30	Session 10	PCIe 2.0 Electricals Tutorial – Part 2	Single Root IOV
12:30 - 1:30	Exhibit Area	Lunch & Exhibit	
1:30 - 2:30	Session 11	PCIe 2.0 Cards/Slots	Multi-Root Resource Allocation
2:30 - 3:30	Session 12	PCIe 2.0 Protocol Updates	Multi-Root IOV
3:30 - 4:00	Foyer	Break in Foyer	
4:00 - 5:00	Session 13	Mobile Form Factor Updates	Error, Interrupt & Event Handling
5:00 - 6:00	Session 14		



Track 3 - Introductory PCI Technology		Track 4 - Members Implementation	
	PCI-SIG Architecture Overview		Formal Verification for PCIe 1.1 and 2.0 RTL Designs
	PCI-SIG Compliance & Interoperability		Modeling Techniques for Efficient Verification of PCIe Switch
	PCI Express Integrity		Looking Beyond the Compliance Checklist
Lunch & Exhibit			
	Conventional PCI		Optimizing PCIe Port Performance
	PCI Express Basics		Implementing MSI and MSI-X in a Root Complex
Break & Exhibit			
	Electrical Modeling Alternatives and Languages <i>(Bonus Track 4 Session)</i>		Implementing PCIe Advanced Error Reporting
	Techniques for Efficient Verification of PCIe to PCI Bridge <i>(Bonus Track 4 Session)</i>		A Successful Approach to PCI Express System Debug
Annual Meeting & Evening Mixer			

Track 3 - Introductory PCI Technology		Track 4 - Members Implementation	
	PCI-SIG Architecture Overview		PCIe Board Routing – To Interleave or Not?
Break & Exhibit			
	PCI-SIG Compliance & Interoperability		Holistic PCIe Phy Integration
	PCI Express Integrity		PCIe Phy Design Case Study
Lunch & Exhibit			
	Conventional PCI		Signal Integrity and Jitter Testing Challenges at 5GHz
	PCI Express Basics		Case Study of PCIe as an On-board System Bus
Break in Foyer			
	PCIe Server Validation <i>(Bonus Track 4 Session)</i>		PCI Express – A Forward Looking Protocol
			The Nuts and Bolts of Integrating PCIe into Your Design

PCI-SIG Developers Conference 2006: Presentation Abstracts

Keynote

The Future of PCI Express Architecture

Track 1: Keynote

Presenter: Ajay Bhatt

PCI Express® architecture is the ubiquitous, general-purpose I/O technology found in PCs, laptops, workstations and server systems. It is implemented in graphics, networking, storage and many other high-speed, low-cost applications. Ajay Bhatt, Intel Fellow and a lead architect for PCI Express, will talk about the current state and the future direction of this important I/O technology as it continues to meet and exceed the varying requirements of Enterprise, Consumer and Communications platforms.

PCI Express

PCIe 2.0 Phy Architecture

Track 1: Session 1, Session 8

Presenter: Debendra Das Sharma



This session will cover the architectural extensions provided in the latest updates of the PCIe® 2.0 draft specification. These include dynamic speed negotiation protocol, mechanisms to control speed during transmitter compliance testing, protocol change to enable a link to operate in a degraded mode in the presence of one or more wire failures, and novel mechanisms to determine electrical idle for enhanced robustness. The session will also cover a new capability introduced in the PCIe 2.0 specification that allows a link to change its width dynamically, enabling devices to save power when bandwidth requirements are low. It will illustrate how these architectural extensions offer power savings, high reliability, improved yield, enhanced robustness, time to market advantages and better performance due to the 5GT/sec data rate. Those who are designing, validating or specifying the latest generation of PCIe components are the target audience for this session.

PCIe 2.0 Electrical Parameters Tutorial – Part 1 & 2

Track 1: Sessions 2-3, Session 9-10

Presenters: Jeff Morriss and Gerry Talbot

The transition from PCIe 1.0 to PCIe 2.0 is intended to minimize system design changes and achieve increased performance through scaling of the data rate of the end points. However, the tightened margins required for operation at 5.0GT/s require that some of the AC parameters and the way they are measured be redefined. The PCIe 2.0 base specification divides up the electrical layer into four components: Transmitter, Channel, Receiver and Reference clock. This tutorial is split into two parts, with Jeff covering the Transmitter and Channel, and Gerry the Receiver and Reference clock. The latest consensus from the Electrical Workgroup for this specification will be discussed, anticipating the 0.9 draft that is planned to be released for member review later this year. This session is geared toward experienced PCI Express Phy designers and validation engineers.



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PCIe 2.0 Cards/Slots

Track 1: Session 4, Session 11

Presenter: Dan Froelich

This course will focus on electrical updates needed to support 5.0 GT/s signaling, but will also provide status on other areas being updated in the CEM specification. You will learn how a form factor specification is derived from the PCI Express 2.0 base specification and the specific process used to derive eye diagram requirements at a form factor interface. You will also learn about testing issues involving real system clocks that require different methodologies from those defined in the PCI Express 2.0 base specification.

PCIe 2.0 Protocol Updates

Track 1: Session 5, Session 12

Presenter: Joe Cowan

The PCIe 2.0 base specification is a significant evolutionary and compatible update to the existing 1.0a and 1.1 Base specs. The 2.0 base spec adds support for higher speed (5GT/sec) signaling, incorporates several major ECNs, and includes the latest errata. This presentation gives a Protocol and Software overview of the updates in the 2.0 base spec. The course will focus on the negotiation and control mechanisms for 5GT/sec signaling, new ECNs and selected errata. The covered ECNs include Bandwidth Change Notification, Completion Timeout, Function-Level Reset and Access Control Services.

Mobile Form Factor Updates

Track 1: Session 6, Session 13

Presenter: Ron Shaw

This presentation provides a status update and changes on mobile form factors: the mini-Card, new half-mini-Card, ExpressCard and the suspension of work on the Wireless Form Factor (WFF). Emphasis will be on changes since the PCI-SIG Developers Conference 2005, and ECRs which have passed or in process at the mini-Card Workgroup and at the PCMCIA technical committee.

PCIe Ask the Experts

Track 1: Session 7

Presenters: PCIe Presenters

An excellent opportunity to query the PCI-SIG experts on the details of the PCIe 2.0 (5GT/s) specifications. Plan to attend if you have questions about the PCIe interconnect architecture or have interesting learnings you want to share with other members.



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I/O Virtualization

IOV Architectural Overview

Track 2: Session 1, Session 8

Presenter: Michael Krause

System virtualization technologies allow multiple operating systems running simultaneously within a single server or even a client computer. As a result, it becomes desirable to share PCI Technology I/O adapters. PCI-SIG® has formed the I/O Virtualization (IOV) Workgroup to develop specifications to enable this sharing. This presentation will give a general introduction to I/O Virtualization, an overview of the areas being addressed by the Workgroup, and updates on the status of the various specifications in progress.

Address Translation Services

Track 2: Session 2, Session 9

Presenter: Michael Krause

The Address Translation Services (ATS) specification provides a set of transactions for PCI Express com-

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ponents to exchange and use translated addressing. This presentation will give an overview of those mechanisms, the ATS transactions themselves and the status of this PCI-SIG Draft Specification.

Single Root IOV

Track 2: Session 3, Session 10

Presenter: David Kahn

This topic will describe the work being done by the PCI-SIG I/O Virtualization Workgroup. Specifically, we will describe the current work being done to support I/O device virtualization (multiple, virtual views of the same function) using the PCI Express base protocol. Single Root refers to the current PCIe base topology in which each hierarchy has a single root complex.

Multi-Root Resource Allocation

Track 2: Session 4, Session 11

Presenter: Michael Krause

This presentation will discuss the processes by which a PCI Multi-Root I/O Virtualization system enumerates the multiple Virtual Hierarchies within the physical hierarchy. The interaction between Multi-Root and Single Root IOV components will be explained, showing the means by which the two techniques complement and overlap to divide up virtualized resources within an endpoint. Special considerations for various types of multi-function IOV endpoints will be covered as well. This session will be of interest to those interested in Multi-Root IOV technologies.

Multi-Root IOV

Track 2: Session 5, Session 12

Presenter: Chris Pettey

The Multi-Root IOV presentation discusses the technical details related to current progress within the PCI-SIG IOV Workgroup as related to Multi-Root specifications. Topics include the overall architecture for Multi-Root PCIe IOV, extensions to the PCIe protocol for Multi-Root, component impact and new software requirements. The session includes both technical requirements and usage models.

Error, Interrupt & Event Handling

Track 2: Session 6, Session 13

Presenter: Mahesh Wagh

This topic will describe the work being done by the PCI-SIG I/O Virtualization workgroup on Error Reporting and Event and Interrupt handling for Single Root and Multi-Root environments.

IOV Q&A Session

Track 2: Session 7

Presenters: All IOV Presenters

Question and Answer session with members of the I/O Virtualization Workgroup.

Introductory PCI Technology

PCI-SIG Architecture Overview

Track 3: Session 1, Session 8

Presenter: Richard Solomon

This presentation will provide an overview of PCI and PCI-X®, including architectural features which form the foundation for PCI Express. Key concepts such as MSI, MSI-X, Transaction Attributes and Split Transactions which span the spectrum from Conventional PCI through PCI-X to PCI Express are explained. This presentation should be a particularly useful starting point for attendees new to PCI-SIG technologies. Information on the specification revisions requiring these features should be of interest even to more experienced members.

PCI-SIG Compliance & Interoperability

Track 3: Session 2, Session 9

Presenter: Dan Froelich

In this course, PCI-SIG will outline the requirements for PCI Express compliance and interoperability. You will learn about the tests and tools provided by PCI-SIG as well as a timeline for upcoming Compliance Workshop events worldwide, where you can validate your parts for compliance to the PCI-SIG “Gold” suite of tests. The course will emphasize the updates to electrical test tools for the 1.1 revisions of the PCI Express base and CEM specifications.

PCI Express Integrity

Track 3: Session 3, Session 10

Presenter: Gord Caruk

The integrity of communications is a key issue facing the computing industry. This session will discuss the features of PCI Express that make it difficult to eavesdrop transactions. Two mechanisms that might be used in an attempt to subvert the integrity of the PCI Express interconnect will serve to highlight these features.

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Members Implementation

Formal Verification for PCIe 1.1 and 2.0 RTL Designs

Track 4: Session 1

Presenter: Vigyan Singh

Assertion-based formal verification can guarantee behavior of critical functionality in RTL designs when simulation may miss corner-case bugs. This is especially important for PCIe compliance. However, a successful application requires judiciously selecting the right design- and specification-specific techniques for decomposing formal proofs. For maximum coverage, it is important to complement formal with coverage- and constraint-driven simulation as well as semi-formal techniques. We describe how these techniques can be used to functionally verify PCIe RTL designs, whether internally developed or bought as third-party IP.

Modeling Techniques for Efficient Verification of PCIe Switch

Track 4: Session 2

Presenter: Asad Khan

With growing complexity of new PCI Express designs where opportunity for IP-reuse may be limited or none, achieving high-quality first silicon demands deployment of novel verification techniques. PCI Express switches incorporate complexities of packet switching with challenges of current and legacy specifications. One strategy in achieving high-quality PCI Express switch silicon is creating reference models or predictors that work in cycle accurate, packet accurate or hybrid fashion to verify the design. This presentation discusses verification techniques to create reference models for block-level testing in such a way that these models seamlessly integrate at the chip-level without additional effort.

Looking Beyond the Compliance Checklist

Track 4: Session 3

Presenter: Erez Kovshi

While the PCI Express Compliance checklist is important, checking all the boxes does not ensure that verification is complete. Worse yet, it does not even ensure that the design is truly PCI Express compliant. If the checklist is viewed as a verification plan, it's easy to be deluded that checking it off means verification is complete. In fact, a verification methodology must be integral to the verification IP. This is needed to answer compliance questions such as: have all scenarios described by an item been covered? This session

Conventional PCI

Track 3: Session 4, Session 11

Presenter: Don Anderson

This course describes the architecture of a PCI based computer system. PCI bus architecture features are described, and the mechanism to complete read/write data transfers is described. This session also covers an overview of the bus arbitration, interrupt and error handling process. The PCI device configuration process will also be explained.

PCI Express Basics

Track 3: Session 5, Session 12

Presenter: Joe Winkles

This session provides an overview of the PCI Express technology. This will cover the basics of such topics as system topologies, device layers, packet types, routing mechanisms, ACK/NAK protocol, flow control, virtual channels, and more.

addresses resolving common checklist pitfalls based on a proven verification methodology.

Optimizing PCIe Port Performance

Track 4: Session 4

Presenter: Ilya Granovsky

This presentation describes various considerations involved in PCI Express logic design for systems with high performance requirements. The impact of different PCI Express parameters on applications performance is analyzed and illustrated by performance simulation results. The presentation elaborates on architecture and design techniques used for improving effective data bandwidth and reducing latency. It is based on experience with various PCI Express applications and relies on practical data gathered during architecture, design, pre-silicon and post silicon verification stages of these projects.

Implementing MSI and MSI-X in a Root Complex

Track 4: Session 5

Presenter: Govinda Tatti

The first portion of this presentation will focus on implementation of PCI Express root complex hardware and software to support MSI and MSI-X interrupts. The second portion will focus on the changes required to the software programming model for Solaris device drivers to use new interrupt Device Driver Interfaces (DDI) defined for MSI and MSI-X interrupts.

Electrical Modeling Alternatives and Languages

Track 3: Session 6

Presenter: Gary Pratt

Choosing a Signal Integrity verification technique can be confusing with all the simulation and modeling choices available today. This presentation will go through the most common choices available and describe the primary strengths and weaknesses of each. The presentation will detail the features of the new IBIS 4.1 AMS SI modeling standard, and demonstrate how it can be used in simulations that are as accurate as transistor-level SPICE but hundreds of times faster. The presentation will show a case study of modeling a PCI Express driver in AMS and will conclude with examples of other novel applications of IBIS 4.1 and AMS (such as automated measurements, CDR and DFE).

Implementing PCIe Advanced Error Reporting

Track 4: Session 6

Presenter: Dr. Gene Saghi

The perils and pitfalls of implementing PCIe Advanced Error Reporting (AER) in an endpoint device will be presented. Main areas of coverage will include error detection, error messages, error pollution, error logging and advisory non-fatal errors. For each of these areas the requirements set out in the PCIe 1.1 specification will be discussed as well as suggestions and issues to be considered. These are derived from the presenter's experience as a designer on two different PCIe cores that have seen silicon and a third core that is currently being developed – all implementing AER.

Techniques for Efficient Verification of PCIe to PCI Bridge

Track 3: Session 7

Presenter: Nitin Gupta

Even without considering the design difficulty, verifying a PCIe to PCI bridge design is a very big challenge today. With different configurations to support PCIe x1-xN, PCI 33/66 MHz and PCI-X 66/100/133 MHz, the environment becomes too complex to handle manually. An ideal verification environment would have an end to end checker as a key component,

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along with protocol checkers to intelligently track and analyze all the traffic on the different bus interfaces. This presentation, written on the basis of the authors' experience and understanding of verifying a PCIe to PCI bridge, discusses a conceptual framework used to build a complete, robust and efficient verification environment.

A Successful Approach to PCI Express System Debug

Track 4: Session 7

Presenter: Betty Luk

The PCI Express interface is often a starting point for the debug process when a system failure is encountered. An important step in the diagnosis of a problem is to distinguish between electrical and logical issues. This can be done using a systematic debug flow to break down the failure into common categories. This presentation discusses an approach to PCI Express debug, with specific examples, to show PCI Express features that can be used for debug, the tools required, and other tips for efficient debugging and timely problem resolution.

PCIe Board Routing - To Interleave or Not?

Track 4: Session 8

Presenter: Patrick Carrier

In writing design implementation guidelines for PCI Express, many chip vendors will make board routing suggestions falling into two distinct camps: 1) to specifically interleave TX and RX differential pairs for crosstalk control or 2) to specifically NOT interleave those signals. This has become an increasingly important topic, with differing opinions being traced back to the very nature of forward and reverse crosstalk, and how they are affected by buffer impedance, trace configuration and trace length. This presentation examines those factors through simulation to determine the correct approach for a given design.

Holistic PCIe Phy Integration

Track 4: Session 9

Presenter: Jeffrey Reynolds

Integrating PCI Express represents the latest system integration challenge faced by many companies today. While traditional engineering techniques focus on improving package design, board design, and cleaner power supplies, these techniques increase costs and reduce flexibility. This paper describes a new holistic approach to PCI Express integration, focusing on the complete physical layer solution of

Phy, package, board and power supply. Increased margins in the physical layer can yield dramatically relaxed margins in package and board designs. A side-by-side comparison leads attendees to the conclusion that PCI Express is actually no more difficult to implement than a standard PCI bus.

PCIe Phy Design Case Study

Track 4: Session 10

Presenter: Kannan Krishna

The ability to effectively test and characterize a PCIe Phy is a crucial element in its commercial success. Although many mature and standardized approaches to testing digital circuits exist, the Phy contains many analog and mixed-signal circuits for which no standardized techniques exist. A design methodology is presented that allows the PCIe Phy to be easily characterized and tested in production. The overhead for this built-in test capability is very low in terms of both area and power. Actual results from 90nm and 130nm CMOS test chips are provided.

Signal Integrity and Jitter Testing Challenges at 5GHz

Track 4: Session 11

Presenter: Dr. Mike Li

The data rate increase for PCI Express from Version 1.x (2.5 GT/s) to Version 2.0 (offering 5.0 GT/s) imposes new challenges and requirements, ranging from device circuit design to verification and testing. This presentation focuses on device circuit verification and testing in the important area of signal integrity and jitter for 5GT/sec devices. Some specific challenges and implementations covered in this presentation are: 1) De-emphasize bit equalization for the transmitter jitter testing; 2) Deterministic jitter (DJ) measurement based on dual-Dirac definition; 3) Jitter increase for transmitter and receiver PLLs in the presence of a noisy reference clock; 4) Receiver tolerance test under varying amount of different jitter types, as well as various stressed eye conditions.

Case Study of PCIe as an On-board System Bus

Track 4: Session 12

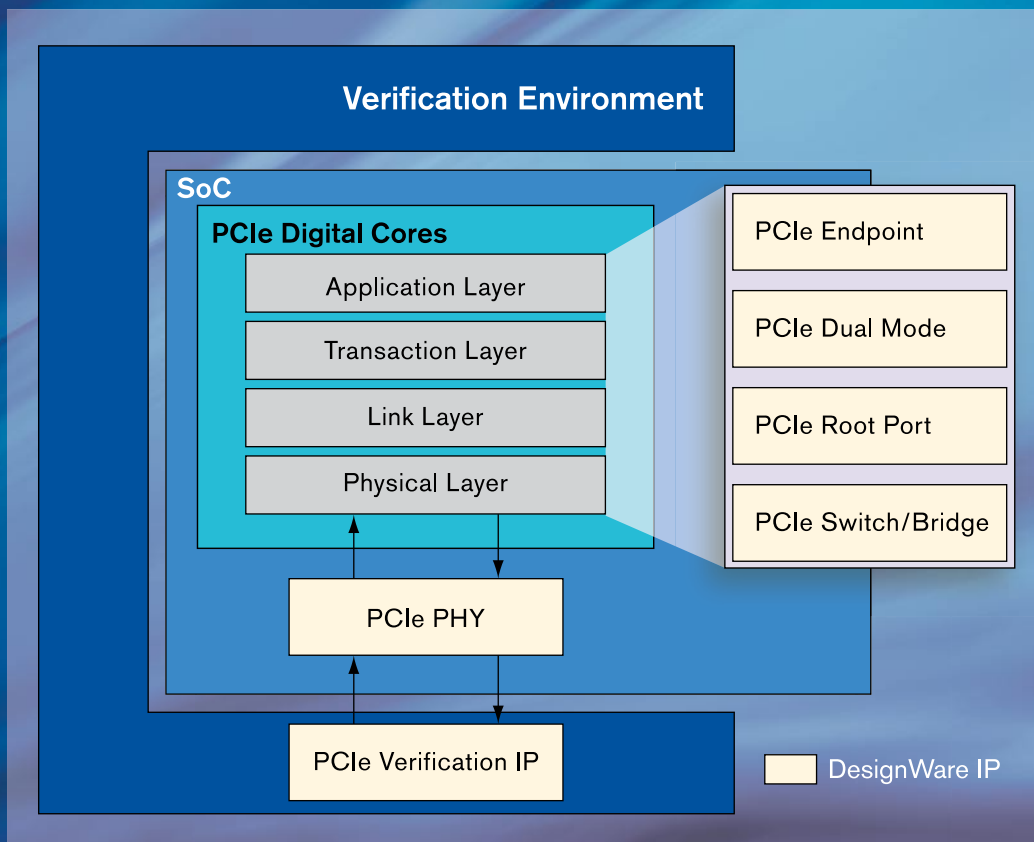
Presenter: Eric Esteve

More than just a high-speed data link, the PCI Express protocol defines sub functions (end point, root port, switch, bridges) that can be used to build a dedicated networking system on a board and solve application-specific architecture challenges. The presentation illustrates such a system with a case study of a real application.

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PCIe Server Validation

Track 3: Session 13

Presenter: Will Atherton

Validating PCI Express can be very challenging in a Server environment. New validation methods must be investigated and tested when new PCI Express features must co-exist in a PCI/PCI X system. New issues also arise as advanced features are enabled in the mass variety of add in cards. Some of the enhanced areas of system testing include: new transactions, co-existence, fault validation, recovery, thresholds and error/information reporting.

PCI Express – A Forward Looking Protocol

Track 4: Session 13

Presenter: Purna Mohanty

This presentation will discuss the critical differences between PCI/PCI-X and PCIe technologies for those using a PCI or PCI-X device for their ASIC/FPGA today and needing to transition to PCIe in the future. This presentation will enable implementers to evaluate the PCIe Technology based on their product requirements. The presentation will also highlight the importance of the PCI-SIG Compliance Program in determining the success of PCIe products. The presenter will share experience from past PCI Express Compliance Workshops.

The Nuts and Bolts of Integrating PCIe into Your Design

Track 4: Session 14

Presenter: Wayne Locke

Developing a PCI Express product and going from prototype to volume production presents a variety of challenges and potential pitfalls. This presentation offers managers and engineers an overview of the challenges involved in selecting and integrating various IP components, the lab equipment and setup required to test the PCI Express subsystem, and key parameters to measure. The presenter describes the preparation required for interoperability and compliance testing, and gives an idea of how much time it may take to successfully complete the integration and test. Methods to limit risk and make the conversion from FPGA to ASIC easier are also presented.

PCI-SIG Developers Conference 2006: Speakers

Don Anderson

Don Anderson has 29 years combined development experience in analog and digital electronics and the computer industry, working for companies such as Hewlett Packard, Schlumberger and Compaq. Since joining MindShare in 1991, he has authored and co-authored 12 books on PC Architecture and has taught over 500 courses.



Will Atherton

Will Atherton works at IBM in the xSeries Servers series on developing new testing methodologies and is the Tools Development lead. He has his BS degrees in Electrical Engineering, and Electrical and Electronic Technology from McNeese State University. He has a MS in Computer Network Engineering from North Carolina State University.



Ajay Bhatt

Ajay Bhatt Chairs the PCI Express Steering Committee for the PCI-SIG. He is a Fellow at Intel Corporation where he has lead development of USB, AGP4X and PCI Express technologies.



Patrick Carrier

Patrick Carrier is a Technical Marketing Engineer at Mentor Graphics for high-speed design tools, including HyperLynx and ICX Pro Explorer. Prior to joining Mentor Graphics, Patrick was a signal integrity engineer at Dell, Inc. in the server division. Patrick has a B.S.E.E. from the Georgia Institute of Technology.



Gord Caruk

Gord Caruk is a hardware architect at ATI Technologies who has successfully implemented support for all major industry bus transitions. Since joining ATI in 1991, Gord has worked closely with the PCI-SIG, is an active contributor in the PCIe Electrical and Protocol Workgroups and is on the PCI-SIG Board of Directors.



Joe Cowan

Joe Cowan is a computer systems architect in HP's Business Critical Servers organization, and represents HP in multiple PCIe Workgroups, where he's authored numerous ECNs/errata. During his 27-year career with HP, Joe has focused on a wide range of technologies, including InfiniBand® Architecture, PCI-X, clustered systems and computer security.



Debendra Das Sharma

Debendra Das Sharma is a Principal Engineer in the Digital Enterprise Group responsible for developing server chipsets. He has been a leading contributor to the PCI Express 2.0 specification in the PCI-SIG. Debendra joined Intel in 2001 and led the development of the Twincastle multiprocessor northbridge chipset and is currently leading the development of several server chipsets. Prior to joining Intel, he was with Hewlett-Packard for seven years where he worked on the development of several server chipsets, including Superdome.



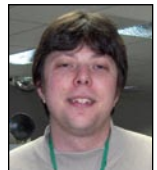
Eric Esteve

Eric Esteve is the Marketing Manager for PLDApplications since 2005. Eric got his PhD from University Paris VII in 1987. ASIC designer and consultant for several years, he joined Texas Instruments in 1992 and has occupied various positions in sales and marketing for Application Specific Products before joining Atmel in 1999 as an ASIC Marketing manager in charge of the North America business.



Dan Froelich

Dan Froelich is a staff engineer/architect at Intel Corporation. He received a B.S. in Physics from Harvey Mudd College in 1996. He played key roles in the technical planning and compliance method and tool development for the USB 2.0 and PCIe compliance programs. He is currently working on the Wireless USB specification and Wireless USB compliance program.



Ilya Granovsky

Ilya Granovsky is a hardware engineer at IBM Engineering and Technology Services division leading PCIe IP cores development team in IBM Haifa Design Lab. He received his B.Sc. in Electrical Engineering from Technion - Israel Institute of Technology.



Nitin Gupta

Nitin Gupta has been with nSys as Project Lead since 2002. He has been instrumental in the development of nSys' portfolio of VIPs including PCI, PCI Express, PCI-X, AXI, etc. He has also been involved in the verification of multiple complex SoCs. Nitin Gupta holds an engineering degree in Electronics and has over 7 years of experience in the industry.



David Kahn

David Kahn is a software I/O Architect at Sun Microsystems, Inc. David has been involved in industry standard activities including Open Firmware and several bus standards. At Sun, David was part of the original team that created the Sun Device Driver Interface specification.

Asad Khan

Asad Khan is a lead design verification engineer for PCI Express Switch project at Texas Instruments. He specializes in ground-up development of verification architectures with a focus towards coverage-driven verification, efficient self-checking reference modeling techniques, and definition of verification methodologies. Asad graduated with BSEE (Summa Cum Laude) in 2001 from University of Texas at Arlington.



Erez Kovshi

Erez Kovshi is Cadence's Engineering Manager for PCI Express Verification IP. He's been creating random and coverage driven verification IP for over 6 years. His expertise in e, Specman, vManager and advanced verification technologies is key to Cadence's Verification IP development. Erez holds a BSC in computer science from Israel's Ben-Gurion University.



Michael Krause

Michael Krause is a member of the PCI-SIG Board of Directors, and participates in multiple PCI-SIG technical workgroups. Michael Krause joined Hewlett-Packard in 1985 where he is currently a HP Fellow Engineer focused on local and fabric I/O and IPC technology development and strategy. He also acts as the HP technical lead for PCIe as well as a co-author of the PCIe specifications.

Kannan Krishna

Kannan Krishna received his B.Tech. in Electrical Engineering from the Indian Institute of Technology, New Delhi, India, in 1990 and M.S. and Ph.D. degrees in Electrical and Computer Engineering from Carnegie Mellon University, Pittsburgh, PA, in 1991 and 1995 respectively. He has been employed at AT&T Bell Labs, Texas Instruments Inc., and Accelerant Networks. Currently, he is with Synopsys, Inc., in Hillsboro, Oregon.



Dr. Mike Li

Dr. Mike Li is currently the Chief Technology Officer (CTO) with Wavecrest. Dr. Li pioneered jitter separation method (Tailfit) and DJ, RJ, and TJ concept and theory formation. He has been involved in setting and contributing to standards for jitter, noise and signal integrity for leading serial data communications, such as Fibre Channel, Gigabit Ethernet, Serial ATA, FB DIMM and PCI Express. He is Co-Chairman for the PCI Express jitter sub-workgroup. Dr. Li has published more than 70 papers in peer-reviewed technical journals and conferences and one book on high-speed design and test. He has filed 12 patents, with 4 granted and 8 pending.



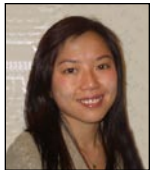
Wayne Locke

Wayne Locke, currently Director of Engineering Services at ChipX, has over 20 years experience in the IC business. He has worked on a variety of design technologies including CPUs, DSP, wireless SoC and ASIC at Texas Instruments, VLSI Technology, Prairiecomm, and ChipX. He is a key part of the team responsible for ChipX latest product introductions, which include PCI Express technology.



Betty Luk

Betty Luk is a PCIe hardware engineer who has spent the last three years in extensive PCIe debugging and co-validation with ATI Technologies' key partners and OEMs. Betty has a B.A. Sc. in E.E. from the University of Waterloo and a M. Eng. in E.E. from Cornell.



Purna Mohanty

Purna Mohanty is the founder and Vice-President at ASIC Architect, Inc. Before founding ASIC Architect, Inc., Purna served at senior engineering and management positions at Adaptec and Philips. Purna comes from a strong ASIC/SoC background specializing in storage and networking.



Chris Pettey

Chris Pettey, CTO and co-founder of NextIO, has more than 15 years of experience delivering high-performance I/O silicon for PC's and Servers. Prior to NextIO, Chris was co-founder, CTO and a member of the Board of Directors of Banderacom, a semiconductor startup focused on InfiniBand. Before co-founding Banderacom, Chris was a chip architect and designer for Jato Technologies, a startup semiconductor company that delivered Gigabit Ethernet. Chris joined Jato after several years at Compaq (now part of HP) where he worked in several engineering capacities

developing silicon and standards for server I/O. Chris began his career with NCR.

Gary Pratt

Gary Pratt is the manager of high speed partnerships for Mentor Graphics Corp.'s System Design division. He is a graduate of the University of Wisconsin at Madison, a member of IEEE, and a licensed professional engineer with 23 years experience in power electronics; control systems; digital image and signal processing; analog, digital and software design; and engineering management. Pratt has been an evangelist for emerging EDA technologies throughout his career.



Jeffrey Reynolds

Jeffrey Reynolds is a Technical Marketing Manager for ARM Physical IP since 2004, working with the 130nm and 90nm high speed SerDes IP offerings. Prior to this, he worked for Texas Instruments in their ASIC group and Defense groups working with SerDes solutions and packaging solutions. He has taught numerous classes on multi-gigabit system design and considerations. Born in Arkansas in 1971, Jeff holds a MSEE from the University of Arkansas in Radar and Microwave Communications and a BSEE from Louisiana Tech University. He lives in Richardson, TX with his wife.

Gene Saghi, PhD., P.E.

Dr. Gene Saghi is a co-founder, director, and principal engineer at Astek Corporation. During the last 6 years he has been a key contributor on several PCI-X and PCIe core designs. Prior to founding Astek, he served as an Assistant Professor at the University of Idaho and as a member of the technical staff at Texas Instruments. Dr. Saghi earned a BSEE from Wichita State University, a MEng in EE from Cornell University, and a PhD in EE from Purdue University.



Ron Shaw

Ron Shaw is a technology strategist in the office of the CTO at Dell. He is a member of the board of directors of PCMCIA, chairman of the Mobile Advisory Council, and the chair of the PCI-SIG Mini-Card Workgroup.



Vigyan Singhal

Vigyan Singhal is the President of Oski Technology. Previously, he founded Jasper Design Automation, and was a Research Scientist at Cadence Design Systems. He has taught design verification at UC Santa



Cruz extension. Vigyan received a Ph.D. in EECS from UC-Berkeley, and a B.Tech. from IIT Kanpur in India.

Richard Solomon

Richard Solomon is an IC Design Engineer with LSI Logic's Storage Standard Products Division. He is the architect of the PCI-X and PCIe interface cores used in LSI Logic's storage chips. Richard holds a B.S.E.E. from Rice University and 13 US Patents, of which five relate to PCI technology.



Gerry Talbot

Gerry Talbot is a Senior AMD Fellow, his primary focus is high speed I/O design, involving the development of, and contributing to, industry standard specifications such as HyperTransport™, PCIe, PCI-X 266/533 and FBDIMM. His work involves silicon circuit design, system level jitter modeling, interconnect channel modeling and signal integrity simulation.



Govinda Tatti

Govinda Tatti is a senior I/O software engineer working at Sun Microsystems since 1997. He has played a major role in the development of USB, PCI Express, and new DDI (Device Driver Interfaces) interrupt frameworks for the Solaris Operating system.



Mahesh Wagh

Mahesh Wagh is a Senior Platform Architect with Intel Corporation, focusing on platform architecture, interconnect technologies and interfaces. He has experience in the platform architecture, component micro-architecture and design development on client and server platforms.

Joe Winkles

Joe Winkles is a Senior Staff Engineer and instructor with MindShare, where he has trained well over 1,000 engineers since joining MindShare in 2003. He is an industry expert on such topics as PCI Express, HyperTransport, AMD Opteron Processors, and Intel IA32 processors. Joe was the technical editor of MindShare's PCI Express System Architecture book. Before joining MindShare, Joe was a chip designer with AMD.

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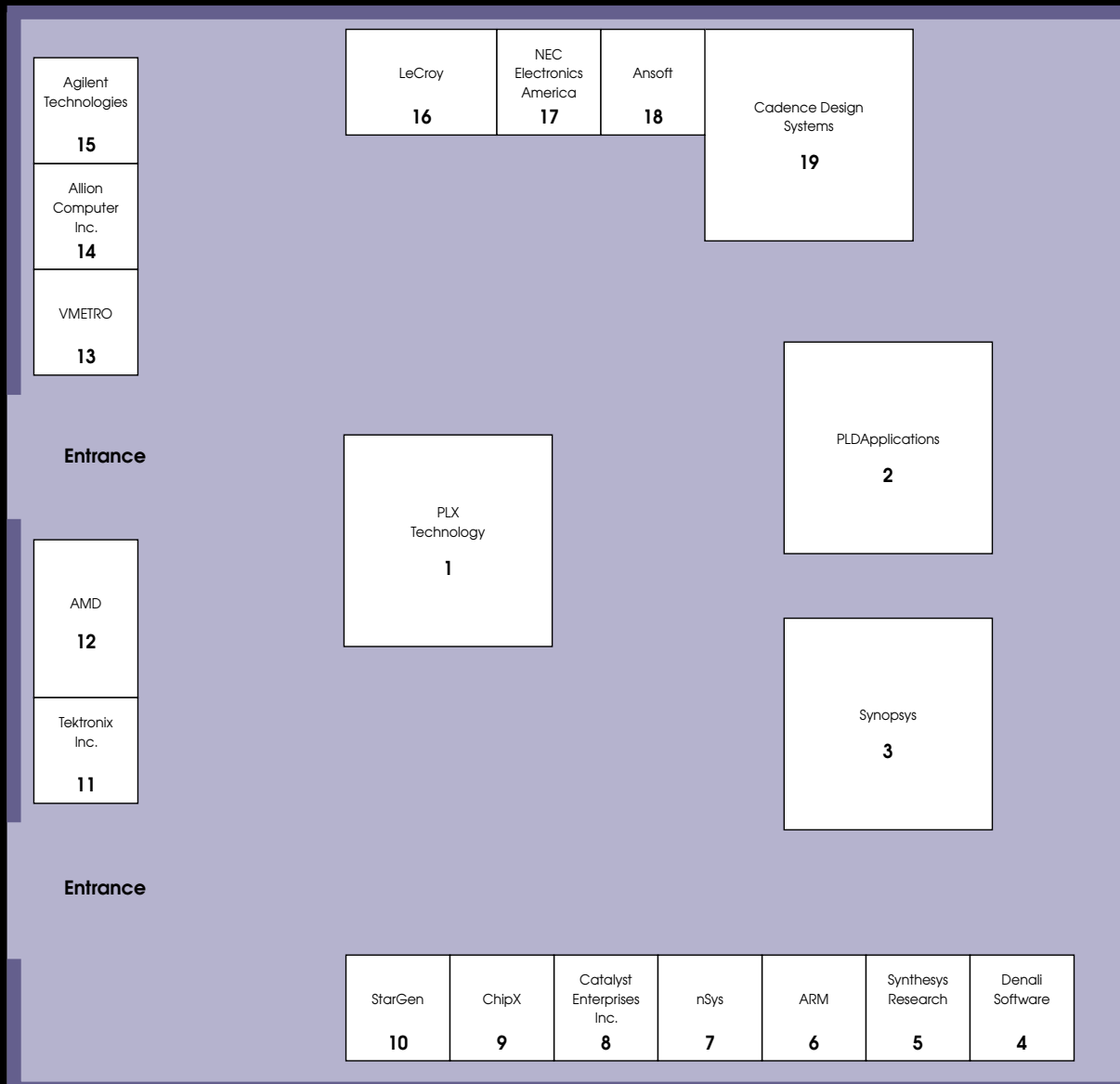
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Exhibit Area Floor Plan



Company	Booth #	Company	Booth #
Agilent Technologies	15	NEC Electronics America	17
Allion Computer Inc.	14	nSys	7
AMD	12	PLDApplications	2
Ansoft	18	PLX Technology	1
ARM	6	StarGen	10
Cadence Design Systems	19	Synopsys	3
Catalyst Enterprises Inc.	8	Synthesis Research	5
ChipX	9	Tektronix Inc.	11
Denali Software	4	VMETRO	13
LeCroy	16		

