



NEWS RELEASE

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PCI-SIG DELIVERS PCI EXPRESS 2.0 SPECIFICATION

PCIe Base 2.0 specification doubles the transfer rate to 5GT/s and introduces enhanced features and protocol improvements

BEAVERTON, Ore. – January 15, 2007 – PCI-SIG®, the Special Interest Group responsible for PCI Express® industry-standard I/O technology, today announced the availability of the PCI Express Base 2.0 specification. After a 60-day review of revision 0.9 of the specification in Fall 2006, members of the PCI-SIG finalized and released PCI Express (PCIe) 2.0, which doubles the interconnect bit rate from 2.5GT/s to 5GT/s to support high-bandwidth applications.

The specification seamlessly extends the data rate to 5GT/s in a manner compatible with all existing PCIe 1.1 products currently supporting 2.5GT/s signaling. The key benefit of PCIe 2.0 is its faster signaling, effectively increasing the aggregate bandwidth of a 16-lane link to approximately 16 GB/s. The higher bandwidth will allow product designers to implement narrower interconnect links to achieve high performance while reducing cost.

“In today’s world, applications are becoming more advanced and are requiring more bandwidth,” said Al Yanes, PCI-SIG chairman and president. “This is the perfect time to release PCIe 2.0, which not only supports high-bandwidth applications such as high-end graphics, but also adds many new architectural enhancements.”

In addition to the faster signaling rate, PCI-SIG working groups also added several new protocol layer improvements to the PCIe Base 2.0 specification which will allow developers to design more intelligent devices to optimize platform performance and power consumption while maintaining interoperability, low cost and fast market introduction. These architecture improvements include:

- Dynamic link speed management allows developers to control the speed at which the link is operating
- Link bandwidth notification alerts platform software (operating system, device drivers, etc) of changes in link speed and width
- Capability structure expansion increases control registers to better manage devices, slots and the interconnect
- Access control services allows for optional controls to manage peer-to-peer transactions

- Completion timeout control allows developers to define a required disable mechanism for transaction timeouts
- Function-level reset provides an optional mechanism to reset functions within a multi-function device
- Power limit redefinition enables slot power limit values to accommodate devices that consume higher power

The PCIe Base 2.0 specification is available for download at <http://www.pcisig.com/specifications/pciexpress/base2/>.

About PCI-SIG

PCI-SIG is the Special Interest Group that owns and manages PCI specifications as open industry standards. The organization defines and implements new industry standard I/O (Input/Output) specifications as the industry's local I/O needs evolve. The PCI Special Interest Group was formed in 1992, and the organization became a nonprofit corporation, officially named "PCI-SIG" in the year 2000. Currently, more than 850 industry-leading companies worldwide are active PCI-SIG members. PCI-SIG's current directors are employed by the following PCI-SIG member companies: AMD, Broadcom, HP, IBM, Intel, LSI Logic, Microsoft and nVIDIA. For more information about PCI-SIG, and PCI-SIG membership benefits, contact PCI-SIG by phone, at 503-619-0569, or by fax at 503-644-6708, or visit the PCI-SIG web site at: www.pcisig.com.

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