



**PCI Express™ 2.0
Frequently Asked Questions
PCI-SIG**

- 1. When will the PCIe 2.0 specification be available? How can I get a copy?**
PCI-SIG expects to deliver the release candidate (v0.9) for the PCIe 2.0 Base specification in Q4 2006 to its members for review. The v0.7 of the PCIe 2.0 Card Electromechanical (CEM) specification will also be delivered in the same timeframe. Visit www.pcisig.com to become a member and access the specification.
- 2. What prompted the need for another generation of PCI Express (PCIe™)?**
The PCIe 1.1 specification was developed to meet the needs of most I/O platforms. However a few applications, such as graphics, continue to require more bandwidth in order to enrich user experiences. PCI-SIG also saw the opportunity to add new functional enhancements (listed below), as well as incorporate all edits it had received to the PCIe 1.1 spec (via ECNs). In response to these needs, PCI-SIG developed PCI Express 2.0 (PCIe 2.0). It provides faster signaling, which doubles the bit rate from 2.5GT/s to 5GT/s.
- 3. What are the benefits of PCIe 2.0? What business opportunities does it bring to the market?**
While doubling the bit rate satisfies high-bandwidth applications, faster signaling has the advantage of allowing various interconnect links to save cost by adopting a narrow configuration. For example, a PCI Express 1.1 x8 link (8 lanes) yields a total aggregate bandwidth of 4GBytes/s, which is the same bandwidth obtained from a PCI Express 2.0 x4 link (4 lanes) that adopts the 5GT/s signaling technology. This can result in significant savings in platform implementation cost while achieving the same performance level. Backward compatibility is retained as existing 2.5 GT/S adapters can plug into 5.0 GT/S slots and will run at the slower rate. Conversely, new PCIe 2.0 adapters running at 5.0 GT/S can plug into existing PCIe slots and run at the slower rate of 2.5 GT/S.
- 4. It sounds as if both speed grades are supported in the PCIe 2.0 specification?**
The PCIe Base 2.0 specification supports both 2.5GT/s and 5GT/s signaling rates, in order to retain backward compatibility with existing PCIe 1.0 and 1.1 systems. Aside from the faster bit rate, there are a number of improvements in this new specification that allow greater flexibility and reliability in designing PCIe links. For example, the interconnect can be dynamically managed for platform power and performance considerations through software controls. Another

significant RAS feature is the inclusion of new controls to allow a PCIe link to continue to function even when some lanes become non-operational.

5. **Then PCIe 2.0 must be backward compatible with PCIe 1.1 and 1.0?**

Yes. The PCIe Base 2.0 specification supports both the 2.5GT/s and 5GT/s signaling technologies. A device designed to the PCIe Base 2.0 specification may support 2.5GT/s, 5GT/s or both. However, a device designed to operate specifically at 5GT/s must also support 2.5GT/s signaling. The PCIe Base specification covers chip-to-chip topologies on the system board. For I/O extensibility across PCIe connectors, the Card Electromechanical (CEM) and ExpressModule™ specifications will also need to be updated, but this work will not impact mechanical compatibility of the slots, cards or modules. Currently, the PCI-SIG is defining the PCIe CEM 2.0 specification which has been released to members for review at v0.5. There are currently no plans to adapt the PCIe Mini CEM specification for the faster bit rate as the market need has not yet materialized.

6. **What other new features are introduced in the PCIe 2.0 specification?**

The most predominant new feature in PCIe 2.0 is 5GT/s speed, which includes new mechanisms for software control of link speed, reporting of speed and width changes, and control of loopback. Other new features include:

Enhanced Completion Timeout Control, which includes required and optional aspects, reduces false timeouts and increases the ability to 'tune' the timeouts

Function Level Reset and Access Control Services, giving enhanced robustness and support of certain IOV features (optional)

Slot Power Limit Changes to allow for higher powered slots, which support the newer, high-performance graphics cards. This new feature works in tandem with the 300W Card Electro-mechanical specification

Speed Signaling Controls to enable software to determine whether a device can operate at a specific signaling rate, which can be used to reduce power consumption, as well as provide gross level I/O to memory

7. **What are the initial target applications for PCIe 2.0?**

The same set of core applications, high-performance graphics, enterprise-class storage and high-speed networking that benefited from the introduction of PCIe 1.0 architecture are expected to lead the charge for adoption of PCIe 2.0.

8. **What test tools and other infrastructure will be available to support the development of PCIe 2.0 products?**

The established PCIe ecosystem will deliver both pre-silicon and post-silicon tools to assist design engineers with implementing PCIe 2.0 products. In addition, the PCI-SIG will provide updated hardware test fixtures and test software upgrades to facilitate compliance verification at its Compliance Workshops.

9. **Are there details available for the Compliance Program for PCIe 2.0 products?**

PCI-SIG is currently working on the necessary upgrades to its suite of compliance tools, tests and fixtures to support the initial wave of PCIe 2.0 products. PCI-SIG will make timely member announcements when these details are ready and available.

10. What enhancements to the PCIe specification are anticipated for the future?

PCI-SIG is continually evaluating the need to enhance the PCIe architecture. Because the PCIe architecture is layered, it allows for the flexibility of extending various layers without impacting other layers. With the PCIe 2.0 specifications, for example, the PCI-SIG has addressed market requirements for enhanced performance by doubling the bit rate to 5GT/s. This enhancement is limited to the electrical layer of the protocol stack. The PCI-SIG is also working on I/O device virtualization extensions to the PCIe protocols. In the future, it can be expected that both the signaling and the protocol layers of the PCIe architecture will be extended to keep abreast of the industry's need for faster signaling, as well as more robust and functional protocols.

11. I've heard mention that PCI-SIG is working on a new graphics spec – what is it? How is it different from the existing PCIe x16 Graphics 150watt-ATX 1.0 spec?

PCI-SIG is developing a new specification to deliver increased power to the graphics card in the system. This new specification is an effort to extend the existing 150watt power supply for high-end graphics devices to 225/300watts. The PCI-SIG is developing some boundary conditions (e.g. chassis thermal, acoustics, air flow, mechanical, etc.) as requirements to address the delivery of additional power to high-end graphics cards through a modified connector. A new 2x4 pin connector supplies additional power in the 225/300w specification. These changes will deliver the additional power needed by high-end GPUs. The PCI-SIG expects the new specification to be complete in 2007.

12. Where can interested parties get more information?

PCI-SIG is the sole source for PCIe specifications. In addition, both the PCI-SIG and its members provide a plethora of technical and marketing collateral in support of the PCIe architecture. Please visit www.pcisig.com for additional information.

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