



PCI Express® 4.0 Specification Frequently Asked Questions PCI-SIG®

Q: What is PCI Express® (PCIe®) 4.0? What are the requirements for this evolution of the PCIe architecture?

A: PCIe 4.0 is the next evolution of the ubiquitous and general-purpose PCI Express I/O specification. At 16GT/s bit rate, the interconnect performance bandwidth will be doubled over the PCIe 3.0 specification, while preserving compatibility with software and mechanical interfaces. The key requirement for evolving the PCIe architecture is to continue to provide performance scaling consistent with bandwidth demand from a variety of applications with low cost, low power and minimal perturbations at the platform level. One of the main factors in the wide adoption of the PCIe architecture is its sensitivity to high-volume manufacturing capabilities and materials such as FR4 boards, low-cost connectors and so on.

Q: When will PCIe 4.0 be released?

A: The final PCIe 4.0 specifications, including form factor specification updates, are expected to be available sometime in the 2014-2015 timeframe. The timing of the specification maturity is a function of the participation and contributions of PCI-SIG members as the technical workgroups consider and debate technology choices, capabilities and analyses.

Q: What is the bit rate for the PCIe 4.0 specification and how does it compare to prior generations of PCIe?

A: Based on PCI-SIG feasibility analysis, the bit rate for the PCIe 4.0 specification will be 16GT/s. This bit rate represents the optimum tradeoff between performance, manufacturability, cost, power and compatibility. PCI-SIG analysis covered multiple topologies. All of these studies confirmed the potential feasibility of 16GT/s signaling with low-cost enablers.

Q: What are the results of the feasibility testing for the PCIe 4.0 specification?

A: After technical analysis, the PCI-SIG has determined that 16 GT/s on copper, which will double the bandwidth over the PCIe 3.0 specification, is technically feasible at approximately PCIe 3.0 power levels. The preliminary data also confirms that a 16GT/s interconnect can be manufactured in mainstream silicon process technology and can be deployed with existing low-cost materials and infrastructure, while maintaining compatibility with previous generations of PCIe architecture. In addition, the PCI-SIG will investigate advancements in active and idle power optimizations as they become available.

Q: What were the requirements outlined for the feasibility analysis?

A: In assessing potential improvements to the connector, materials, silicon and channel improvements, PCI-SIG required that compatibility, low-cost and high-volume manufacturing be maintained.

Q: Will PCIe 4.0 products be compatible with existing PCIe 1.x, PCIe 2.x and PCIe 3.x products?

A: PCI-SIG is proud of its long heritage of developing compatible architectures and its members have consistently produced compatible and interoperable products. In keeping with this tradition, the PCIe 4.0 architecture is compatible with prior generations of this technology, from software to clocking architecture to mechanical interfaces. That is to say PCIe 1.x, 2.x and 3.x cards will seamlessly plug into PCIe 4.0-capable slots and operate at the highest performance levels possible. Similarly, all PCIe 4.0 cards will plug into PCIe 1.x-, PCIe 2.x- and PCIe 3.x-capable slots and operate at the highest performance levels supported by those configurations.

Q: Why is a new generation of PCIe architecture needed?

A: PCI-SIG responds to the needs of its members. As applications evolve to consume the I/O bandwidth provided by the current generation of the PCIe architecture, PCI-SIG begins to study the requirements for technology evolution to keep abreast of performance and feature requirements.

Q: What are the initial target applications for the PCIe 4.0 architecture?

A: The PCIe 4.0 specification will address the many applications pushing for increased bandwidth at a low cost including server, workstation, desktop PC, notebook PC, tablets, embedded systems, peripheral devices, high-performance computing markets and more. The target implementations are entirely at the discretion of the designer.

Q: Is PCIe 4.0 architecture more expensive to implement than PCIe 3.x?

A: PCI-SIG attempts to define and evolve the PCIe architecture in a manner consistent with low-cost and high-volume manufacturability considerations. While PCI-SIG cannot comment on design choices and implementation costs, optimized silicon die size and power consumption continue to be important considerations that inform PCIe specification development and architecture evolution.

Q: Will there be a new compliance specification developed for the PCIe 4.0 specification?

A: For each revision of its specification, PCI-SIG develops compliance tests and related collateral consistent with the requirements of the new architecture. All of these compliance requirements are incremental in nature and build on the prior generation of the architecture. PCI-SIG anticipates releasing compliance specifications as they mature along with corresponding tests and measurement criteria. Each revision of the PCIe technology maintains its own criteria for product interoperability and admission into the PCI-SIG Integrators List.