PCI-SIG® Technologies

PCI-X™ 2.0: High-Performance, Backward-Compatible PCI for the Future

PCI-X™ 2.0 is an evolutionary, backward compatible technology that builds on the foundation of PCI and PCI-X 1.0b while offering bandwidths 4 times higher than PCI-X 1.0b™ without increasing pin-count. These new, higher bandwidths are ideal for future server-oriented adapter cards in the areas of Fibre Channel, RAID, networking, InfiniBand™ Architecture, SCSI, iSCSI, and other high-bandwidth technologies. The migration to PCI-X 2.0 is simplified by the fact that it is both hardware and software compatible with PCI-X 1.0b and PCI. PCI-X 2.0 design and implementation are also made easy because many elements of PCI-X 1.0b are retained. There are also hundreds of products currently available that can seamlessly connect with PCI-X 2.0. Some of the key features include:

- Hardware and software backward compatibility to all speed grades of PCI and PCI-X.
- Thousands of compatible adapter cards currently available.
- Offers performance 32 times faster than the first generation of PCI.
- ECC support for both header and payload for enhanced system reliability, including automatic single-bit error recovery and double-bit error detection.
- Cost model leverages 10 years of PCI device, card, and connector volumes.
- Addresses requirements of multiple market segments in the computing and communications industries.
- Suitable for board-to-board, add-in peripherals and backplane implementations.
- Low-overhead, low-latency data transfers and maximized interconnect efficiency.
- High-bandwidth, 16-bit implementations for space-constrained applications.
- Performance scaling through interconnect width and frequency bumps.
- Advanced error reporting and handling for fault isolation and system recovery.
- Automatic power management functions to conserve power when the bus is idle.
- Hot plug and hot swap capabilities with compatible support for existing PCI hot-plug schemes.
- Advanced peer-to-peer communications for streaming media.
- Workstation support

PCI Express™: Performance Scalability for the Next Decade

PCI Express™ Architecture is a state-of-the-art serial interconnect technology from the PCI-SIG that delivers performance headroom and advanced features for expected processor and memory subsystem improvements over the next decade. Its initial release at 0.8V and 2.5GHz signaling rate supports configurations consisting of 1, 2, 4, 8, 12, 16 and 32 lanes which can yield up to 16 Giga Bytes per second of bandwidth. Future frequency increases promise to scale total bandwidth to the limits of copper. Even higher bandwidth can be achieved with other physical media without impacting levels above the Physical Layer in the protocol stack, thus allowing PCI Express™ technology to continue to seamlessly evolve well into the next decade and beyond.

The PCI Express Architecture retains the PCI usage model and software interfaces to facilitate a smooth development migration from existing PCI based designs. The technology is suitable for multiple market segments in the computing and communications industries, and supports chip-to-chip, board-to-board and adapter solutions at an equivalent or lower cost structure than existing PCI designs. Investment preservation is maintained through backwards compatibility to existing PCI software as well as headroom for performance scalability in both interconnect width and frequency as required.

The PCI Express technology offers a rich feature set that address multiple usage models in the computing and communications industries. For example, high-performance graphics and multimedia, interconnects such as 1394b, USB 2.0 and Gigabit Ethernet benefit from its native power management, ease and low cost of implementation, the ability to match bandwidth to the application, isochronous data delivery and flexible form factors. Interconnects such as InfiniBand™ Architecture, 10Gb Fibre Channel and 10Gb Ethernet work well with its features such as low latency data transfers, native RAS functionality including hot plug, simplified signal routing and flexible connectivity. Other implementations can benefit

from its high-availability features such as distributed processing, quality of service, latency control, advanced message passing, flow control, and multicast.

- PCI software compatibility
- Scalable performance for multiple computing and communications market segments
- Suitable for chip-to-chip, board-to-board, add-in peripherals and backplane implementations
- Support for end-to-end data integrity to achieve highly-available solutions
- Advanced error reporting and handling for fault isolation and system recovery
- Native power management functions for flexible platform power budgeting
- Inherent hot plug and hot swap capabilities with compatible support for existing PCI hot-plug schemes
- Low-overhead, low-latency data transfers and maximized interconnect efficiency
- Differentiated services through isochronous data delivery for bandwidth-sensitive applications
- Multi-hierarchy and advanced peer-to-peer communications across fabric topologies
- High-bandwidth, low pin-count implementations for optimized performance
- Cost effective silicon component designs relative to package and die-area

PCI Hot-Plug™: Advancing PCI to Better Support Mission Critical Servers

PCI Hot-Plug™ allows the removal and insertion of devices without having to turn off a server, therefore maximizing uptime, and allowing IT managers to build in redundancy. The adoption of the specification is important for businesses that operate in mission-critical server environments. Today, PCI Hot-Plug is a "must have" for most server markets. To further expand the standard, the PCI-SIG has recently released the new *PCI Standard Hot-Plug Controller and Subsystem Specification*. This will help lower the cost of hot-plug systems and enable standard operating systems to include native support for PCI Hot-Plug. The *PCI Hot-Plug Specification* and the *PCI Standard Hot-Plug Controller and Subsystem Specification* are both available to PCI-SIG members and can be downloaded from www.pcisig.com.

PCI-X 1.0b™: A High-performance Extension to the PCI Bus Architecture

PCI-X 1.0b™ is a backward compatible high-performance extension to the PCI Bus. PCI-X 1.0b is shipping today in servers that require higher bandwidth, with potential use in workstations.

Running at frequencies of up to 133 MHz at either 32-or 64-bit widths, PCI-X 1.0b is designed to bring the PCI Local Bus data throughput performance to over 1 Gbyte/second (8 Gbits/sec). PCI-X 1.0b brings more efficient bus operation, allowing easier interfacing with memory controllers, bridges and other advanced I/O solutions. Other details include:

- Split Transactions allow an initiator device to make only one data request and relinquish the bus, rather than constantly polling the bus for a response.
- Byte Count enables initiator to specify in advance the number of bytes requested, eliminating the inefficiency of speculative pre-fetches.
- Improved error handling allows recovery from some kinds of data parity errors
- Relaxed transaction ordering improves performance in complex multi-CPU systems and in real-time applications

The PCI-X 1.0b specification is available to PCI-SIG members and can be downloaded from www.pcisig.com.

PCI 2.3 – An Evolution of the Conventional PCI Specification

Revision 2.3 is an evolutionary change to the PCI Local Bus Specification. Revision 2.3 makes a significant step in migrating the PCI bus from the original 5.0 volt signaling, to a 3.3 volt signaling bus. Revision 2.3 supports the 5V and 3.3V keyed system board connectors (as did revision 2.2) but revision 2.3 supports only the 3.3V and Universal keyed add-in cards. The 5V keyed add-in card is not supported in revision 2.3. PCI 66, PCI-X 1.0b, Mini PCI, and Low Profile PCI support only 3.3 volt signaling on 3.3V keyed system board connectors and 3.3V and Universal keyed add-in cards.

High performance technologies power the logic within the chips with 3.3 or lower voltages. The newer high performance technologies cannot support 5 volt compatible signaling on the off-chip drivers. As a result, the host bridge needs to migrate to 3.3 volt signaling with 3.3V keyed system board connectors. Removing support for 5V keyed add-in cards is the first step

in the migration to 3.3 volt signaling systems and ensures revision 2.3 compliant add-in cards will be usable in 3.3V keyed system board connectors.

In addition to the changes described above, revision 2.3 also incorporates other ECNs and approved errata. Revision 2.3 PCI Local Bus Specification is available to PCI-SIG members and can be downloaded from www.pcisig.com.

PCI-SIG® – A Leading Standards Organization

Formed in 1992, the PCI Special Interest Group (PCI-SIG®) is the organization that develops and manages what has become one of the most successful I/O bus standards, the PCI Local Bus specification. Through wide industry support and active developer participation, the PCI Local Bus specification has been a well-maintained, open and non-proprietary solution that is scalable and retains legacy compatibility for today's applications. In addition to the advancement of the PCI specification, the PCI-SIG educates the industry on the latest developments of the PCI Local Bus through technical seminars. The Compliance Workshops (Plugfests) provide forums for testing of interoperability of the many PCI-related systems and software in the market. The PCI-SIG has continued to develop successful extensions to the PCI Local Bus, such as PCI-X 1.0b and Mini PCI™, as industry needs evolve. For information on how to become a member of the PCI-SIG go to www.pcisig.com.