

This paper describes the differences between the review draft and the Final version of the PCI Local Bus specification revision 2.2. Following this description is a list of the changes between the 2.1 version and the 2.2 draft. Please refer to the PCI SIG WebPages (www.pcisig.com in the member's only section) for the latest information.

Changes from draft copy to the Final version.

- 1) The Spread Spectrum Clocking (SSC) was included. SSC is used to meet EMI requirements by slowly changing the CLK frequency to spread the EMI energy. See the SSC ECR on the WebPages or section 7.6.4.1. (Clock Specification) for details.
- 2) Clarified that if a device supports MSI and DAC as a master, then the device must support the 64-bit (address) register layout for MSI. See section 6.8.1 (Message Capability Structure) for details.
- 3) Clarified the receiver of MSI messages have no requirement to ensure that they are serviced in the order that they were received. See section 6.8.2.2. (MSI Transaction Reception and Ordering Requirements)
- 4) Many edits to improve readability, typos, references and spelling.
- 5) Fixed some mechanical figures to included missing dimensions, and redrew to improve readability.
- 6) Removed all references to SBO# and SDONE.

The remainder of this paper gives an overview of the differences between revisions of 2.1 and the 2.2 draft version of the PCI Local Bus specification. This list is not comprehensive and the Final version should be used. It is highly recommended that previous versions (including draft copies) should not be used for future designs.

Preface

Added pointer to webpage for latest information. Updated ECR list.

Chapter 1 Introduction

Corrected contact information for the SIG. Address, phone numbers, fax, and Email addresses.

Chapter 2 Signal Definition

Added new pins and their description that have been approved via the ECR process. Added reference to the RST# description to highlight that special attention needs to be given to AD[63:32], C/BE[7::4]# and PAR64. Replaced two sentences with a reference to the error handling section. The two sentences did not give a complete understanding of the use of PERR#. The reference helps the reader locate the correction section where a detailed description occurs.

Chapter 3 Bus Operation

Section 3.1.2. Command Usage Rules

Restored a paragraph that was inadvertently deleted in the 2.1 update. The paragraph describes the requirement on a target that supports memory space. The target is not required to support all the memory commands (MRM, MRL, MR, MWI and MW) but is required at a minimum to decode all five commands and alias them to the basic memory read or write command.

Section 3.2.2. Addressing

Rewrote this section to improve readability. This section now has subsections for Memory, I/O and Configuration spaces. Discussion about how configuration space is accessed, how a device devices this space and how the host bus bridge generates configuration cycles has been moved to this section. Discussion about compatibility issues has been moved to Appendix G.

Section 3.3.3.2.2. Requirements on a Master Because of Target Termination

Clarified the requirements on a multifunction device that is terminated when STOP# is asserted. The clarification list three specific cases, a single function device that has independent functions internally, a multifunction device and a PCI to PCI Bridge. The clarification states the device is

only required to deassert REQ# for two clocks before allowing the “function” that was terminated with Retry or disconnect from repeating its request.

An Implementation Note named “Potential Temporary Livelock and Resulting Performance Impacts” was added. It describes some consequences when a master does not comply with the requirement to repeat a request terminated with Retry.

Section 3.3.3.3.2. Information Required to Complete a Delayed Transaction

The initial paragraph was rewritten to improve the clarity of what is required to be latched for a delayed transaction. The requirements for completing a delayed read and write transactions are not discussed separately.

Section 3.5.1.1. Target Initial Latency

Incorporates the RST# ECR changes which specify when a device can be accessed following the deassertion of RST# and what is it allowed to do if accessed during this time. From the time RST# is deasserted until $2^{**}25$ PCI clocks the target can do the following: Ignore the request, claim the access and holding in waitstates until ready to complete the request (no initial latency requirement) or Retry the request. After $2^{**}25$ clocks, the target is required to meet the initial latency time. No accesses can occur before 5 clocks after RST#.

Section 3.5.3 Memory Write Maximum Completion Time Limit

Incorporated the Max. Completion ECR. Requires the target to accept a memory write transaction within 10 microseconds.

Section 3.6 Exclusive Access

This section has been moved to Appendix F. The use of LOCK# has been restricted such that only a bridge is allowed to use lock to prevent a deadlock and for compatibility issues. No other device is allowed to use LOCK#.

Section 3.8 Error Functions

This section has been totally re-written to improve the readability. Error discussions that were in others parts of the spec have been moved to this section with a reference from the previous locations.

Section 3.10 Cache Support

Cache Support in the 2.2 version is being dropped. For the review copy this section is being moved to Appendix X. It is being proposed that Appendix X be dropped when the final version of 2.2 is completed.

Section 3.11.2 Determining Bus Width During System Initialization

Material from various parts of the spec has been consolidated in this new section. It discusses the meaning of REQ64# and ACK64# when RST# is deasserted. It discusses how a device can tell if it is connected to 32 or 64-bit data path.

Section 3.12 Special Design Considerations, item #6 Potential data inconsistency when an agent uses delayed transaction termination

Another description of the same inconsistency was added. The master changes how it completes a transaction that was terminated with Retry because it received information after the request was terminated with Retry. It extends the burst read because additional data is now valid, instead of completing the request as it had initiated it.

Section 3.12 Special Design Considerations, Item #7 is added. A PCI Host Bus Bridge is not required to support PCI peer-to-peer transactions that traverse multiple PCI host bus bridges.

Section 3.12 Special Design Considerations, Item #8 is added. The effect of a PCI -to-PCI bridge on the PCI clock specification.

There are two clarifications.

1. If the bridge is on the add-in card, the secondary devices have to tolerate a degraded clock.

2. If the bridge is on the system board, the clock INTO the bridge must be better than the spec requires such that the clock AT the connector meets the spec.

Section 3.12 Special Design Considerations, Item #9 is added. Devices cannot drive and receive signals at the same time.

The timing budget does not allow the device to use as inputs bus signals that it is driving as outputs.

Chapter 4 Electrical Specification

Section 4.3.4.1. Power Requirements, now requires the system designer to provide 3.3 V rail in the connector. Before it was not required, but system designer was to provide a way to add it.

Relocated some information about REQ64#/ACK64# during reset to chapter 3. Updated Reset figure (4-12) per RST# ECR. Added a clarification that a device is not allowed to use a signal as an input if it is driving it as an output.

Incorporated Tprop ECR into section 4.3.5.

Chapter 5 Mechanical Specification

Incorporated ECRs, M1-M6.

Chapter 6 Configuration Space

Section 6.2.4. -- Added more detail to the description of the MIN_GNT and MAX_LAT registers.

Section 6.2.5. Base Address -- Clarified the use of the Base Address and Expansion ROM registers.

The configuration software will write FFFF FFFFh to the BAR and read back the value that specifies the amount of the resource the device is requesting. Software determines the size by determining which bits are read-only (return zero when read) and which are read/writable.

This boundary will be a naturally aligned power of 2. Software then writes back the base address of the address range assigned to the device. The maximum memory allowed to be requested with a 32-bit memory BAR is 2 Gigabytes. Devices will not be allowed to request memory space below the 1 Meg (Software will continue to support requests from pre-2.2 devices.)

Section 6.4 Vital Product Data. All but introduction has been moved to Appendix J.

Section 6.7 User Definable Configuration Items removed from spec.

New Capabilities ECR has been incorporated into section 6.7.

Message Signaled Interrupts ECR has been incorporated into section 6.8.

Chapter 7 66 MHz PCI Specification

Clarified that a device cannot use a signal as an input when it drives the signal as an output.

Appendix A Special Cycle Messages

No Changes

Appendix B State Machines

Added Footnote about the only bridges can use LOCK#.

Appendix C Operating Rules

Clarified

Rule 10 – Section 3.3.3.2.2 Requirements on a Master Because of Target Termination

Rule 21 -- Adds that a master can start a transaction when the current transaction is in the last data phase if the master is going to do a fast back to back transaction.

Rule 25 -- Added reference that gives host bus bridges an exception to the initial latency rule.

Move rules 28-32 to Appendix F.

Appendix D Class Codes

Add that an updated list of class codes can be found the SIG's webpage as well as the form to submit a new one.

Appendix E System Transaction Ordering

Table E-1 has been corrected. The intersection Rows 4 and 5 and Columns 3 and 4 are required to be Yes and NOT Yes/No. Added explanation why these are required to be “Yes”.

Appendix F Exclusive Accesses

Moved from section 3.6. Lock usage only allowed by bridges to prevent deadlock or provide compatibility.

Appendix G I/O Space Address Decoding for Legacy Devices

Discussion of compatibility issues associated with legacy addresses is moved out of section 3.2.2.

Appendix H New Capabilities

Incorporated New Capabilities ECR.

Appendix I Vital Product Data

Moved from section 6.4. Incorporated the VPD ECR.

Appendix X Cache Support

Moved from section 3.10 to this appendix for the review draft. The protocol workgroup intends to remove all cache support from the specification in the final version of 2.2.