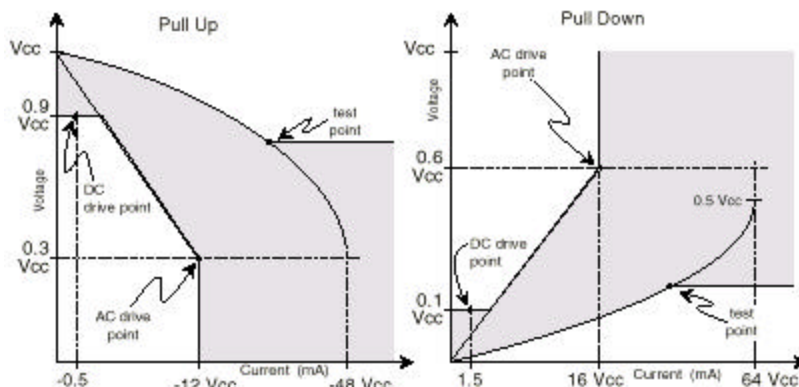


This paper lists the known errata for the Local Bus Specification Revision 2.2. If you have found others please mail them to techsupp@pcsig.com.

1. In Section 5.2, Expansion Card Physical Dimensions and Tolerances, Figures 5-1 and 5-2 have an error in the dimension for the I/O window height. The dimension (on the left side of each figure) should be 88.9 (3.50) rather than 89.9 (3.539). The correct dimension for this I/O window height can also be found in Figure 5-14.
2. Section 5.2.1, Connector Physical Description, page 172, there is an error in Figure 5-27. The location of Datum "A" in the lower half of the drawing is incorrectly shown to be on the right side of the slot. Datum "A" should reference the center of the slot, like it does in Figure 5-26 and the top part of Fig 5-27. There are three dimensions in Figure 5-27 that have the correct values, but should be referenced to the corrected Datum "A" (ie. the middle of the slot). Those dimensions (all in the lower part of the drawing) are 15.44 (0.608), 17.58 (0.692) and 58.62 (2.308).
3. In section 7.8 Expansion Board Specifications, page 237, a reference was left out. "Refer to Section 4.4." should appear at the beginning of this section. The 66 MHz board specifications are the same as 33 MHz except as noted in this section.
4. In section 7.6.4.1 there is a value in Table 7-3 that is incorrect. The maximum value for f_{spread} (frequency spread) should be 0%, not 9%.
5. The diagrams in Figure 4-4 are missing some text on the X-axis. The figures below (the same as appeared in the Rev. 2.1 specification) are correct. Along the X-axis, values including V_{cc} mean the number times V_{cc} expressed in milliamps. So the first value (-12 V_{cc}) means -12 times V_{cc} or -39.6mA (-12 * 3.3).



6. In Figure 3-1 on page 31, the some characters and numbers have been dropped. In the figure showing Type 0 Address Phase Format, the bit number on the left is 31 (not 1), the 'R' and 'd' is missing from 'Reserved' (upper 22 bits), and the 'R' is missing from 'Register Number' (bits 7-2). In the figure showing Type 1 Address Phase Format, a '3' is missing from the bit numbering '23' (next to 24), and the 'R' is missing from 'Register Number' (bits 7-2). Also, the text inside the diagrams is not readable when viewing the .pdf file (although they do appear when printed).
7. The diagrams in Figure 7-10 on page 235 are examples of an electrically short interconnect, and the actual waveforms at the load might be delayed by trace propagation. Also, Figure 7010(d) has an incorrect ending location for T_{prop} . T_{prop} is supposed to end where the Driving Bus curve crosses V_{test} (not V_{il}).
8. In section 4.3.5 on page 139 there are two reference to Figure 7-11 which should be references to Figure 7-10.