

## 1. PCI Engineering Change Notice – Power Valid to Reset High Timing Specification

<b>TITLE:</b>	Power Valid to Reset High Timing Specification
<b>DATE:</b>	December 6, 1999
<b>AFFECTED DOCUMENT(S):</b>	PCI Local Bus Specification, Revision 2.2, December 18, 1998 and PCI Compliance Checklist, Revision 2.2
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### 1.1. Clarification

This ECN adds a timing specification to the PCI specification in order to guarantee a minimum time between power valid and reset deassertion. The new relationship is called Tpvrh (power valid to reset high) and is a minimum of 100 ms.

### 1.2. Benefits

Devices that implement the 64-Bit Bus Extension are required to sample **REQ64#** on the rising edge of **RST#**. This presents a specific problem for PCI interfaces implemented in FPGAs.

Many FPGA devices load configuration data immediately after power is applied to the device. If an FPGA cannot finish loading its configuration data before the rising edge of **RST#** on the PCI bus, the FPGA will fail to sample **REQ64#**.

The lack of a relationship between power good and reset deassertion means that the only guaranteed time before the deassertion of reset is 1 ms (the PCI Local Bus Specification cites 100 ms as a typical value). In PCI-X, this problem becomes worse, since several critical signals are sampled at **RST#** deassertion. This change will make it easier to design both 64-bit PCI and PCI-X boards with FPGAs.

This ECN ensures that FPGA implementations of PCI bus interfaces will have sufficient time to configure after power is applied. This ECN only impacts the timing of any reset immediately after power is applied; it has no impact on subsequent resets.

These changes will allow FPGAs to be used at PCI interface devices in fully compliant PCI systems.

**1.3. PCI Local Bus Specification, Rev. 2.2 Changes**

**Chapter 4 “Electrical Specification”, Section 4.2.3.2 Timing Parameters, page 128:**

Change as shown below:

**Table 4-3: 5V and 3.3V Timing Parameters**

Symbol	Parameter	Min	Max	Units	Notes
$T_{val}$	CLK to Signal Valid Delay - bused signals	2	11	ns	1, 2, 3
$T_{val}(ptp)$	CLK to Signal Valid Delay - point to point	2	12	ns	1, 2, 3
$T_{on}$	Float to Active Delay	2		ns	1, 7
$T_{off}$	Active to Float Delay		28	ns	1, 7
$T_{su}$	Input Setup Time to <b>CLK</b> - bused signals	7		ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to <b>CLK</b> - point to point	10, 12		ns	3, 4
$T_h$	Input Hold Time from <b>CLK</b>	0		ns	4
$T_{rst}$	Reset active Time <b>after power stable</b>	1		ms	5
$T_{rst-clk}$	Reset active Time after <b>CLK STABLE</b>	100		$\mu$ s	5
$T_{rst-off}$	Reset Active to Output Float delay		40	ns	5, 6, 7
$T_{rrsu}$	<b>REQ64#</b> to <b>RST#</b> Setup time	$10 \cdot T_{cyc}$		ns	
$T_{rrh}$	<b>RST#</b> to <b>REQ64#</b> Hold time	0	50	ns	
$T_{rhfa}$	<b>RST#</b> High to First configuration Access	$2^{25}$		clocks	
$T_{rhff}$	<b>RST#</b> High to First <b>FRAME#</b> assertion	5		clocks	
$T_{pvrh}$	<b>Power valid to RST# high</b>	100		ms	

**Chapter 4 “Electrical Specification”, Section 4.3.2 Reset, page 133:**

Change as shown below:

**4.3.2 Reset**

The assertion and deassertion of the PCI reset signal (**RST#**) is asynchronous with respect to **CLK**. The rising (deassertion) edge of the **RST#** signal must be monotonic (bounce free) through the input switching range and must meet the minimum slew rate specified in Table 4-5. The PCI specification does not preclude the implementation of a synchronous **RST#**, if desired. The timing parameters for reset are contained in Table 4-6, with the exception of the  $T_{fail}$  parameter. This parameter provides for system reaction to one or both of the power rails going out of spec. If this occurs, parasitic diode paths could short circuit active output buffers. Therefore, **RST#** is asserted upon power failure in order to float the output buffers.

The value of  $T_{fail}$  is the minimum of:

- 500 ns (maximum) from either power rail going out of specification (exceeding specified tolerances by more than 500 mV)
- 100 ns (maximum) from the 5V rail falling below the 3.3V rail by more than 300 mV.

The system must assert **RST#** during power up or in the event of a power failure. In order to minimize possible voltage contention between 5V and 3.3V parts, **RST#** must be asserted as soon as possible during the power up sequence. Figure 4-11 shows a worst case assertion of **RST#** asynchronously following the "power good" signal.<sup>33</sup> After **RST#** is asserted, PCI components must asynchronously disable (float) their outputs, but are not considered reset until both  $T_{rst}$  and  $T_{rst-clk}$  parameters have been met.

The first rising edge of **RST#** after power-on for any device must be no less than  $T_{pvrh}$  after all the power supply voltages are within their specified limits for that device. If **RST#** is asserted while the power supply voltages remain within their specified limits, the minimum pulse width of **RST#** is  $T_{rst}$ .

Figure 4-11 shows **RST#** signal timing.

**Chapter 4 “Electrical Specification”, Section 4.3.2 Reset, Figure 4-11, page 135:**

Replace Figure 4-11 with the figure shown below:

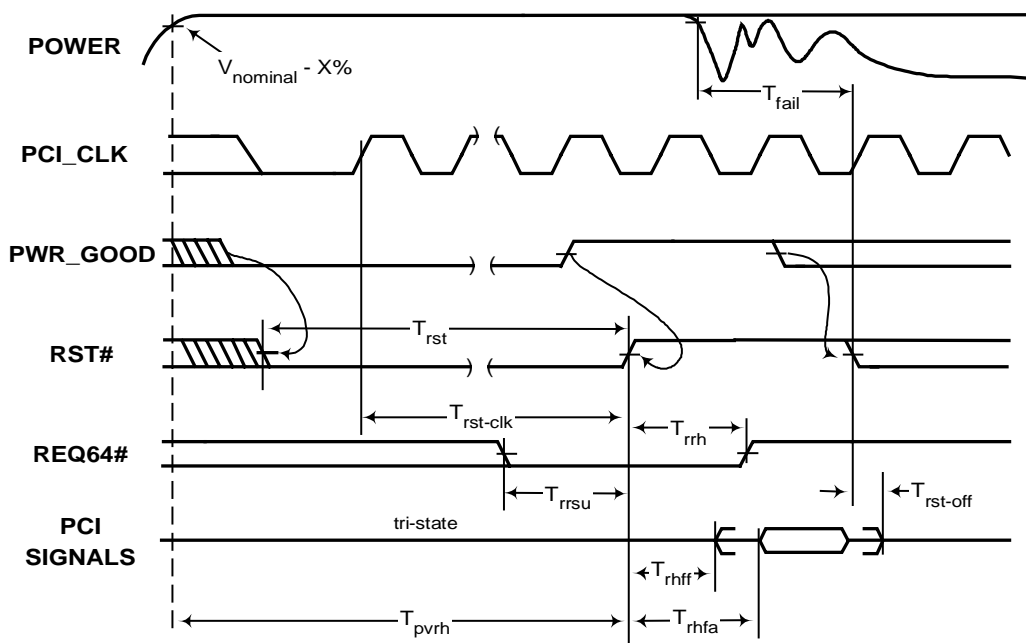


Figure 4-11: Reset Timing<sup>34</sup>

**1.4. PCI Compliance Checklist, Rev. 2.2 Changes**

**“Motherboard Electrical Checklist”, page 6:**

Change as shown below:

- ME1. All bussed PCI signals are driven by compliant components? yes \_\_\_ no\_\_\_
- ME1a. CLK cycle time is 30 ns minimum for 33 Mhz PCI, 15 ns to 30 ns for 66 Mhz PCI? yes \_\_\_ no\_\_\_
- ME2. CLK skew between any two receivers in the system is less than 2 nS for 33 Mhz PCI, 1 nS for 66 Mhz PCI? yes \_\_\_ no\_\_\_
- ME3. CLK is delivered to all components with at least 12nS of high/low time for 33 Mhz PCI, 6 nS for 66 Mhz PCI? yes \_\_\_ no\_\_\_
- ME4. (5V signaling) Peak-to-peak CLK swing is at least 2V (0.4V to 2.4V)? yes \_\_\_ na\_\_\_
- ME5. (3.3V signaling) P-t-p CLK swing is at least 0.4Vcc (0.2Vcc to 0.6Vcc)? yes \_\_\_ na\_\_\_
- ME6. Both edges of RST# are monotonic through the switching range? yes \_\_\_ no\_\_\_
- ME7a Power is stable for at least 100 mS prior to RST# de-assertion for each device? yes \_\_\_ no\_\_\_
- ME7b Minimum RST# active pulse width is 1mS? yes \_\_\_ no\_\_\_
- ME8. CLK is stable for at least 100uS prior to RST# de-assertion? yes \_\_\_ no\_\_\_
- ME9. RST# is asserted within 500nS after either 5V or 3.3V rails go out of tolerance by more than 500mV? yes \_\_\_ no\_\_\_
- ME10. RST# is asserted within 100nS after the 5V supply falls below the 3.3V rail by more than 300mV? yes \_\_\_ no\_\_\_
- ME11. REQ64# and ACK64# are pulled high at all components/slots that are NOT connected to the 64-bit data path, and are never driven low? yes \_\_\_ no\_\_\_
- ME12. The following signals are pulled up with a resistor of the correct value: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#? yes \_\_\_ no\_\_\_
- ME13. REQ64# and ACK64# are pulled up at each 32 bit connector?? yes \_\_\_ no\_\_\_
- ME14. Tprop from any driver (PCI compliant) to any receiver is less than or equal to Tcyc-(Tval+Tskew+Tsu), which evaluates to 10 nS for Tcyc = 30 ns in 33 Mhz PCI, and 5 ns for Tcyc = 15 ns in 66 Mhz PCI?  
*proven through: \_\_\_ simulation, \_\_\_ measurement, \_\_\_ other:\_\_\_\_\_*