1. PCI Engineering Change Notice – Addition of the SMBus to the PCI Connector

TITLE:	Addition of the SMBus to the PCI Connector
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1.1. Clarification

System management and reduced Total Cost of Ownership are increasingly important imperatives in the PC industry. To further these aims, many of today's systems contain motherboard instrumentation for temperature and voltage monitoring, asset tags, and chassis intrusion detection and more. A low-power, low-bandwidth serial bus interface, typically System Management Bus (SMBus), is the common communication link for such instrumentation. Furthermore, emerging manageability applications will be tied into this instrumentation and will require a connection between the motherboard and expansion boards. For more information refer to the justification described below. The primary barrier to these applications is the lack of a suitable standard interface connection on PCI card slots that can operate independently of the PCI bus itself. In these applications, for reasons of fault tolerance[1] and reliability, the link would be required to operate when the standard PCI bus is inoperative, powered down or otherwise unavailable. This is explained in more detail below. The current expedient, a cable between the motherboard and an add-in card to support these newer applications is highly undesirable for reasons of usability, cost, standardization and more.

The popular two-wire (clock and data) serial interface provides the desired attributes and functionality. It is a low signal-count interface that is well suited for the types of low bandwidth functions targeted. There is a multitude of devices commonly available and an SMBus host controller is incorporated into the majority of motherboard core logic chipsets today.

This ECN defines two reserved PCI connector pins as the SMBus interface clock and data signals.

1.2. Benefits

The capabilities enabled by adding the SMBus interface to the PCI connector include:

- Support for client management technologies, for example, used to alert remote machines of problems on local machines.
- Support for thermal sensors and other instrumentation devices on expansion boards
- Card identification when the PCI Configuration Space is inaccessible:
  - When the bus is in the B3 state
  - When the PCI device is in the D3hot or D3cold states

[1] Note that SMBus is not, in itself, a fault tolerant bus. However, it operates independently of the PCI bus, using, by the terms of this ECN, only two pins on the PCI connector. It is highly unlikely that a fault on the PCI bus will cause a fault on the SMBus and it is also unlikely that a fault on the PCI bus would occur when a fault occurs on the SMBus.

These new capabilities also enable system manufacturers to add value to their products reducing the total cost of ownership. A card or motherboard could be identified and have problems diagnosed remotely. Pre-failure warnings and asset management will benefit IS managers and service personnel. This directly results in an ownership cost reduction.

1.3. PCI Local Bus Specification, Rev. 2.2 Changes

Chapter 2 “Signal Definition”, following Section 2.2.9:

Insert the following:

2.2.10 System Management Bus Interface Pins (Optional)

The SMBus interface pins are collectively optional. If the optional management features described in Section 8 are implemented, **SMBCLK** and **SMBDAT** are both required.

SMBCLK	o/d	Optional SMBus interface clock signal. This pin is reserved for the optional support of **SMBCLK**.
SMBDAT	o/d	Optional SMBus interface data signal. This pin is reserved for the optional support of **SMBDAT**.

Chapter 4 “Electrical Specification”, Section 4.2.1.1 DC Specifications, Table 4-1, page 117:

Change as shown below:

NOTES:

1. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter include, **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#**, **SERR#**, **PERR#**, **LOCK#, INTA#**, **INTB#**, **INTC#**, **INTD#**, and, when used, **AD[63::32]**, **C/BE[7::4]#**, **PAR64**, **REQ64#**, and **ACK64#**.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for **CLK**, **SMBDAT**, and **SMBCLK**) with an exception granted to motherboard-only devices up to 16 pF, in order to accommodate PGA packaging. This means, in general, that components for expansion boards need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.). Pin capacitance for **SMBCLK** and **SMBDAT** is not specified, however the maximum capacitive load is specified for the expansion board in Section 8.2.5.
4. Lower capacitance on this input-only pin allows for non-resistive coupling to **AD[xx]**.
5. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.
6. This input leakage is the maximum allowable leakage into the **PME#** open drain driver when power is removed from V_{CC} of the component. This assumes that no event has occurred to cause the device to attempt to assert **PME#**.

Chapter 4 "Electrical Specification", Section 4.2.1.1 DC Specifications, Table 4-3, page 122:

Change as shown below:

NOTES:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.

2. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for **CLK**, **SMBDAT**, and **SMBCLK**) with an exception granted to motherboard-only devices up to 16 pF in order to accommodate PGA packaging. This would mean in general that components for expansion boards need to use alternatives to ceramic PGA packaging; i.e., PQFP, SGA, etc. Pin capacitance for **SMBCLK** and **SMBDAT** is not specified, however the maximum capacitive load is specified for the expansion board in Section 8.2.5.

4. Lower capacitance on this input-only pin allows for non-resistive coupling to **AD[xx]**.

5. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

6. This input leakage is the maximum allowable leakage into the **PME#** open drain driver when power is removed from V_{CC} of the component. This assumes that no event has occurred to cause the device to attempt to assert **PME#**.

Chapter 4 "Electrical Specification", Section 4.3.3 Pull-ups, page 135:

Change as shown below:

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes **FRAME#**, **TRDY#**, **IRDY#**, **DEVSEL#**, **STOP#**, **SERR#**, **PERR#**, **LOCK#**, **INTA#**, **INTB#**, **INTC#**, **INTD#**, **REQ64#**, and **ACK64#**. The point-to-point and shared 32-bit signals do not require pull-ups; bus parking ensures their stability. Refer to Section 3.8.1. for special requirements for terminating **AD[63::32]**, **C/BE[7::4]#**, and **PAR64.** Refer to Section 4.3.7. for pull-up and decoupling requirements for **PRSNT1#** and **PRSNT2#**. Refer to Section 7.7.7. for pull-up and decoupling requirements for **M66EN**.

~~Reserved pins 40A and 41A must be separately pulled up with an ~5 KΩ resistor to be consistent with previous versions of this specification. (Previous versions of this specification assigned functions to these pins.)~~ A system that does not support the optional SMBus interface must provide individual pull-up resistors (~5 KΩ) on the **SMBCLK** and **SMBDAT** pins for the expansion slot connectors. A system that supports the SMBus interface must provide pull-up devices (passive or active) on **SMBCLK** and **SMBDAT** as defined in the SMBus 2.0 Specification. Please see Chapter 8. The pull-ups must be connected to the power source attached to the 3.3Vaux pin of the PCI connector for systems with the optional auxiliary power supply and to +3.3V supply for systems without the optional supply. ~~Also, i~~If boundary scan is not implemented on the planar, **TMS** and **TDI** must be independently bused and pulled up, each with ~5 KΩ resistors, and **TRST#** and **TCK** must be independently bused and pulled down, each with ~5 KΩ resistors. **TDO** must be left open.

Chapter 4 “Electrical Specification”, Section 4.3.7 Connector Pin Assignments, page 143:

Table 4-1: PCI Connector Pinout

	5V System Environment		3.3V System Environment		
Pin	**Side B**	**Side A**	**Side B**	**Side A**	**Comments**
1	-12V	TRST#	-12V	TRST#	32-bit connector start
2	TCK	+12V	TCK	+12V	
3	Ground	TMS	Ground	TMS	
4	TDO	TDI	TDO	TDI	
5	+5V	+5V	+5V	+5V	
6	+5V	INTA#	+5V	INTA#	
7	INTB#	INTC#	INTB#	INTC#	
8	INTD#	+5V	INTD#	+5V	
9	PRSNT1#	Reserved	PRSNT1#	Reserved	
10	Reserved	+5V (I/O)	Reserved	+3.3V (I/O)	
11	PRSNT2#	Reserved	PRSNT2#	Reserved	
12	Ground	Ground	CONNECTOR KEY		3.3 volt key
13	Ground	Ground	CONNECTOR KEY		3.3 volt key
14	Reserved	3.3Vaux	Reserved	3.3Vaux	
15	Ground	RST#	Ground	RST#	
16	CLK	+5V (I/O)	CLK	+3.3V (I/O)	
17	Ground	GNT#	Ground	GNT#	
18	REQ#	Ground	REQ#	Ground	
19	+5V (I/O)	PME#	+3.3V (I/O)	PME#	
20	AD[31]	AD[30]	AD[31]	AD[30]	
21	AD[29]	+3.3V	AD[29]	+3.3V	
22	Ground	AD[28]	Ground	AD[28]	
23	AD[27]	AD[26]	AD[27]	AD[26]	
24	AD[25]	Ground	AD[25]	Ground	
25	+3.3V	AD[24]	+3.3V	AD[24]	
26	C/BE[3]#	IDSEL	C/BE[3]#	IDSEL	
27	AD[23]	+3.3V	AD[23]	+3.3V	
28	Ground	AD[22]	Ground	AD[22]	
29	AD[21]	AD[20]	AD[21]	AD[20]	
30	AD[19]	Ground	AD[19]	Ground	
31	+3.3V	AD[18]	+3.3V	AD[18]	
32	AD[17]	AD[16]	AD[17]	AD[16]	
33	C/BE[2]#	+3.3V	C/BE[2]#	+3.3V	
34	Ground	FRAME#	Ground	FRAME#	
35	IRDY#	Ground	IRDY#	Ground	
36	+3.3V	TRDY#	+3.3V	TRDY#	
37	DEVSEL#	Ground	DEVSEL#	Ground	
38	Ground	STOP#	Ground	STOP#	
39	LOCK#	+3.3V	LOCK#	+3.3V	
40	PERR#	~~Reserved~~ SMBCLK	PERR#	~~Reserved~~ SMBCLK	
41	+3.3V	~~Reserved~~ SMBDAT	+3.3V	~~Reserved~~ SMBDAT	
42	SERR#	Ground	SERR#	Ground	

Chapter 4 "Electrical Specification", Section 4.4.3.1 Trace Length Limits, page 151:

Trace lengths from the top of the expansion board's edge connector to the PCI device are as follows:

- The maximum trace lengths for all 32-bit interface signals are limited to 1.5 inches for 32-bit and 64-bit expansion boards. This includes all signal groups (refer to Section 2.2.) except those listed as "System Pins," "Interrupt Pins," ~~and~~ "JTAG Pins", and "SMBus Pins."
- The trace lengths of the additional signals used in the 64-bit extension are limited to 2 inches on all 64-bit expansion boards.
- The trace length for the PCI **CLK** signal is 2.5 inches ± 0.1 inches for 32-bit and 64-bit expansion boards and must be routed to only one load.

Chapter 4 "Electrical Specification", Section 4.4.3.4 Signal Loading, page 152:

Shared PCI signals must be limited to one load on the expansion board. Violation of expansion board trace length or loading limits will compromise system signal integrity. It is specifically a violation of this specification for expansion boards to:

- Attach an expansion ROM directly (or via bus transceivers) on any PCI pins.
- Attach two or more PCI devices on an expansion board, unless they are placed behind a PCI-to-PCI bridge.
- Attach any logic (other than a single PCI device) that "snoops" PCI pins.
- Use PCI component sets that place more than one load on each PCI pin; e.g., separate address and data path components.
- Use a PCI component that has more than 10 pF capacitance per pin.
- Attach any pull-up resistors or other discrete devices to the PCI signals, unless they are placed behind a PCI-to-PCI bridge.

The SMBus signal group is exempt from this requirement; refer to Section 8.2.5 for SMBus signal loading requirements.

After Chapter 7 add the following new Chapter:

Chapter 8
System Support for SMBus

The SMBus interface is based upon the *System Management Bus Specification*[2] (SMBus 2.0 Specification). This two-wire serial interface has low power and low software overhead characteristics that make it well suited for low-bandwidth system management functions. The capabilities enabled by the SMBus interface include, but are not limited to, the following:

- Support for client management technologies
- Support for server management technologies
- Support for thermal sensors and other instrumentation devices on expansion boards
- Card identification when the bus is in the B3 state or when the PCI device is in the $D3_{hot}$ or $D3_{cold}$ states as defined in the PCI Power Management Specification[3]

8.1 SMBus System Requirements

SMBus device interfaces must meet the electrical and protocol requirements in the SMBus 2.0 Specification.

The SMBus interface connections on the PCI connector are optional. However, if the SMBus interface is supported, then all of the following requirements must be met.

8.1.2 Power

It is recommended that the system board provide 3.3V auxiliary power to the PCI connector (pin 14A). This allows an expansion card to maintain SMBus functionality when the system is in a low power state.

8.1.3 Physical and Logical SMBus

A physical SMBus segment is defined as a set of SMBus device interfaces whose SMBCLK and SMBDAT lines are directly connected to one another (i.e., not connected through an SMBus

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[2] *System Management Bus (SMBus) Specification, Version 2.0*, available from the SMBus website at http://www.smbus.org.

[3] *PCI Bus Power Management Specification Version 1.1* available from the PCI Special Interest Group website at http://www.pcisig.com.

repeater or bridge). Each physical bus segment must meet the electrical requirements of the SMBus 2.0 Specification.

A logical SMBus is defined as one or more physical SMBuses having a single SMBus address space and a single SMBus arbitration domain. Multiple physical SMBus segments are connected into a single logical SMBus segments by means of bus repeaters. An SMBus address space is a logical connection of SMBus devices such that two devices with the same slave address will conflict with one another. An arbitration domain is a collection of one or more physical buses connected such that bus signal assertions caused by any device on any physical bus within the arbitration domain are seen by all devices on all the physical buses within the arbitration domain.

8.1.4 Bus Connectivity

Connection of SMBus to expansion slots is optional. However, if SMBus is connected to one slot in a chassis, it must be connected to all slots in that chassis. SMBus-connected slots in a chassis must be in the same logical SMBus. This logical SMBus may optionally be broken during system initialization or hot remove to allow the system to determine which SMBus device is in which PCI slot, but must be restored before the end of system initialization and during normal operation.

A typical implementation of a single physical SMBus is illustrated in the diagram below. The SMBus host bus controller is provided by the system.

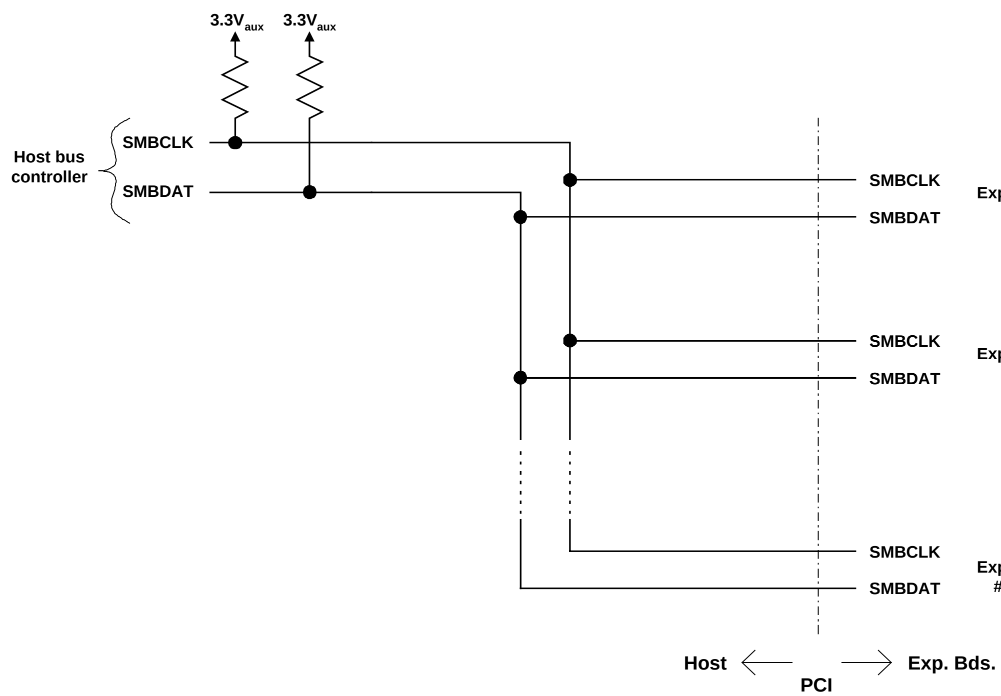

Figure 8-1. ?????????

An SMBus in any one chassis is not required to support connection to an SMBus in another chassis. This does not preclude connection to another chassis, but the specification of any such connection is outside the scope of this document.

System board configurations with one or more SMBus-connected PCI bus segments must contain a single logical SMBus between all the PCI bus segments. There is no correlation between PCI bus segments and SMBus physical buses. As such the SMBus is wired “around” a PCI bus bridge and not “through” it.

8.1.5 Master and Slave Support

As defined in the SMBus 2.0 Specification, an SMBus transaction occurs between a *master* and a *slave*. A *master* is a device that issues commands, generates the clock signal and terminates the bus transaction. A *slave* is a device that receives or responds to the bus transaction.

The system board supporting the SMBus interface must have both *slave* and *master* capability and support the *multi-master* arbitration mechanism as defined in the SMBus 2.0 Specification.

8.1.6 Addressing and Configuration

An address resolution protocol (ARP) is defined in the SMBus 2.0 specification that is used to assign slave addresses to SMBus devices. Although optional in the SMBus 2.0 specification, it is required that systems that connect the SMBus to PCI slots implement the ARP for assignment of SMBus slave addresses to SMBus interface devices on PCI expansion boards. The system must execute the ARP on a logical SMBus whenever any PCI bus segment associated with the logical SMBus exits the B3 state or a device in an individual slot associated with the logical SMBus exits the $D3_{cold}$ state. Prior to executing the ARP the system must insure that all ARP-capable SMBus interface devices are returned to their default address state[4].

The system may optionally support in a chassis inclusion of a single expansion board with an SMBus interface device with a fixed address in the range C6h – C9h. Such a system must not contain SMBus interface devices with a fixed address in this range and must not assign addresses in this range to other SMBus interface devices on PCI expansion boards. Such systems are not required to provide mechanisms to resolve conflicts if more than one such board is installed.

[4] The SMBus 2.0 Specification allows SMBus devices that are not associated with PCI expansion boards to have fixed SMBus addresses that are not assigned by the ARP. Such devices include, for example, system board temperature sensors. The SMBus slave addresses of such devices must be known to the system prior to the execution of the ARP and are not assigned to any ARP-capable SMBus devices.

Implementation Note: Fixed Address SMBus Interface Devices on an Expansion Board

Versions of the SMBus Specification prior to 2.0 did not include the ARP and SMBus interface devices compliant with those earlier specifications had fixed slave addresses. Many systems used such devices on the motherboard only. With the advent of the need for SMBus-enabled expansion boards and prior to this specification, a few expansion boards were introduced for special-purpose applications that included the available fixed-address SMBus interface devices with slave addresses fixed in the range C6h – C9h. This specification supports use of such expansion boards for backward compatibility. However, it is expected that all new designs will use the ARP and thereby avoid address-conflict problems.

The system may optionally implement a mechanism by which system configuration software performs a mapping of the associations between SMBus devices and physical expansion board slots. This mechanism determines the slot number in which an expansion board resides and associates this number with the address(s) of the SMBus interface device(s) on that expansion board. The system is permitted to isolate individual slots during the mapping process but must restore isolated slot connection states once the mapping process is complete.

8.1.7 Electrical

SMBus physical segments that connect to a PCI connector must use the high-power DC electrical specifications as defined in the SMBus 2.0 Specification.

The maximum capacitive load for a physical SMBus segment is 400 pF. If an SMBus physical segment includes PCI expansion slots, a maximum capacitance per expansion board of 40 pF must be used in calculations. The absolute value of the total leakage current for an SMBus physical segment, source and/or sink, must be less than 200 uA measured at 0.1 * Vcc and 0.9 * Vcc.

8.1.8 SMBus Behavior on PCI Reset

When power is applied to an SMBus device it must perform default initialization of internal state as specified in the SMBus 2.0 specification. SMBus device interface logic is not affected by **RST#**. This normally allows the SMBus to support communications when the PCI bus cannot.

8.2 Expansion-Board SMBus Requirements

8.2.1 Connection

Only PCI expansion boards that support the SMBus interface as described in the SMBus 2.0 Specification, including the address resolution protocol (ARP) are permitted to connect to the **SMBCLK** and **SMBDAT** pins. Any PCI expansion board implementing SMBus interface functionality via the PCI connector must connect to the **SMBCLK** and **SMBDAT** pins.

8.2.2 Master and Slave Support

An expansion board SMBus implementation that is intended to respond to commands or requests for data from a master must implement SMBus slave functionality and must support the Address Resolution Protocol.

Master capability is optional. However, if an expansion board implementation supports master capability, it must support multi-master arbitration.

8.2.3 Addressing and Configuration

Expansion board SMBus interface devices must implement the address resolution protocol (ARP) for establishing their slave addresses as defined in the SMBus 2.0 Specification. Although the ARP is optional in the SMBus 2.0 Specification, it is required by this specification.

8.2.4 Power

An expansion board is permitted to power its SMBus interface logic from the 3.3Vaux pin on the PCI connector if the board vendor intends that the board's SMBus functionality be available while the system is at a low power consumption state. Such a board must support PME# from ***D3****$_{cold}$*, as defined in the PCI Power Management Specification. Alternatively, the SMBus interface logic may be powered from the standard 3.3V supply.

8.2.5 Electrical

Expansion board SMBus interface devices must comply with the high-power electrical requirements stated in the SMBus 2.0 Specification.

Expansion board designers must meet the maximum-capacitance-per-board requirement of 40 pF per SMBus signal pin. The 40 pF limit includes:

- The sum of device capacitance loads
- The capacitance of trace length from the expansion board's PCI connector

The absolute value of the sum of the leakage current, source and/or sink, for all SMBus interface devices on the expansion board must be less than 20 uA measured at 0.1* Vcc and 0.9 * Vcc.

There is no limitation on the number of SMBus devices on an expansion card provided these requirements are met.

Implementation Note: SMBus Loading in a PCI Low-power State

When/if power is removed from SMBus interface logic when an associated PCI function is transitioned to a low-power state, the SMBus clock and data lines must not be loaded so as to make the SMBus inoperative. Other SMBus interfaces on the bus may still be powered and operational. The designer is reminded to observe the leakage current parameters in the SMBus 2.0 specification for unpowered SMBus interfaces.